System-Level Analysis of Mesh-Based Hybrid Optical-Electronic Network-on-Chip

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***Abstract*—Network-on-chip (NoC) can improve the performance, power efficiency, and scalability of multiprocessor system-on-chip (MPSoC). Optical NoCs, which are based on CMOS-compatible optical waveguides and microresonators, have significant bandwidth and power advantages over metallic interconnects. We propose a low-cost mesh-based hybrid optical-electronic NoC, HOME, with non-blocking 5x5, 4x4 and 3x3 optical switching fabrics. We systematically analyzed the key characteristics of HOME for a 64-core MPSoC in 45nm under different traffic conditions. Besides, we quantitatively analyzed the thermal effects in the 64-core HOME under temperature variations.**

I. Introduction

Multiprocessor system-on-chip (MPSoC) has become an important approach to achieving high performance by providing parallelization for a large number of functional units on a single chip. Optical network-on-chip (NoC) architectures were proposed to breakthrough the bottleneck of on-chip communication in MPSoCs. Vantrease *et al.* proposed a clustered optical NoC system Corona with a pure optical arbitration scheme [1]. Shacham *et al.* proposed a folded torus-based photonic circuit-switched network [2]. Gu *et al.* proposed a mesh-based optical NoC with low power loss and cost [3]. Pan *et al.* proposed Firefly and Flexishare [4] for global communication. Batten *et al.* proposed an optical NoC with the nodes connected as a mesh with global crossbar topology [5]. Kirman *et al.* proposed a hierarchical opto-electrical system, where an optical ring is used to connect electronic clusters [6]. The device aspects of a source-based optical link using heterogeneous integration for on-chip data transport was first presented in [7].

Regular topologies such as ring, mesh, and torus are widely used in NoC design because of their good scalability and simplicity. However communication locality is poorly supported in these common used topologies. The multi-hop communication path may result in a large latency and higher power consumption. NoC architectures with a higher communication locality are desired for better performance and energy efficiency. Researchers have explored this idea in a mesh-based clustered electronic NoC targeting high throughput computing [8]. Cores within a cluster are connected by a crossbar, while all the clusters are interconnected in a mesh-based electronic NoC.

In this paper, we proposed a low-cost mesh-based hybrid optical-electronic NoC, HOME, based on our previous work [9], and systematically analyzed the key characteristics of HOME under different traffic conditions. Low-cost non-blocking 5x5, 4x4 and 3x3 optical switching fabrics are proposed to reduce the cost of microresonators. We developed SystemC-based cycle-accurate NoC simulators and compared the performance of HOME with a matched optical mesh NoC for a 64-core MPSoC in 45nm. Besides, we quantitatively analyzed the thermal effects in HOME under temperature variations. The rest of the paper is organized as follows. Section II details the HOME architecture with new router designs. Section III shows the simulation results and comparison. Section IV draws the conclusions.

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II. HOME Architecture and Router

HOME (Figure 1) is a hierarchical hybrid optical-electronic mesh NoC with HOME routers. The HOME router is a hybrid optical-electronic router, consisting of an optical switching fabric, an electronic switching fabric, a router control unit (RCU) and an optical/electronic (O/E) interface. Inside each cluster, four processor cores are connected to a HOME router with metallic interconnects. For intra-cluster traffic, local electronic switching fabric is used for a fast switching. Optical switching fabrics are interconnected with optical waveguides to form a mesh-based NoC for inter-cluster communication. An overlapping electronic mesh serves as a control network for path maintenance.

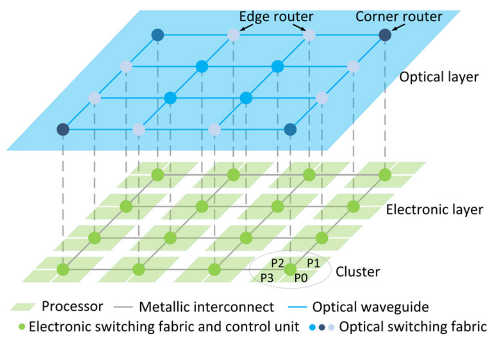

Fig. 1. HOME for a 64-core MPSoC

Before each inter-cluster transmission, a dimension-order-routing optical path is reserved by routing a setup packet in the electronic control network. If the path reservation is successful, an acknowledgement (ACK) signal would be sent back to the source along the reserved optical path. Upon

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receiving the ACK, the source will pass the payload to the O/E interface. At the same time, a single-flit tear-down packet will be sent to the destination through the electronic control network. It contains a time-to-live (TTL) field which indicates the necessary number of clock cycles for the payload transmission. The number in the TTL field will be decreased with elapsed cycles by each router along the path. Upon receiving the tear-down packet, RCUs in the path will set the corresponding countdown counter based on the TTL field and start the countdown immediately. Resources associated with the transmission will be released when the countdown counter is timeout.

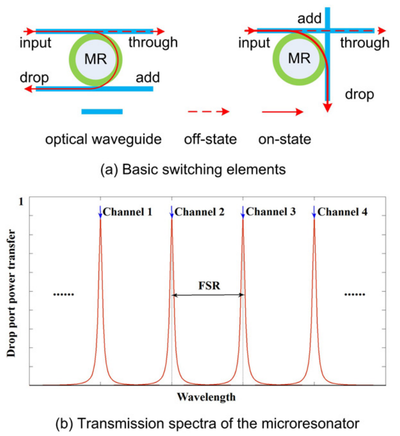

Fig. 2. Basic switching elements and the transmission spectra

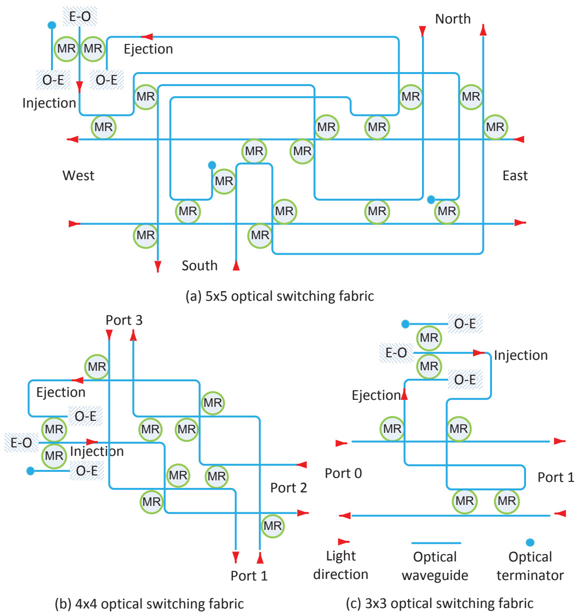

Fig. 3. 5x5, 4x4, 3x3 non-blocking optical switching fabrics

The optical switch fabric in HOME router is based on the basic 1x2 optical switching element (Figure 2). Based on the technique of comb switching, a single microresonator (MR) can support wavelength-division multiplexing (WDM) by simultaneously switching on/off multiple wavelengths [10]. Figure 3(a) shows a 5x5 strictly non-blocking optical switching fabric [11]. The internal structure of the 5x5 router is optimized to minimize the number of MRs, waveguide crossings, and MR switching activities. For HOME routers at network edges, 4x4 optical switching functions are enough to satisfy the connect requirement (three neighboring routers and the local O/E interface). For HOME routers at the four corners, only 3x3 optical switching functions are needed. In order to further reduce the cost of optical resource, we newly design a 4x4 optical switching fabric and a 3x3 optical switching fabric for the edge routers (Figure 3). The two reduced optical switching fabrics use 8 less MRs and 12 less MRs respectively than the 5x5 optical switching fabric. We use a small circuit with each optical switching fabric to implement the optical ACK mechanism, in case the O/E interfaces of the communication pair are not available to send or receive the optical ACK. It uses one additional O-E receiver and two additional MRs. In case that it is going to send an optical ACK while sending payload data, the power emission of the E-O transmitter is doubled to counteract the additional power loss of the optical ACK. The three optical switching fabrics do not need to turn on any MRs if light passes from south to north, east to west and vice-versa. With the passive routing feature, the number of switching stages in a dimension-order-routing path is three at most. As illustrated in [12], the number of switching stages in an optical link directly affects the total optical power loss under thermal variations, and thus dominates the thermal-induced power overhead. We show the analysis of thermal effects in Section III.

TABLE I
OPTICAL RESOURCES COST OF DIFFERENT COMMUNICATION ARCHITECTURES, 64-CORE

	HOME	OM	Torus [2]	Corona [1]
Optical switching fabric	16	64	256	/
MR	176	1024	2048	258K
Laser source	64	256	64	/
Photodetector	80	256	64	5K

Table I shows the cost of a 64-core HOME. It uses 16 optical routers in total, and 12 of them are at network edges. By using low-cost edge/corner routers, the total number of MR is reduced from 288 to 176. Each E-O interface requires four laser sources for four-wavelength WDM, and the 64-core HOME uses 64 laser sources in total. The matched optical mesh NoC (OM) is an 8x8 mesh-based optical NoC with the 5x5 optical router [13]. The OM is also with four-wavelength WDM for 40Gbps data link bandwidth, and it requires 256 laser sources in total. For a 64-core system, HOME only needs 8.6% of MRs used by [2] and 0.066% of MRs used by Corona.

III. COMPARISON AND ANALYSIS

We evaluated the network throughput, latency, and power consumption of HOME for a 64-core MPSoC in 45nm, and compared it with the matched optical mesh NoC (OM).

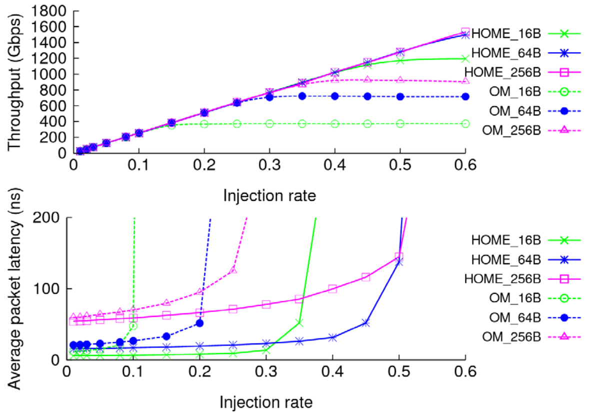

Fig. 4. Network throughput and the average packet latency of the 64-core MPSoC, SD=0.5

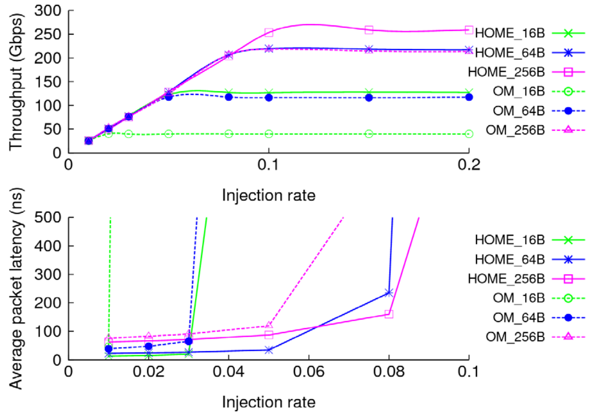

Fig. 6. Network throughput and the average packet latency of the 64-core MPSoC with uniform traffic

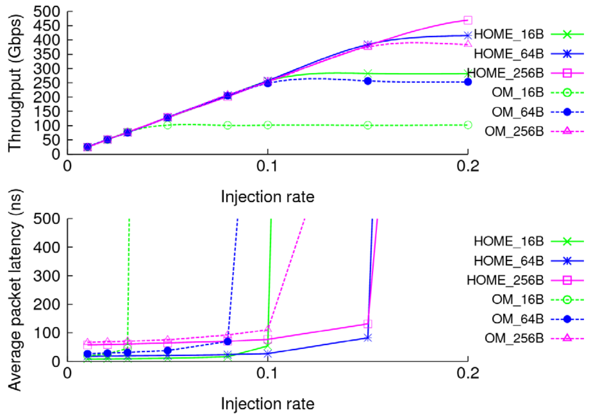

Fig. 5. Network throughput and the average packet latency of the 64-core MPSoC, SD=2

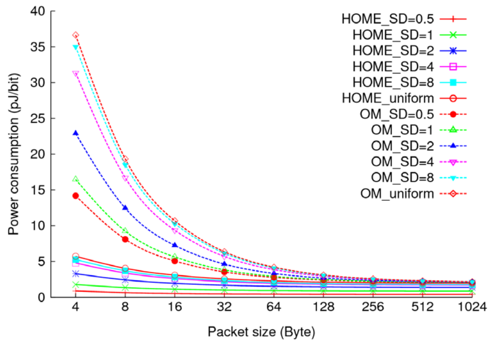

Fig. 7. Power consumption for the 64-core MPSoC

A. Network Throughput and Latency

SystemC-based cycle-accurate NoC simulators were developed for network simulations. For localized traffic, we model the destination addresses according to a Gaussian distribution with different value of standard deviation (SD). Network throughput and average packet latency of the 64-core HOME are shown in Figure 4 to Figure 6. Four packet sizes ranging from 16-byte to 256-byte were simulated. When SD equals to 0.5, the traffic is highly localized which leads to the highest throughput achieved by both NoCs. With a packet size of 64 bytes, HOME has a throughput of 1607Gbps and the matched optical mesh has a throughput of 716Gbps. The average packet latency in HOME is 18ns before network saturation, with a 43% reduction compared to the optical mesh. After network saturation, congestions dominate the packet delay and the average packet latency increases quickly to μs. When SD equals to two, inter-cluster traffic takes a larger percentage and HOME still outperforms the matched optical mesh significantly.

For uniform traffic, about 95% of traffics are inter-cluster. In this case, the benefits from the use of local switching fabric are greatly reduced. When packet size equals to 64-byte, HOME shows an 85% higher throughput compared to the matched optical mesh. The difference is even larger than in the case of SD equal to two. For the average packet latency in the unsaturated network, the latency of HOME is 22ns which is 42% lower than the matched optical mesh. This shows the increases in the efficiency of the optical circuit switching brought by the proposed hierarchical architecture and protocol.

B. Power Consumption

We designed and simulated the electronic part of the HOME router based on the 45nm Nangate open cell library and Predictive Technology Model in Cadence Spectre. It works at 1.25GHz and the power consumption is about 10.85mW/GHz. It has an area of 27012μm^2. Simulation results show that on average the crossbar of the router consumes 0.07pJ/bit, the input buffer consumes 0.003pJ/bit, and the RCU consumes 1.8pJ to make decisions for each packet. For the metal wires, global interconnect takes 0.62pJ/bit for the communication between routers. Local interconnect between router and processor takes 0.04pJ/bit. HOME achieves a good power efficiency since the intra-cluster transmissions only involve the local crossbar and two short local interconnects without any power-hungry electrical global wire. Power consumption of HOME and the matched optical mesh is measured under various traffic patterns (Figure 7). While the optical mesh consumes 3.4pJ/bit to transmit 64-byte packets (SD=2), HOME only consumes

1.53pJ/bit, which is 55% lower. When the locality increases, e.g. SD equal to 0.5, the power consumption of HOME reduces to 0.42pJ/bit and the energy reduction compared to the matched optical mesh is further increased to 84%. For uniform traffic with 64-byte packet, the power consumption of HOME is 2.28pJ/bit which still saves 47% power compared to the matched optical mesh.

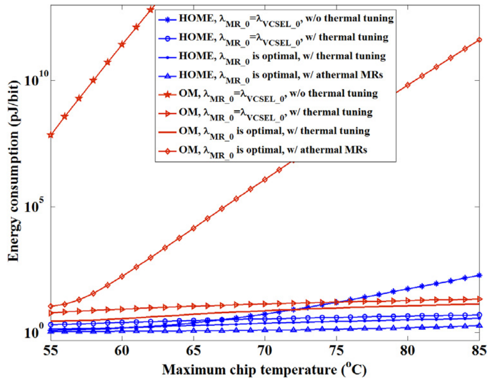

Fig. 8. Worst-case power overhead due to thermal variations

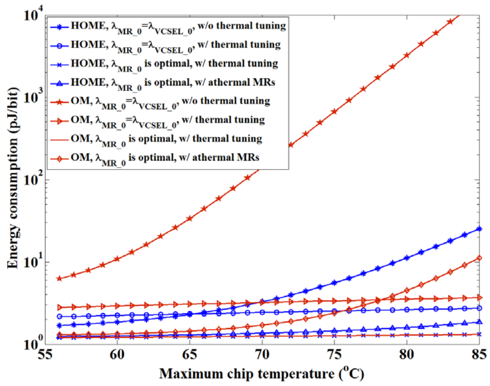

Fig. 9. Average-case power overhead due to thermal variations

Based on the system-level optical NoC thermal model proposed in [12], we quantitatively evaluated the thermal-induced power overhead in the 64-core HOME and compared it with the matched optical mesh NoC (OM) (Figure 8, Figure 9). We assume that the minimum chip temperature is $55^{o}C$, and the 3-dB bandwidth of MRs is $3.1nm$. We assume the receiver sensitivity is -14.2dBm [14]. The number of switching stages in an optical link directly affects the total optical power loss under thermal variations. The passive-routing HOME optical routers guarantee that the maximum number of switching stages in the 64-core HOME is three. For comparison, the worst-case number of switching stage is 15 in the matched 64-core optical mesh NoC with the 5x5 optical router [13]. By applying the optimal device setting [12] and local thermal tuning, the worst-case thermal-induced power overhead in HOME and the matched optical mesh NoC are improved to $3.7pJ/bit$ and $13pJ/bit$ respectively, when the maximum chip temperature reaches $85^{o}C$. By combining the technique of optimal device setting with thermal tuning, the average-case power overhead in HOME is about $1.3pJ/bit$. If using the technique of athermal (temperature insensitive) MRs, the average-case power overhead in HOME and the matched optical mesh NoC is about $1.8pJ/bit$ and $11pJ/bit$.

IV. CONCLUSIONS

We systematically analyzed the key characteristics of a mesh-based hybrid optical-electronic NoC, HOME, for a 64-core MPSoC in 45nm under different traffic conditions. Simulation results show that HOME achieves a better performance and energy efficiency compared with a matched optical mesh NoC. Besides, we quantitatively analyzed the power overhead in the 64-core HOME under thermal variations.

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