Digital electronics 1

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The repository contains VHDL lab exercises for bachelor course *Digital Electronics 1* at Brno University of Technology, Czechia.

Exercises

EDA Playground

- Introduction to Git and VHDL
- Combinational logic

Vivado

- Introduction to Vivado
- Seven-segment display decoder
- Binary counter
- Driver for multiple seven-segment displays
- Stopwatch
- Traffic light controller

Project

- General instructions

Materials

The following hardware and software components are mainly used in the lab.

Hardware

- Nexys A7 Artix-7 FPGA Trainer Board: reference manual, schematic, XC7A50T-1CSG324C FPGA, Nexys-A7-50T-Master.xdc
- Oscilloscope Keysight Technologies DSOX3034T (350 MHz, 4 analog channels), including 16 logic timing channels DSOXT3MSO and serial protocol triggering and decode options D3000BDLA

Software

- EDA Playground
- Vivado Design Suite 2020.1: installation

References

1. ES 4 VHDL reference sheet
2. Digital electronics 1 wiki
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4. CHU, Pong P. *FPGA prototyping by VHDL examples*. Hoboken, N.J.: Wiley-Interscience, c2008. ISBN 978-0-470-18531-5.
5. MANO, M. Morris. Digital Design: With an Introduction to the Verilog, HDL, VHDL, and System Verilog. Pearson, 6th edition, 2018. ISBN-13: 978-1292231167.
6. KALLSTROM, P. A Fairly Small VHDL Guide. Version 2.1.
7. GitHub GIT CHEAT SHEET