MachXO3 sysIO Usage Guide

May 2016 Technical Note TN1280

Introduction

The MachXO3™ PLD family sysIO™ buffers are designed to meet the needs of flexible I/O standards in today's fast-paced design world. The supported I/O standards range from single-ended I/O standards to differential I/O standards so that users can easily interface their designs to standard buses, memory devices, video applications and emerging standards. This technical note provides a description of the supported I/O standards and the banking scheme for the MachXO3L/LF PLD family. The sysIO architecture and the software usage are also discussed to provide a better understanding of the I/O functionality and placement rules.

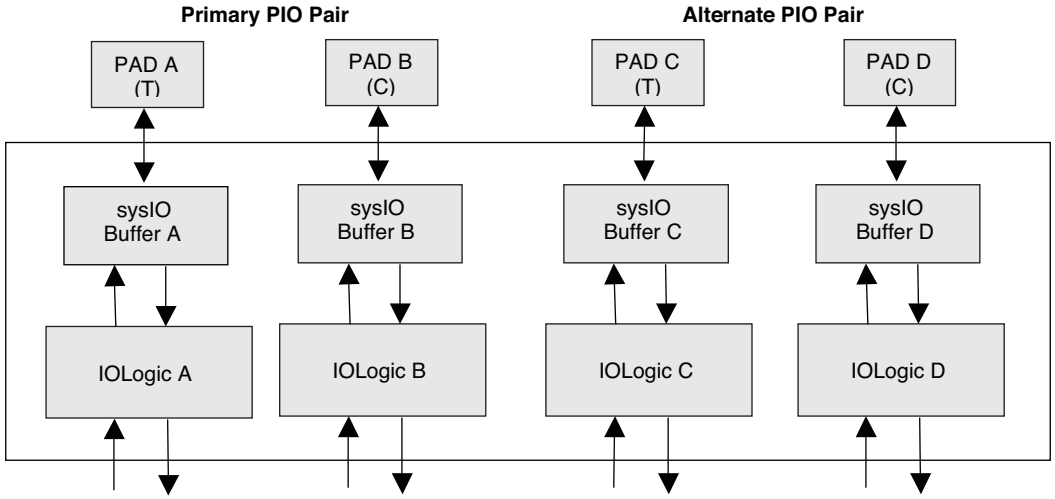
sysIO Buffer Overview

The basic building block of the MachXO3L/LF sysIO is the Programmable I/O Cell (PIC) block. There are four types of PIC blocks in the MachXO3L/LF device architecture. These include the basic PIC block, the memory PIC block for DDR memory support, the receiving PIC block with gearing, and the transmitting PIC block with gearing. The PIC blocks with gearing are used for video and high-speed applications. The PIC blocks with gearing have a built-in control module for word alignment. The details of the gearing PIC block can be found in TN1281, Implementing High-Speed Interfaces with MachXO3 Devices.

A common feature of all four types of PIC blocks is that each PIC block consists of four programmable I/Os (PIOs). Each PIO includes a sysIO buffer and an I/O logic block. A simplified sysIO block diagram is shown in Figure 1. The I/O logic block consists of an input block, an output block, and a tri-state block. These blocks have registers, input delay cells, and the necessary control logic to support various operational modes. The sysIO buffer determines the compliance to the supported I/O standards. It also supports features like hysteresis to meet common design needs. The I/O logic block and the sysIO buffer are designed with a minimal use of die area; providing easy bus interfacing, and pin out efficiency.

Two adjacent PIOs can form a pair of complementary output drivers. In addition, PIOA and PIOB of the PIC block form the primary pair of the buffer, while PIOC and PIOD form the alternate pair of the buffer. The primary pairs have additional capability that is not available on the alternate pair. The sysIO buffers of the PIC block are equivalent when implemented as the single-ended I/O standards.

Figure 1. PIC Block Diagram



Supported sysIO Standards

The Lattice MachXO3L/LF sysIO buffer supports both single-ended and differential standards. The internally ratioed standards support individually configurable drive strength and bus maintenance circuits (weak pull-up, weak pull-down, or bus keeper).

All banks of the MachXO3L/LF devices support true differential inputs, and emulated differential outputs using external resistors and the complementary LVCMOS outputs. The true-LVDS differential outputs and LVDS input termination are supported in specific banks as described in the sysIO Banking Scheme section of this document.

Table 1. Supported Input Standards

Input Standard	V_{REF} (Nominal)	V_{CCIO}[1] (Nominal)
Single-Ended Interfaces		
LVTTL33	—	—
LVCMOS33	—	—
LVCMOS25	—	—
LVCMOS18	—	—
LVCMOS15	—	—
LVCMOS12	—	—
Differential Interfaces		
LVDS25	—	—
LVPECL33	—	—
MLVDS25	—	—
BLVDS25	—	—
LVTTL33D	—	—
LVCMOS33D	—	—
MIPI[2]	—	—

1. If not specified, refer to mixed voltage support in the VCCIO Requirement section.
2. This interface can be emulated with external resistors.

Table 2. Supported Output Standards

Output Standards	Drive (mA)	V_{CCIO} (Nominal)
Single-Ended Interfaces		
LVTTL33	4, 8, 12, 16	3.3
LVCMOS33	4, 8, 12, 16	3.3
LVCMOS25	4, 8, 12	2.5
LVCMOS18	4, 8, 12	1.8
LVCMOS15	4, 8	1.5
LVCMOS12	2, 6	1.2
Differential Interfaces		
LVDS25	3.5	2.5, 3.3
LVDS25E	8	2.5
LVPECL33E	16	3.3
MLVDS25E	16	2.5
BLVDS25E	16	2.5
LVTTL33 Differential	4, 8, 12, 16	3.3
LVCMOS33 Differential	4, 8, 12, 16	3.3
LVCMOS25 Differential	4, 8, 12	2.5
MIPI[1]	2	2.5

1. This interface can be emulated with external resistors.

Note: Refer to RD1182, MIPI D-PHY Interface IP for information on support for MIPI Input and Output.

sysIO Banking Scheme

The MachXO3L/LF family has a non-homogeneous I/O banking structure. MachXO3L/LF-640 and MachXO3L/LF-1300 have four I/O banks each with one I/O bank per side. MachXO3L/LF-1300, MachXO3L/LF-2100, MachXO3L/LF-4300, MachXO3L/LF-6900 and MachXO3L/LF 9400 devices have six I/O banks each, with one I/O bank on each of the top, bottom and right sides, and three banks on the left side.

The MachXO3L/LF devices support true LVDS differential outputs through the primary pairs on the top bank (Bank 0). These devices also support 100 Ohm differential input termination on every I/O pair on the bottom I/O bank.

Each of the I/O pins on all MachXO3L/LF PLDs has a clamp feature which can be disabled or enabled. This clamp is similar to the PCI clamp but it is not PCI compliant. The arrangements of the I/O banks are shown in Figure 2 and Figure 3.

Figure 2. MachXO3L/LF-640 and MachXO3L/LF-1300 I/O Banking Arrangement

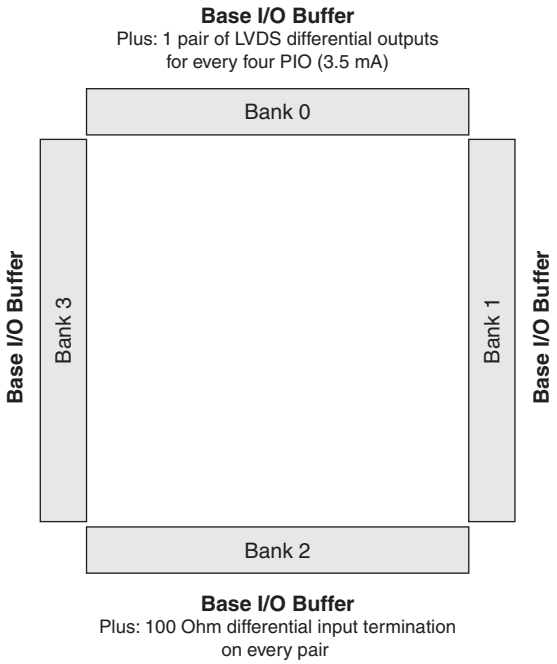
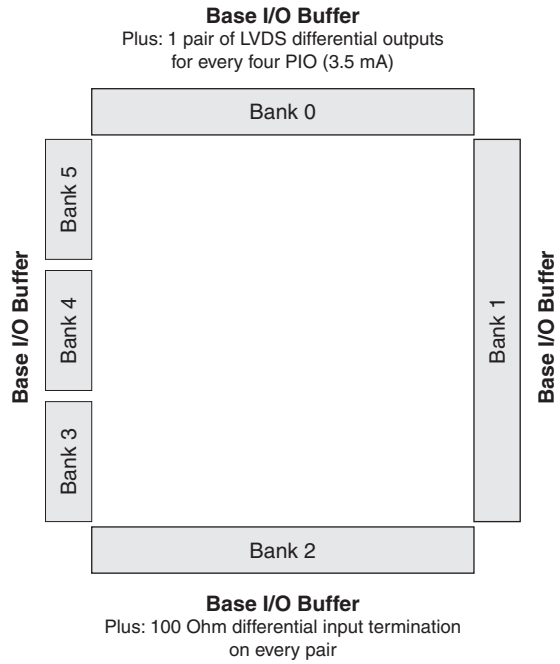


Figure 3. MachXO3L/LF-1300, MachXO3L/LF-2100, MachXO3L/LF-4300, MachXO3L/LF-6900 and MachXO3L/LF-9400 I/O Banking Arrangement



sysIO Standards Supported by I/O Banks

All banks can support multiple I/O standards under the V_{CCIO} rules discussed above. Table 3 and Table 4 summarize the I/O standards supported on various sides of the MachXO3L/LF device.

Table 3. Single-Ended I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
LVTTL33	Yes	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes	Yes

Table 4. Differential I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
LVDS output	Yes[1]	—	—	—
LVPECL33E[2]	Yes	Yes	Yes	Yes
MLVDS25E[2]	Yes	Yes	Yes	Yes
BLVDS25E[2]	Yes	Yes	Yes	Yes
LVDS25E[2]	Yes	Yes	Yes	Yes
LVTTL33D output	Yes	Yes	Yes	Yes
LVCMOS33D output	Yes	Yes	Yes	Yes
LVCMOS25D output	Yes	Yes	Yes	Yes
LVDS input	Yes	Yes	Yes	Yes
LVPECL33 input	Yes	Yes	Yes	Yes
MLVDS25 input	Yes	Yes	Yes	Yes
BLVDS25 input	Yes	Yes	Yes	Yes
LVTTL33D input	Yes	Yes	Yes	Yes
LVCMOS33D input	Yes	Yes	Yes	Yes
LVCMOS25D input	Yes	Yes	Yes	Yes
MIPI	Yes	Yes	Yes	Yes

1. True LVDS output is supported at the top bank.
2. Emulated output standards are denoted with a trailing “E” in the name of the standard.

Power Supply Requirements

The MachXO3L/LF device family has a simplified power supply scheme for sysIO buffers. The core power V_{CC} and the bank power V_{CCIO} are the two main power supplies. A MachXO3L/LF device can be powered and operated with a single power supply by connecting V_{CC} and V_{CCIO} to nominal voltages of 1.2 V. The JTAG programming pins are powered by V_{CCIO} in bank 0 where the JTAG pins reside. All the user sysIOs have a weak pull-down after power-up is complete and before the device configuration is done.

V_{CCIO} Requirement for I/O Standards

Each I/O bank of a MachXO3L/LF device has a separate V_{CCIO} supply pin that can be connected to 1.2 V, 1.5 V, 1.8 V, 2.5 V or 3.3 V. This voltage is used to power the output I/O standard and source the drive strength for the output. In addition to this, V_{CCIO} also powers the ratioed input buffers such as LVTTL and LVCMOS. This ensures that the threshold of the input buffers is tracking the V_{CCIO} voltage level.

Input buffer set up to be a 1.2 V ratioed input can be used on bank set to any VCCIO. This is possible because the MachXO3L/LF sysIO buffer has two ratioed input buffers connected to V_{CCIO} and V_{CC} in parallel.

Table 5. Mixed Voltage Support for LVCMOS and LVTTL I/O Types[8]

	Inputs						Outputs					
V_{CCIO}	**1.0 V**	**1.2 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**1.0 V**	**1.2 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**
1.2 V		YES	YES[6]					YES				
1.5 V		YES[1]	YES	YES[6]	YES[6]	YES[6]			YES			
1.8 V		YES[1]	YES[5]	YES	YES[6]	YES[6]				YES		
2.5 V	YES[1, 9]	YES[1, 10]	YES[2, 5, 7]	YES[3, 5, 7]	YES	YES[6]	YES[11]	YES[11]			YES	
3.3 V	YES[1, 9]	YES[1, 10]	YES[2, 5, 7]	YES[3, 5, 7]	YES[4, 5, 7]	YES	YES[11]	YES[11]				YES

1. Leakage will occur if bus hold or weak pull-up is turned on.
2. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS15R25 or LVCMOS15R33 with the referenced input buffer.
3. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS18R25 or LVCMOS18R33 with the referenced input buffer.
4. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS25R33 with the referenced input buffer.
5. Under-drive condition when using the ratioed input buffer and the input standard voltage is below Vccio
   a. Under-drive causes higher DC current when the IO is at logic high. It is recommended to use Power Calculator to estimate the power consumption under such condition.
   b. Hysteresis is not supported. In the Diamond software, HYSTERESIS must be set to NA.
   c. CLAMP is not supported. In the Diamond software, CLAMP must be set to OFF.
   d. IO termination is not supported. In the Diamond software, PULLMODE must be set to NONE.
6. Over-drive condition when using the ratioed input buffer and the input standard voltage is above Vccio
   a. Hysteresis is not supported. In the Diamond software, HYSTERESIS must be set to NA.
   b. CLAMP is not supported. In the Diamond software, CLAMP must be set to OFF.
   c. IO termination is not supported. In the Diamond software, PULLMODE must be set to NONE.
7. Ratioed input buffer in under-drive conditions is preferred over referenced input buffer due to lower power requirement for the ratioed input buffer.
8. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting shall be NA, the CLAMP setting shall be OFF, and the UP and KEEPER PULLMODE settings are not supported.
9. This input standard can be supported using the I/O types LVCMOS10R25 or LVCMOS10R33 with the referenced input buffer.
10. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS12R25 or LVCMOS12R33 with the referenced input buffer.
11. This output standard is supported as a Bidirectional open-drain buffer only. IO termination is not supported. In the Diamond software, OPENDRAIN must be set to ON, PULLMODE must be set to NONE, and CLAMP must be set to OFF.

For differential input standards, certain mixed voltage support is allowed in the architecture as shown in Table 6.

Table 6. Mixed Voltage Support for Differential Input Standards

Vccio	Differential Inputs		
	LVDS LVPECL33 MLVDS25 BLVDS25	LVTTL33D LVCMOS33D	LVCMOS25D
1.2 V			
1.5 V			
1.8 V			
2.5 V	YES		YES
3.3 V	YES	YES	YES

Input Reference Voltage

To support Mixed Voltage I/O using the referenced input buffer, each I/O bank supports one reference voltage (V_{REF}). Any I/O in the bank can be configured as the input reference voltage pin. This pin is a regular I/O if it is not used as reference voltage input. The input reference voltage can also be generated internally from the V_{REF} generator. Again, there is one V_{REF} generator per bank and its programmable settings include OFF, 45% of V_{CCIO}, 50% of V_{CCIO}, and 55% of V_{CCIO}. Programming of the internal V_{REF} generator and the external V_{REF} pin cannot be set at the same time for a particular bank because there is only one V_{REF} bus per bank.

sysIO Buffer Configuration

Each sysIO buffer pair is made of two PIO buffers. PIO A and B pads form the primary pair, and PIO C and D pads form the alternate pair. Pads A and C of the pair are considered the “true” pad, while pads B and D are considered the “comp” pad. The “true” pad is associated with the positive side of the differential signal, while the “comp” pad is associated with the negative side of the differential signal.

All the PIOs support bus maintenance circuitry to allow a weak pull-up, or a weak pulldown, or a weak bus keeper. The LVDS sysIO buffer pairs have additional LVDS output drivers in the primary PIO and are available on the top side of the device. The bottom sysIO buffer pairs have additional 100 Ohm termination resistors between the “true” and “comp” pads.

LVCMOS Buffer Configurations

The LVCMOS buffers can be configured in a variety of modes to support common circuit design needs.

Bus Maintenance circuit

Each pad has a weak pull-up, weak pull-down, and weak bus-keeper capability. These are selected with ON and OFF programmability. The pull-up and pull-down settings offer a fixed characteristic, which is useful in creating wired logic such as wired ORs. The bus-keeper option latches the signal in the last driven state, holding it at a valid level with minimal power dissipation. Input leakage can be minimized by turning off the bus maintenance circuitry. However, it is important to ensure that inputs are driven to a known state to avoid unnecessary power dissipation in the input buffer. The bus maintenance circuit is available for single-ended ratioed I/O standards.

Programmable Drive Strength

All single-ended drivers have programmable drive strength. This option can be set for each I/O independently. The drive strengths available for each I/O standard can be found in Table 8. The MachXO3L/LF programmable drive architecture is guaranteed with minimum drive strength for each drive setting. The V/I curves in the data sheet provide details of output driving capability versus the output load. This information, together with the current per bank and the package thermal limit current, should be taken into consideration when selecting the drive strength.

Input Hysteresis

VIH is the trip point for a low-to-high transition and VIL is the trip point for a high-to-low transition, hysteresis voltage is the difference between VIH and VIL. Hysteresis is used to prevent several quick successive changes if the input signal contains some noise, for example. The noise could mean that you cross the trip point more than just once, which causes a glitch in the system.

All ratioed input receivers, except LVCMOS12, support input hysteresis. The input hysteresis for the LVCMOS33, LVCMOS25, LVCMOS18 and LVCMOS15 have two settings for flexibility. The ratioed input receivers have no input hysteresis when they are operated in under-drive or over-drive input conditions as shown in Table 7.

Programmable Slew Rate

The single-ended output buffer for each device I/O pin has programmable output slew rate control that can be configured for either low noise (SLEWRATE=SLOW) or high speed (SLEWRATE=FAST) performance. Each I/O pin has an individual slew rate control. This slew rate control affects both the rising edge and the falling edges. The rise and fall ramp rates for each I/O standard can be found in the in the device IBIS file for a given I/O configuration.

Tri-state and Open Drain Control

Each single-ended output driver has a separate tri-state control in addition to the global tri-state control for the device. The single-ended output drivers also support open drain operation on each I/O independently. The open drain output is typically pulled up externally and only the sink current specification is maintained.

Differential Buffer Configurations

The sysIO buffer pair supports differential input standards. The top and bottom edges support some additional functions over those supported by the base sysIO buffer pairs.

Differential Receivers

All the sysIO buffer pairs support differential input on all edges of the device. When a sysIO buffer pair is configured as differential receiver, the input hysteresis and the bus maintenance capabilities will be disabled for the buffer.

On-Chip Input Termination

The MachXO3L/LF device supports on-chip 100 Ohm (nominal) input differential termination on the bottom edge. The termination is available on all input PIO pairs of the bottom edge and is programmable.

Emulated Differential Outputs

All sysIO buffer pairs support complementary outputs as described above. This feature can be used to drive complementary LVCMOS signals. It can also be used together with off-chip resistor networks for emulating the differential output standards such as LVPECL, MLVDS, MIPI and BLVDS differential standards. When a sysIO buffer pair is configured as differential transmitter, the bus maintenance and open drain capabilities will be disabled. All single-ended sysIO buffers pairs in the MachXO3L/LF family can support emulated differential output standards.

True Differential Output And Output Drive

MachXO3L/LF devices support true differential output drivers on the top edge of these devices. These true differential outputs are only available on the primary PIO pairs. The output driver has a fixed common mode of 1.2 V and a programmable drive current of 3.5 mA. The bank V_{CCIO} for true differential output can be 2.5 V or 3.3 V.

Software sysIO Attributes

The sysIO attributes or primitives must be used in the Lattice development software to control the functions and capabilities of the sysIO buffers. sysIO attributes or primitives can be specified in the HDL source code, in the Lattice Diamond™ Spreadsheet View GUI, or in the ASCII preference file (.lpf) file directly. Appendices A, B and C list examples of using such attributes in different environments. This section describes each of these attributes in detail.

HDL Attributes

All the attributes discussed in this section, except two, can be used in the HDL source code to direct the sysIO buffer functionality.

IO_TYPE

This attribute is used to set the sysIO standard for an I/O. The V_{CCIO} required to set these I/O standards are embedded in the attribute names. The BANK VCCIO attribute is used to specify allowed V_{CCIO} combinations for each I/O type. Table 7 shows the valid I/O types for the MachXO3L/LF family.

Table 7. Supported I/O Types

sysIO Signaling Standard	IO_TYPE
LVDS 2.5 V	LVDS25
Emulated LVDS 2.5 V[1]	LVDS25E
Bus LVDS 2.5 V	BLVDS25
Emulated Bus LVDS 2.5 V[1]	BLVDS25E
MLVDS 2.5 V	MLVDS25
Emulated MLVDS 2.5 V[1]	MLVDS25E
LVPECL 3.3 V	LVPECL33
Emulated LVPECL 3.3 V[1]	LVPECL33E
LVTTL 3.3 V	LVTTL33
LVTTL 3.3 V differential[2]	LVTTL33D
LVCMOS 3.3 V	LVCMOS33
LVCMOS 3.3 V differential[2]	LVCMOS33D
LVCMOS 2.5 V (default)	LVCMOS25
LVCMOS 2.5 V differential[2]	LVCMOS25D
LVCMOS 2.5 V in 3.3 V VCCIO bank[3]	LVCMOS25R33
LVCMOS 1.8 V	LVCMOS18
LVCMOS 1.8 V in 3.3 V VCCIO bank[3]	LVCMOS18R33
LVCMOS 1.8 V in 2.5 V VCCIO bank[3]	LVCMOS18R25
LVCMOS 1.5 V	LVCMOS15
LVCMOS 1.5 V in 3.3 V VCCIO bank[3]	LVCMOS15R33
LVCMOS 1.5 V in 2.5 V VCCIO bank[3]	LVCMOS15R25
LVCMOS 1.2 V	LVCMOS12
LVCMOS 1.2 V in 3.3 V VCCIO bank[4]	LVCMOS12R33
LVCMOS 1.2 V in 2.5 V VCCIO bank[4]	LVCMOS12R25
LVCMOS 1.0 V in 3.3 V VCCIO bank[4]	LVCMOS10R33
LVCMOS 1.0 V in 2.5 V VCCIO bank[4]	LVCMOS10R25
MIPI	MIPI

1. These differential output standards are emulated by using a complementary LVCMOS driver pair together with an external resistor pack.
2. These differential standards are implemented by using a complementary LVCMOS driver pair.
3. These are input only and require VREF to be set to certain value to allow the specified I/O types to be used.
4. These are input or bidirectional only and require VREF to be set to certain value to allow the specified I/O types to be used.

DRIVE

The DRIVE strength attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used. Table 8 shows the supported drive strength for the single-ended I/O types under designated V_{CCIO} conditions.

Table 8. Output Drive Capability for Ratioed sysIO Standards

Drive Strength (mA)	I/O Type					
	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25	LVCMOS33	LVTTL33
2	YES					
4		YES	YES	YES	YES	YES
6	YES					
8		YES	YES	YES	YES	YES
12			YES	YES	YES	YES
16				YES	YES	YES

DIFFDRIVE
The DIFFDRIVE strength attribute is available for the true LVDS output standard. All true LVDS differential drivers on the top edge is set to 3.5 mA setting. This is not programmable on the MachXO3L/LF device.

Values: 3.5
Default: 3.5

PULLMODE
The PULLMODE option can be enabled or disabled independently for each I/O. When the user selects OPENDRAIN=ON, the PULLMODE for the output standard is default to NONE.

Values: UP, DOWN, NONE, KEEPER
Default: DOWN for LVTTL, and LVCMOS; all others NONE

CLAMP
The CLAMP option can be enabled or disabled independently for each I/O. The available settings on the bottom edge. All other I/O have ON or OFF settings for this attribute.

Values: OFF, ON
Default: OFF

HYSTERESIS
The ratioed input buffers have two input hysteresis settings. The HYSTERESIS option can be used to change the amount of hysteresis for the LVTTL and LVCMOS input and bidirectional I/O standards, except for the LVCMOS12 inputs. The LVCMOS12 inputs do not support HYSTERESIS.

The LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, and LVCMOS10R25 input types do not support HYSTERESIS. The HYSTERESIS option for each of the input pins can be set independently when it is supported for the I/O type.

Values: SMALL, LARGE, NA
Default: SMALL

VREF
The VREF option is enabled for referenced LVMCOS input buffers. The referenced LVMCOS input buffers are specified by choosing the I/O type as LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, or LVCMOS10R25. The default value of NA will apply for all I/O types that do not use a VREF signal.

The VREF will default to external VREF pin for the single-ended LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, or LVCMOS10R25 inputs. The user may enter a VREF_NAME value in the “VREF Location(s)” pop-up window of the Spreadsheet View of the Diamond software. In doing so, the software will present the VREF_NAME as an available value in additional to the I45, I50 and I55 values in the VREF column of the Port Assignments tab of the Diamond Spreadsheet View. A pin location specified by the VREF_NAME value will be used as the VREF driver for that I/O bank. VREF_NAME is only necessary if the user wants to specify a pin to be used as an external VREF pin. Otherwise, the software will automatically assign a pin for the VREF signal.

There is only one VREF pin or internal VREF driver per I/O bank. Only one of the VREF driver settings chosen from I45, I50, I55 or VREF1_LOAD can be used in each I/O bank. This attribute can be set in the software GUI or in the ASCII preference file.

Values: OFF, I45, I50, Values: OFF, I45, I50, I55, VREF_NAME
Software Default: NA
Hardware Default (Erased): OFF

OPENDRAIN
The OPENDRAIN option is available for all LVTTL and LVCMOS output and bidirectional I/O standards. Each sysIO can be assigned independently to be open drain. When the OPENDRAIN attribute is used, the PULLMODE must be NONE and the CLAMP must be OFF.

Values: OFF, ON
Default: OFF

SLEWRATE
Each I/O pin has an individual slew rate control. This allows the designer to specify slew rate control on a pin-by-pin basis for outputs and bidirectional I/O pins. This is not a valid attribute for inputs or true differential outputs.

Values: FAST, SLOW, NA
Default: SLOW

DIFFRESISTOR
The bottom side I/O pins support on-chip differential input termination resistors. The termination resistor is available for both the primary pair and the alternate pair of a sysIO. The values supported are zero (OFF) or 100 Ohm.

Values: OFF, 100
Default: OFF

DIN/DOUT
The DIN/DOUT option is available for each I/O and can be configured independently. An input register is used for the input if the DIN attribute is assigned. Similarly, the software assigns an output register when the DOUT attribute is specified. By default, the software automatically assigns DIN or DOUT to input or output registers if possible.

LOC
This attribute specifies the site location for the component after the mapping process. When attached to multiple components, it indicates that these blocks are to be mapped together in the specified site. It specifies the PIC site for the pad when it is assigned to a pad. The LOC attribute can be attached to components that will end up on an I/O cell, clocks, and internal flip-flops, but it should not be attached to combinational logic that will end up on a logic cell; doing so could fail to generate a locate preference. The LOC attribute overrides register ordering.

Bank VCCIO
This attribute is necessary to verify the valid I/O types for a bank, to determine which input buffer to use, and to set the correct drive strength for the applicable I/O types. Since the I/O bank information is not required at the HDL level, this attribute is available through either the Diamond software's Spreadsheet View or in the ASCII preference file. Values: AUTO, 3.3, 2.5, 1.8, 1.5, 1.2. Default: AUTO.

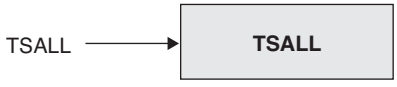
sysIO Primitives

There are many sysIO primitives in the software library. A few are selected to be discussed in this section because some sysIO capabilities can only be utilized through instantiating the primitives in the HDL source code.

Tri-State All (TSALL)
The MachXO3L/LF device supports the TSALL function that is used to enable or disable the tristate control to all the output buffers. The user can choose to assign any general purpose I/O pin to control the TSALL function since there is no dedicated TSALL pin. The TSALL primitive must be instantiated in the source code in order to enable the TSALL function. The input of the primitive can be assigned to an input pin or to an internal signal.

A value of TSALL=1 will tri-state all outputs but the outputs will be under individual OE control when TSALL=0.

Figure 4. TSALL Primitive



Fixed Data Delay (DELAYE)

This primitive supports up to 32 steps of static delay for all sysIO buffers in all banks of a MachXO3L/LF device. Refer to the MachXO3 Family Data Sheet External Switching Characteristics table for delay step values. Although users can choose USER_DEFINED mode to set input delay, this primitive is primarily used by pre-defined source synchronous interfaces as described in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

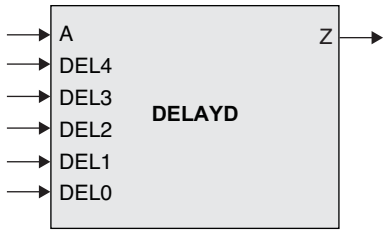
Figure 5. DELAYE Primitive and Associated Attributes

Attribute	Description	Value	Software Default
DEL_MODE	Fixed delay value depending on interface or user-defined delay values	SCLK_ZEROHOLD ECLK_ALIGNED ECLK_CENTERED SCLK_ALIGNED SCLK_CENTERED USER_DEFINED	USER_DEFINED
DEL_VALUE	User-defined value	DELAY0…DELAY31	DELAY0

Dynamic Data Delay (DELAYD)

This primitive supports dynamic delay for the sysIO buffers in the bottom bank (Bank 2) of the MachXO3L/LF device only. The 5-bit inputs can be controlled by user logic to modify the delay during the device operation.

Figure 6. DELAYD Primitive



Design Consideration and Usage

This section summarizes the MachXO3L/LF designs rules and considerations that have been discussed in detail in previous sections. Table 9 lists the miscellaneous I/O features on each side of a MachXO3L/LF device.

sysIO Buffer Features Common to All MachXO3L/LF Devices

1. All banks support true differential inputs.
2. All banks support emulated differential outputs using external resistors and complementary LVCMOS outputs. Emulated differential output buffers are supported on both primary and alternate pairs.
3. All banks have programmable I/O clamps.
4. All banks support weak pull-up, pull-down, and bus-keeper (bus hold latch) settings on each I/O independently.
5. V_{CCIO} voltage levels, together with the selected I/O types, determine the characteristics of an I/O, such as the pull mode, hysteresis, clamp behavior, and drive strength, supported in a bank. Each bank can support 1.2 V inputs regardless of the V_{CCIO} setting of the bank.
6. Each bank supports one V_{CCIO} signal.

sysIO Buffer Rules

1. Only Bank 0 (top side) supports true differential output buffers with programmable drive strengths. Only the primary pair supports true differential output buffers.
2. Only Bank 2 (bottom side) supports internal 100 Ohm differential input terminations.

Table 9. Miscellaneous I/O Features on Each Device Edge

Feature	Top	Bottom	Left	Right
100 Ohm Differential Resister	—	Yes	—	—
Hot Socket	Yes	Yes	Yes	Yes
Clamp[2]	Yes	Yes	Yes	Yes
Weak Pull-up[2]	Yes	Yes	Yes	Yes
Weak Pull-down[1]	Yes	Yes	Yes	Yes
Bus Keeper[2]	Yes	Yes	Yes	Yes
Input Hysteresis[2]	Yes	Yes	Yes	Yes
Slew Rate Control	Yes	Yes	Yes	Yes
Open Drain	Yes	Yes	Yes	Yes

1. Software default setting
2. I/O characteristic under special conditions
   a. HYSTERESIS option is not available for LVCMOS12.
   b. HYSTERESIS option and BUS KEEPER option are not available for referenced input standards.
   c. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting shall be NA, the CLAMP setting shall be OFF, and the UP and KEEPER PULLMODE settings are not supported.
   d. HYSTERESIS and the bus maintenance capabilities are disabled for differential receivers.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
May 2016	1.6	Minor update in Introduction section. Removed specific reference to L version.
		Minor update in Supported sysIO Standards section. Corrected typo in LVDS25 value in Table 2, Supported Output Standards.
		Added Input Reference Voltage section.
		Minor update in sysIO Banking Scheme section. Mentioned MachXO3L/LF 9400.
		Minor update in VCCIO Requirement for I/O Standards section. — Fixed grammatical errors. — Replaced previous table with new Table 5, Mixed Voltage Support for LVCMOS and LVTTL I/O Types. — Corrected reference to Table 6.
		Updated Software sysIO Attributes section. — Added standards to Table 7, Supported I/O Types. — Added footnote 3 and 4. — Added information to Hysteresis section. — Added VREF section.
		Updated Appendix B. sysIO Attributes Using the Spreadsheet View section. Removed reference to VREF in introductory paragraph.
April 2015	1.5	Updated Appendix B. sysIO Attributes Using the Spreadsheet View section. — Removed Figure 8, V_{REF} Name and Location Pop-up Window of the Spreadsheet View. — Removed the V_{REF} Assignment in the Spreadsheet View section.
	1.4	Included MachXO3LF device.
		Updated Input Hysteresis section. Added information.
		Updated Technical Support Assistance section.
February 2015	1.3	Updated the following sections to add MIPI information: — Supported sysIO Standards. Updated Table 1, Supported Input Standards (also added footnote) and Table 2, Supported Output Standards. — sysIO Standards Supported by I/O Banks. Updated Table 4, Differential I/O Standards Supported on Various Sides — Software sysIO Attributes. Updated Table 7, Supported I/O Types.
		Updated the VCCIO Requirement for I/O Standards section. — Updated Table , Mixed Voltage Support for LVCMOS and LVTTL I/O Types. Revised information for Inputs and removed footnotes on over drive and under drive conditions. — Removed the VCCIO for Same Bank LVCMOS/LVTTL Input/Output Requirements table.
		Updated Emulated Differential Outputs section. Added MIPI to examples of output standards.
August 2014	1.2	Updated Table 10-6, Mixed Voltage Support for LVCMOS and LVTTL I/O Types. Revised data on V_{CCIO} 1.2 V.

Date	Version	Change Summary
May 2014	01.1	Product name/trademark adjustment.
		Updated Table 10-1, Supported Input Standards. Removed LVTTL / LVCMOS Differential and added input standards.
		Updated Table 10-2, Supported Output Standards. Removed LVCMOS Differential output standards.
		Updated Table 10-4, Differential I/O Standards Supported on Various Sides. Removed LVCMOS input and output standards.
		Added Table 10-6, Mixed Voltage Support for LVCMOS and LVTTL I/O Types and Table 10-7, Mixed Voltage Support for Differential Input Standards.
		Updated Table 10-8, Supported I/O Types. Removed LVCMOS differential standards.
February 2014	01.0	Initial release.

Appendix A. sysIO HDL Attributes

The sysIO attributes can be used directly in the HDL source codes. This section provides a list of sysIO attributes supported by the MachXO3L/LF PLD family. The correct syntax and examples for the Synplify® synthesis tool are provided here for reference.

Attributes in VHDL Language

Syntax

Table 10. VHDL Attribute Syntax

Attribute	Syntax
IO_TYPE	attribute IO_TYPE: string; attribute IO_TYPE of Pinname: signal is “IO_TYPE Value”;
DRIVE	attribute DRIVE: string; attribute DRIVE of Pinname: signal is “Drive Value”;
DIFFDRIVE	attribute DRIVE: string; attribute DRIVE of Pinname: signal is “Diffdrive Value”;
DIFFRESISTOR	attribute DIFFRESISTOR: string; attribute DIFFRESISTOR of Pinname: signal is “DIFFRESISTOR Value”;
CLAMP	attribute CLAMP: string; attribute CLAMP of Pinname: signal is “Clamp Value”;
HYSTERESIS	attribute HYSTERESIS: string; attribute HYSTERESIS OF Pinname: signal is “Hysteresis Value”;
VREF	NA
PULLMODE	attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is “Pullmode Value”;
OPENDRAIN	attribute OPENDRAIN: string; attribute OPENDRAIN of Pinname: signal is “OpenDrain Value”;
SLOWSLEW	attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is “Slewrate Value”;
DIN	attribute DIN: string; attribute DIN of Pinname: signal is “value “;
DOUT	attribute DOUT: string; attribute DOUT of Pinname: signal is “value “;
LOC	attribute LOC: string; attribute LOC of Pinname: signal is “Pin locations”;
BANK VCCIO	NA

Examples

IO_TYPE

```
 --***Attribute Declaration***
ATTRIBUTE IO_TYPE: string;
 --***IO_TYPE assignment for I/O Pin***
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE IO_TYPE OF portD: SIGNAL IS "LVDS25";
```

DRIVE

```
--***Attribute Declaration***
ATTRIBUTE DRIVE: string;
--***DRIVE assignment for I/O Pin***
ATTRIBUTE DRIVE OF portB: SIGNAL IS “8”;
```

DIFFDRIVE

```
 --***Attribute Declaration***
ATTRIBUTE DIFFDRIVE: string;
--*** DIFFDRIVE assignment for I/O Pin***
ATTRIBUTE DIFFDRIVE OF portD: SIGNAL IS “2.0”;
```

DIFFRESISTOR

```
 --***Attribute Declaration***
ATTRIBUTE DIFFRESISTOR: string;
--*** DIFFRESISTOR assignment for I/O Pin***
ATTRIBUTE DIFFRESISTOR OF portD: SIGNAL IS "100";
```

CLAMP

```
--***Attribute Declaration***
ATTRIBUTE CLAMP: string;
--*** CLAMP assignment for I/O Pin***
ATTRIBUTE CLAMP OF portA: SIGNAL IS “PCI33”;
```

HYSTERESIS

```
--***Attribute Declaration***
ATTRIBUTE HYSTERESIS: string;
--*** HYSTERESIS assignment for Input Pin***
ATTRIBUTE HYSTERESIS OF portA: SIGNAL IS " LARGE ";
```

PULLMODE

```
--***Attribute Declaration***
ATTRIBUTE PULLMODE : string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PULLMODE OF portA: SIGNAL IS “DOWN”;
ATTRIBUTE PULLMODE OF portB: SIGNAL IS “UP”;
```

OPENDRAIN

```
--***Attribute Declaration***
ATTRIBUTE OPENDRAIN: string;
--***Open Drain assignment for I/O Pin***
ATTRIBUTE OPENDRAIN OF portB: SIGNAL IS “ON”;
```

SLEWRATE

```
 --***Attribute Declaration***
ATTRIBUTE SLEWRATE : string;
--*** SLEWRATE assignment for I/O Pin***
ATTRIBUTE SLEWRATE OF portB: SIGNAL IS “FAST”;
```

DIN/DOUT

```
--***Attribute Declaration***
ATTRIBUTE din : string; ATTRIBUTE dout : string;
--*** din/dout assignment for I/O Pin***
ATTRIBUTE din OF input_vector: SIGNAL IS “TRUE “;
ATTRIBUTE dout OF output_vector: SIGNAL IS “TRUE “;
```

LOC

```
--***Attribute Declaration***
ATTRIBUTE LOC : string;
 --*** LOC assignment for I/O Pin***
ATTRIBUTE LOC OF input_vector: SIGNAL IS “E3,B3,C3 “;
```

Attributes in Verilog Language

Syntax

Table 11. Verilog Attribute Syntax

Attribute	Syntax
IO_TYPE	PinType PinName /* synthesis IO_Type=”IO_Type Value”*/;
DRIVE	PinType PinName /* synthesis DRIVE=”Drive Value”*/;
DIFFDRIVE	PinType PinName /* synthesis DIFFDRIVE =” DIFFDRIVE Value”*/;
DIFFRESISTOR	PinType PinName /* synthesis DIFFRESISTOR =” DIFFRESISTOR Value”*/;
CLAMP	PinType PinName /* synthesis CLAMP =” Clamp Value”*/;
HYSTERESIS	PinType PinName /*synthesis HYSTERESIS = “Hysteresis Value” */;
VREF	N/A
PULLMODE	PinType PinName /* synthesis PULLMODE=”Pullmode Value”*/;
OPENDRAIN	PinType PinName /* synthesis OPENDRAIN =”OpenDrain Value”*/;
SLOWSLEW	PinType PinName /* synthesis SLEWRATE=”Slewrate Value”*/;
DIN	PinType PinName /* synthesis DIN= “value” */;
DOUT	PinType PinName /* synthesis DOUT= “value” */;
LOC	PinType PinName /* synthesis LOC=”pin_locations “*/;
Bank VCCIO	N/A

Examples

//IO_TYPE, PULLMODE, SLEWRATE and DRIVE assignment

```
output portB /*synthesis IO_TYPE=”LVCMOS33”
PULLMODE =”UP” SLEWRATE =”FAST” DRIVE =”20”*/;
output portC /*synthesis IO_TYPE=”LVDS25” */;
```

//DIFFDRIVE

```
output portD /* synthesis IO_TYPE="LVDS25" DIFFDRIVE="2.0"*/;
```

//DIFFRESISTOR

```
output [4:0] portA /* synthesis IO_TYPE="LVDS25" DIFFRESISTOR ="100"*/;
```

//CLAMP

```
output portA /*synthesis IO_TYPE=”LVCMOS33” CLAMP =”ON” */;
```

//HYSTERESIS

```
input mypin /* synthesis HYSTERESIS = “LARGE” */;
```

//OPENDRAIN

```
output portA /*synthesis OPENDRAIN =”ON”*/;
```

// DIN Place the flip-flops near the load input

```
 input load /* synthesis din=”” TRUE */;
```

// DOUT Place the flip-flops near the outload output

```
 output outload /* synthesis dout=”TRUE” */;
```

//LOC pin location

```
input [3:0] DATA0 /* synthesis loc=”E3,B1,F3”*/;
```

//LOC Register pin location

```
reg data_in_ch1_buf_reg3 /* synthesis loc=”R10C16” */;
```

//LOC Vectored internal bus

```
reg [3:0] data_in_ch1_reg /*synthesis loc =”R10C16,R10C15,R10C14,R10C9” */;
```

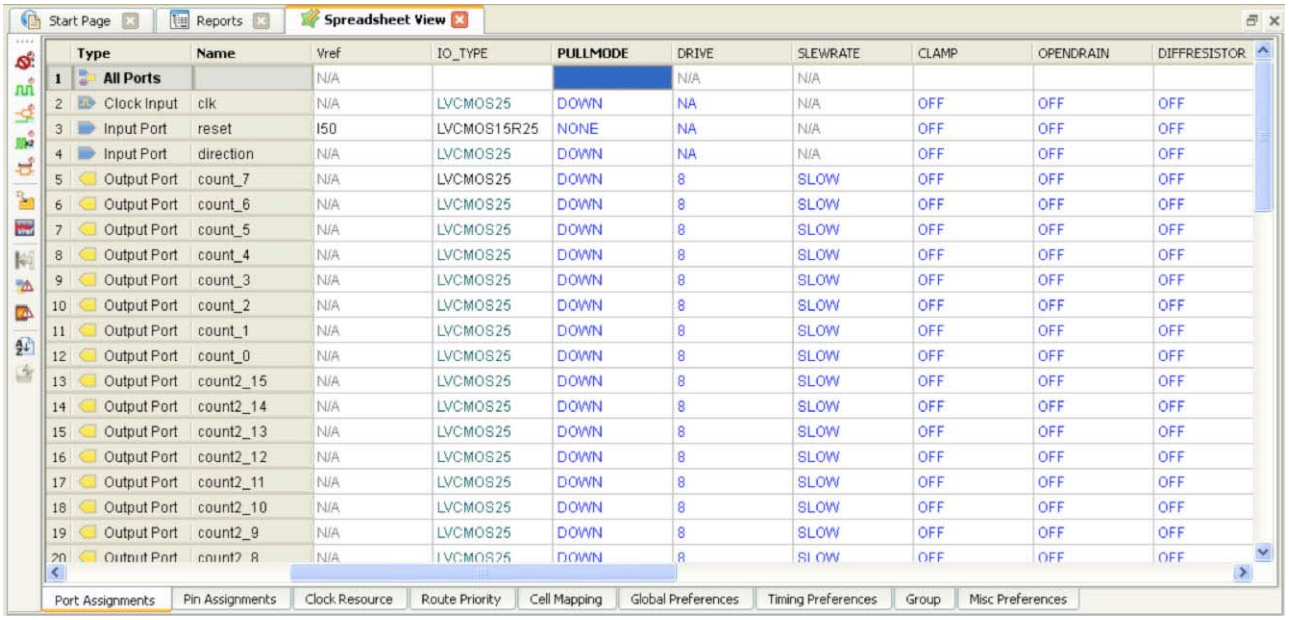
Appendix B. sysIO Attributes Using the Spreadsheet View

The sysIO buffer attributes can be assigned using the Spreadsheet View available in the Diamond design tool. The attributes that are not available as HDL attributes, such as Bank VCCIO, are available in the Spreadsheet View GUI.

The Port Assignment tab lists all the ports in a design and all the available sysIO attributes as preferences. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when a particular IO_TYPE is chosen, the columns for the DRIVE, PULL-MODE, SLEW-RATE and other attributes will list the valid combinations for that IO_TYPE. Pin locations can be locked using the Pin column of the Port Assignment tab. Right-clicking on a cell will list all the available pin locations. The Spreadsheet View can run a DRC check to check for incorrect sysIO attribute assignments.

All the preferences assigned using the Spreadsheet View are written into the logical preference file (.lpf).

Figure 7. Port Assignment Tab of Spreadsheet View

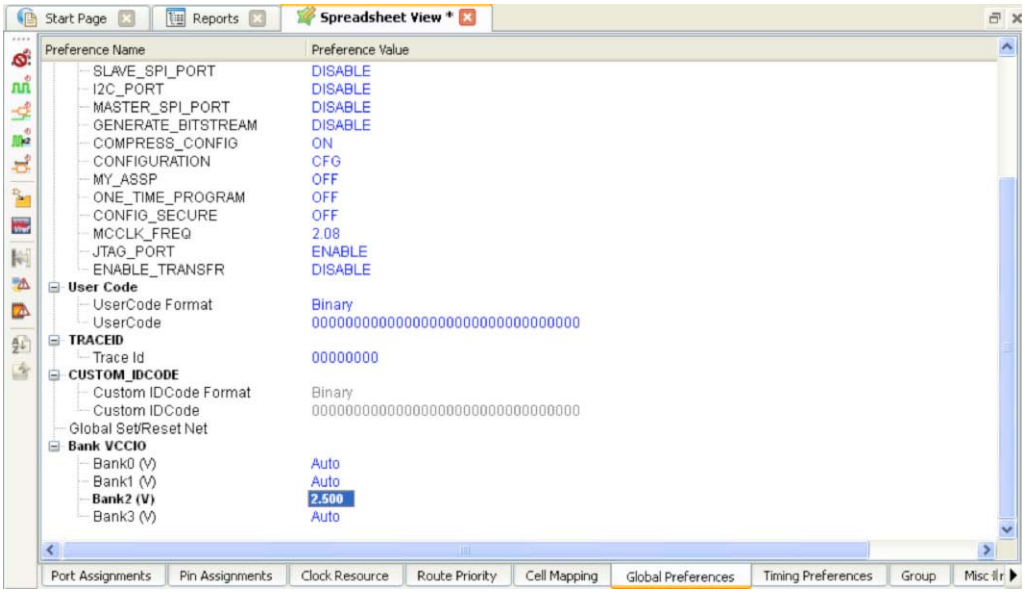


	Type	Name	Vref	IO_TYPE	PULLMODE	DRIVE	SLEWRATE	CLAMP	OPENDRAIN	DIFFRESISTOR
1	All Ports		N/A			N/A	N/A			
2	Clock Input	clk	N/A	LVCMOS25	DOWN	NA	N/A	OFF	OFF	OFF
3	Input Port	reset	I50	LVCMOS15R25	NONE	NA	N/A	OFF	OFF	OFF
4	Input Port	direction	N/A	LVCMOS25	DOWN	NA	N/A	OFF	OFF	OFF
5	Output Port	count_7	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
6	Output Port	count_6	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
7	Output Port	count_5	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
8	Output Port	count_4	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
9	Output Port	count_3	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
10	Output Port	count_2	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
11	Output Port	count_1	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
12	Output Port	count_0	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
13	Output Port	count2_15	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
14	Output Port	count2_14	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
15	Output Port	count2_13	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
16	Output Port	count2_12	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
17	Output Port	count2_11	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
18	Output Port	count2_10	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
19	Output Port	count2_9	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
20	Output Port	count2_8	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF

Bank V_{CCIO} Setting in the Spreadsheet View

Bank VCCIO is editable in the Global Preference tab of the Spreadsheet View. The value of the Bank VCCIO can be chosen by the users to determine the value of VCCIO of a specific bank.

Figure 8. Bank VCCIO in Global Preference Tab



Appendix C. sysIO Attributes Using Preference File (ASCII File)

Designers can enter sysIO attributes directly in the preference (.lpf) file as sysIO buffer preferences. The LPF file is a post-synthesis FPGA constraint file that stores logical preferences that have been created or modified in the Spreadsheet View or directly in a text editor. It also contains logical preferences originating in the HDL source. Modifying the Spreadsheet View in the Diamond software will automatically update the content of the LPF file and vice versa. The settings in the Spreadsheet View are reflected in the preference file once they are saved. Details of the supported preferences and their corresponding syntax can be found in the Diamond Help System.