

# Lattice Diamond Tutorial (Basic Hello Word)

# Topic

- Download Lattice Diamond Software and request for the license
- Use Lattice Diamond Software for writing Verilog code
- Use Lattice Diamond Software for signal assignments
- Use Lattice Diamond Software for generate bitstream
- Use Lattice Programmer to program MachXO2 FPGA chip

# Lattice Diamond Software

# Download Lattice Diamond and request a license



A Lattice account is required to download software, documentations or request licenses

Download Lattice Diamond

<http://www.latticesemi.com/en/Products/DesignSoftwareAndIP/FPGAandLDS/LatticeDiamond.aspx>

Request a license

<http://www.latticesemi.com/en/Support/Licensing/DiamondAndiCEcube2SoftwareLicensing/DiamondFree.aspx>

Quick Reference		Technical Resources	Information Resources	Downloads		
<a href="#">Data Sheet</a>		<a href="#">Known Issues</a>	<a href="#">Product Brochure</a>	Downloadable Software		
<a href="#">Application Note</a>		<a href="#">Product Change Notification</a>	<a href="#">Release Notes</a>			
<a href="#">Installation Guides</a>			<a href="#">Tutorials</a>			
<a href="#">User Manual</a>			<a href="#">Help</a>			
 	TITLE	NUMBER	VERSION	DATE	FORMAT	
<input type="checkbox"/>	<a href="#">Diamond 3.10 64-bit Encryption Pack for Linux</a>		3.10	10/10/2017		
<input type="checkbox"/>	<a href="#">Diamond 3.10 64-bit Encryption Pack for Windows</a>		3.10	10/10/2017		
<input type="checkbox"/>	<a href="#">Diamond 3.10 64-bit for Linux</a>		3.10	10/10/2017	RPM	
<input type="checkbox"/>	<a href="#">Diamond 3.10 64-bit for Windows</a>		3.10	10/10/2017	ZIP	

Software License Request Form

**Note:** The license file will be sent to the web account email address: [tthanhpdx.edu](mailto:tthanhpdx.edu)

Host NIC (physical address) \*

☐ I verify that I am not an employee of Cadence Design Systems, Mentor Graphics Corp

[Generate License](#)

# Get your MAC address

```
Command Prompt

Microsoft Windows [Version 10.0.16299.125]
(c) 2017 Microsoft Corporation. All rights reserved.

C:\Users\Thanh>ipconfig /all
```

```
Command Prompt

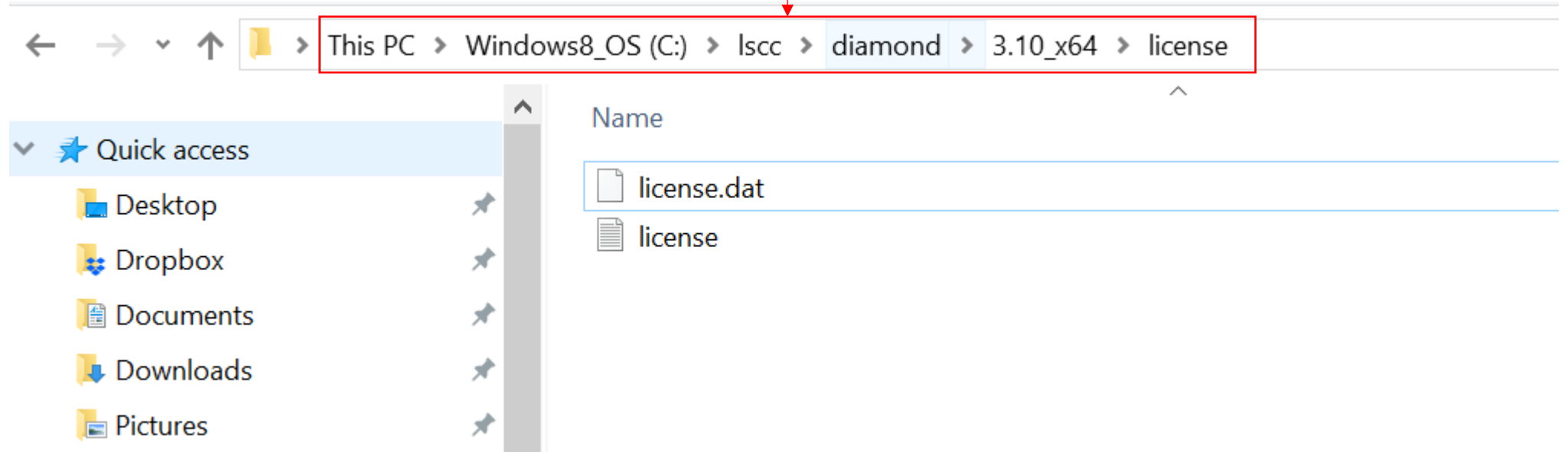
Wireless LAN adapter Wi-Fi:

    Connection-specific DNS Suffix  . : pdx.edu
    Description . . . . . : Broadcom 802.11n Network Adapter
    Physical Address. . . . . : 38-B1-DB-D1-7A-BD
    DHCP Enabled. . . . . : Yes
    Autoconfiguration Enabled . . . . : Yes
    Link-local IPv6 Address . . . . . : fe80::d8a1:a67b:2f07:87ee%5(Preferred)
    IPv4 Address. . . . . : 10.200.122.10(Preferred)
    Subnet Mask . . . . . : 255.255.240.0
    Lease Obtained. . . . . : Wednesday, December 13, 2017 12:28:58 PM
    Lease Expires . . . . . : Friday, December 15, 2017 12:29:01 PM
    Default Gateway . . . . . : 10.200.112.1
    DHCP Server . . . . . : 131.252.100.40
    DHCPv6 IAID . . . . . : 389591515
    DHCPv6 Client DUID. . . . . : 00-01-00-01-1C-2C-CC-E0-68-F7-28-52-05-20

    DNS Servers . . . . . : 131.252.120.128
                           131.252.111.20
    NetBIOS over Tcpip. . . . . : Enabled
```

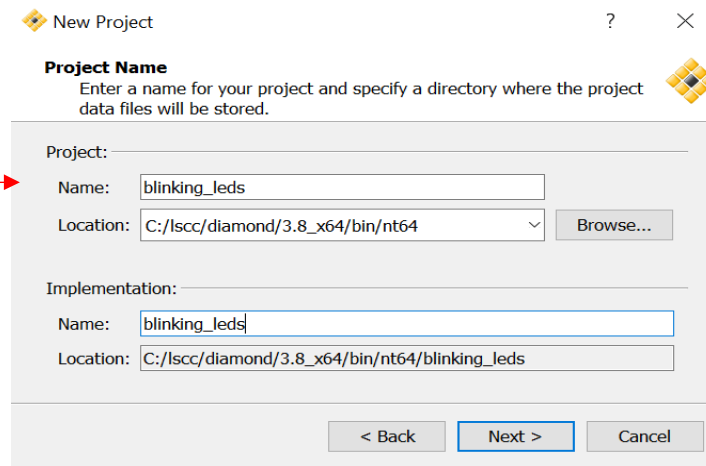
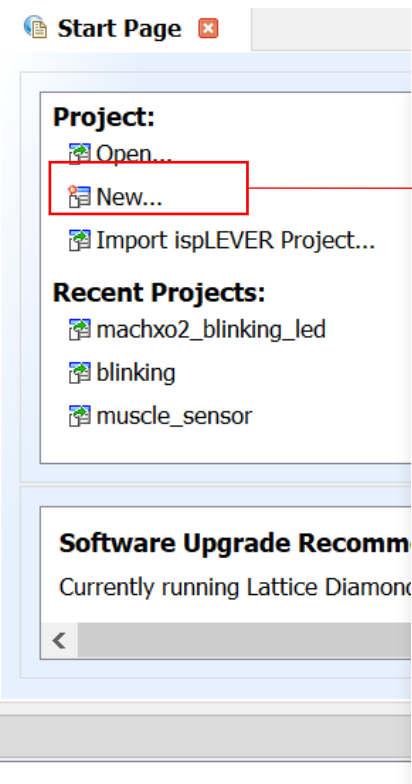
# Activate Lattice Diamond With The License

Installation path

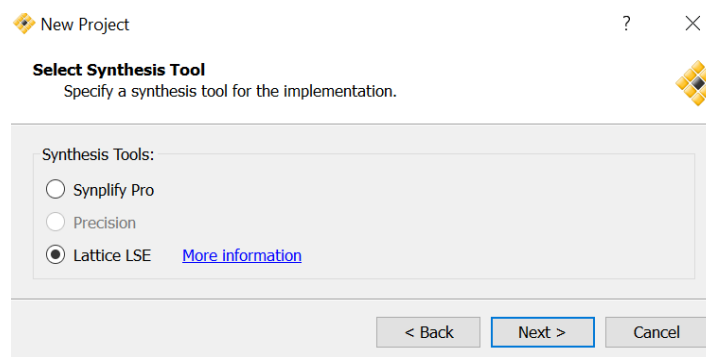
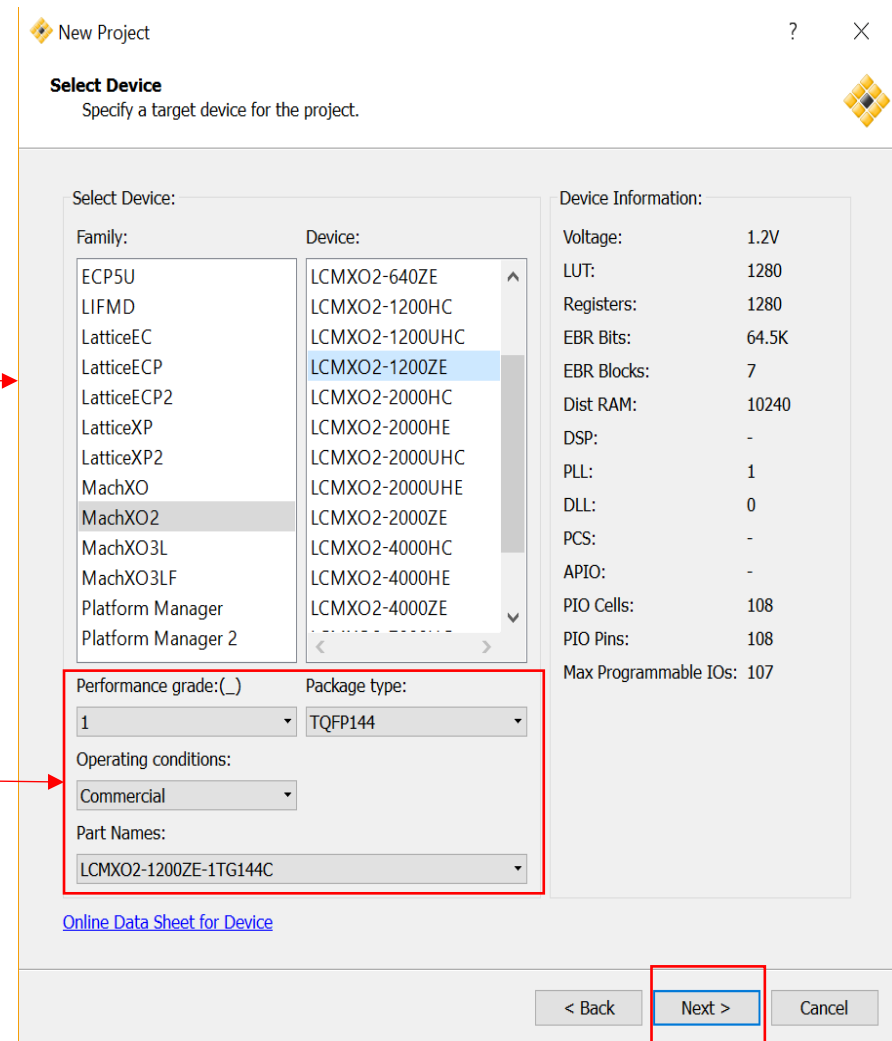


# Hello World With MachXO2 Breakout Board

# Create Working Directory

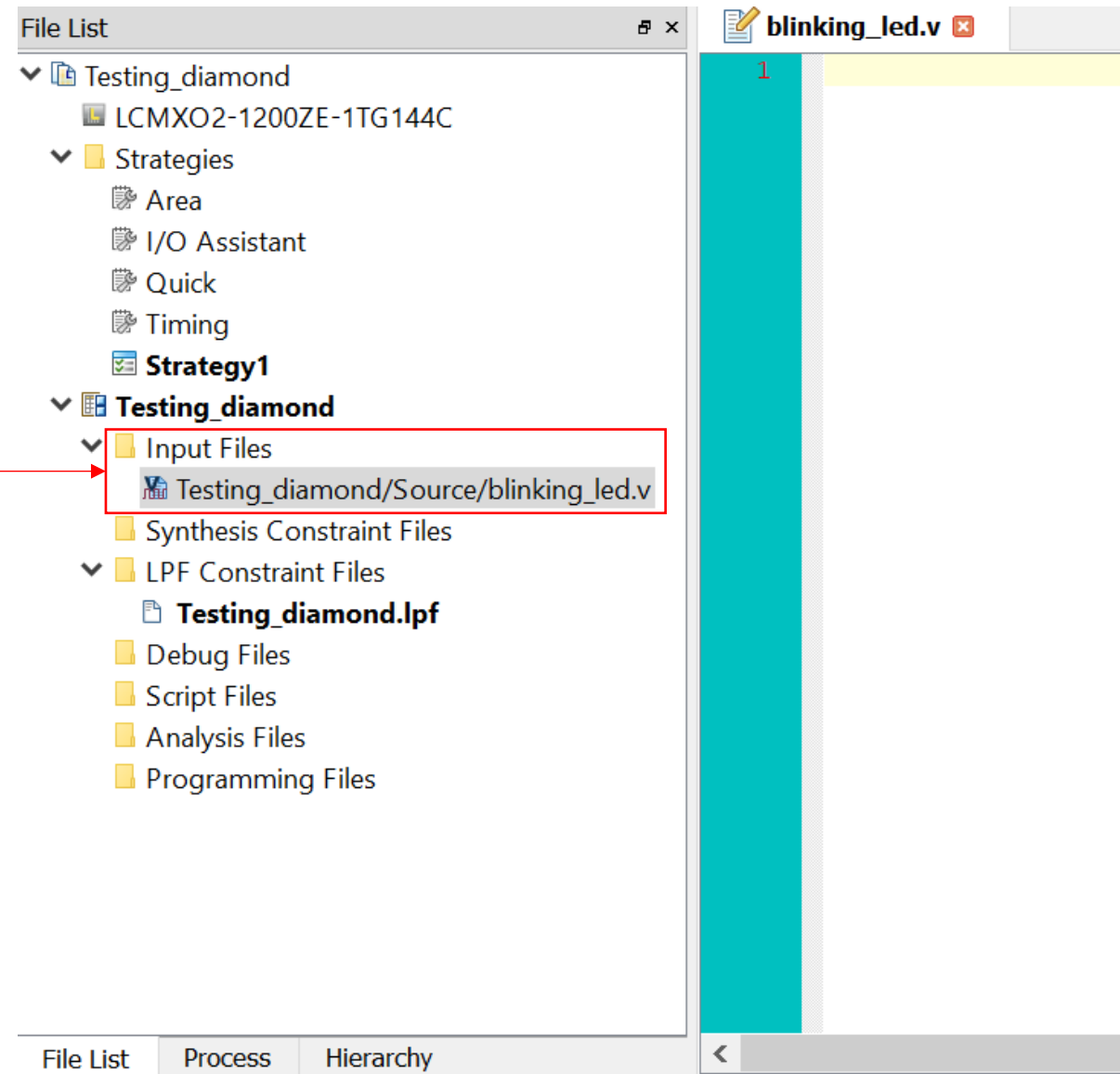
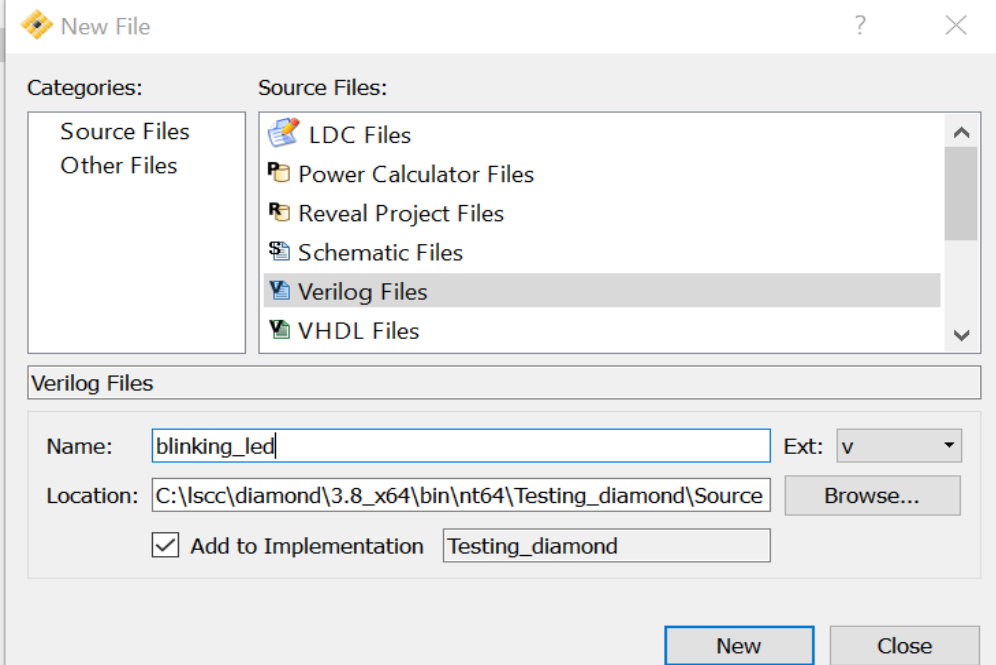
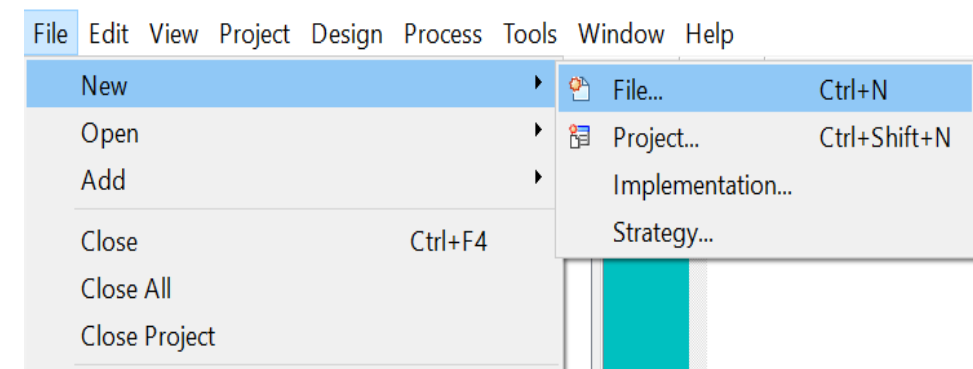


Found these info on  
Lattice's website





# Adding Verilog files

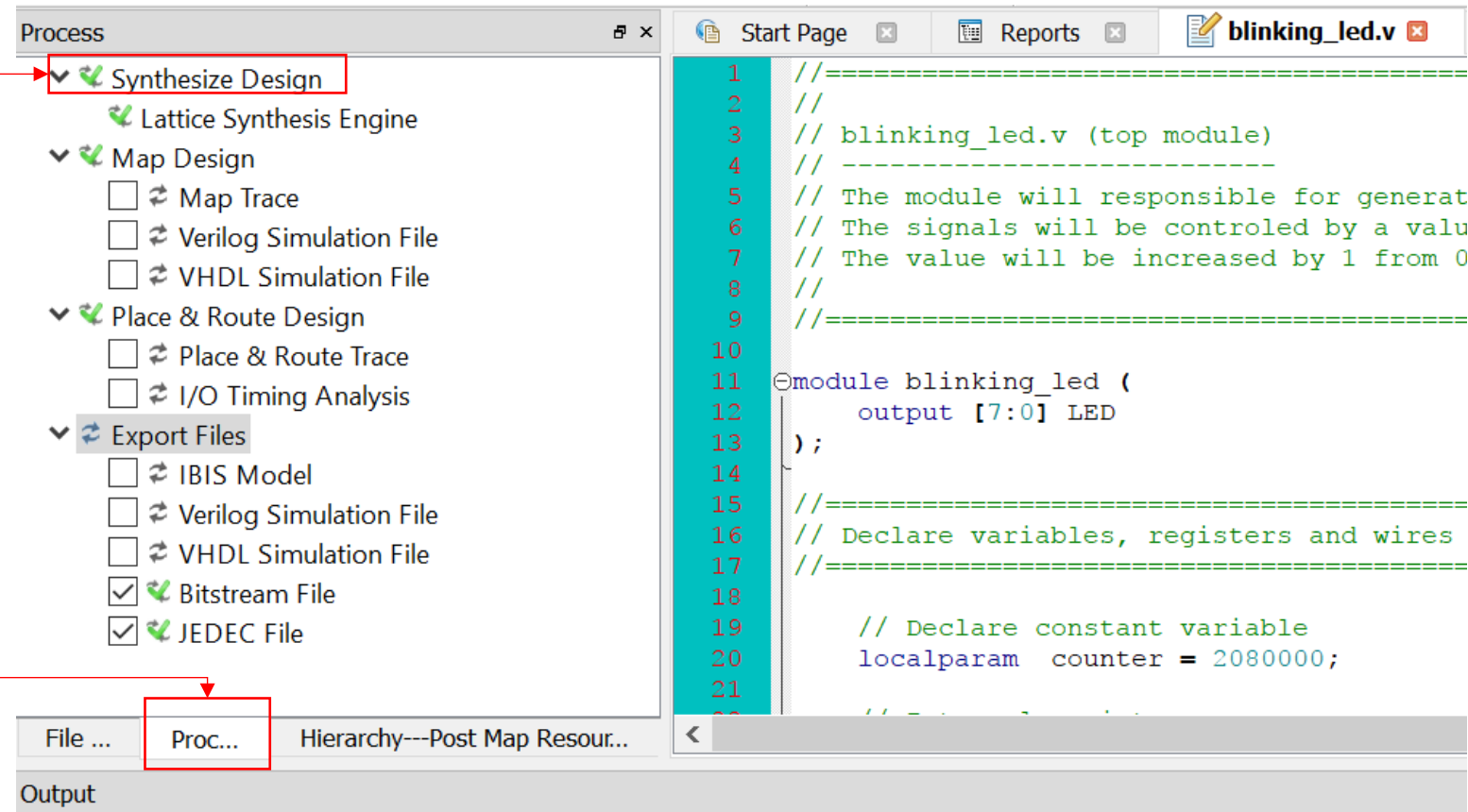


# Writing Verilog Code And Program MachXO2 FPGA Chip

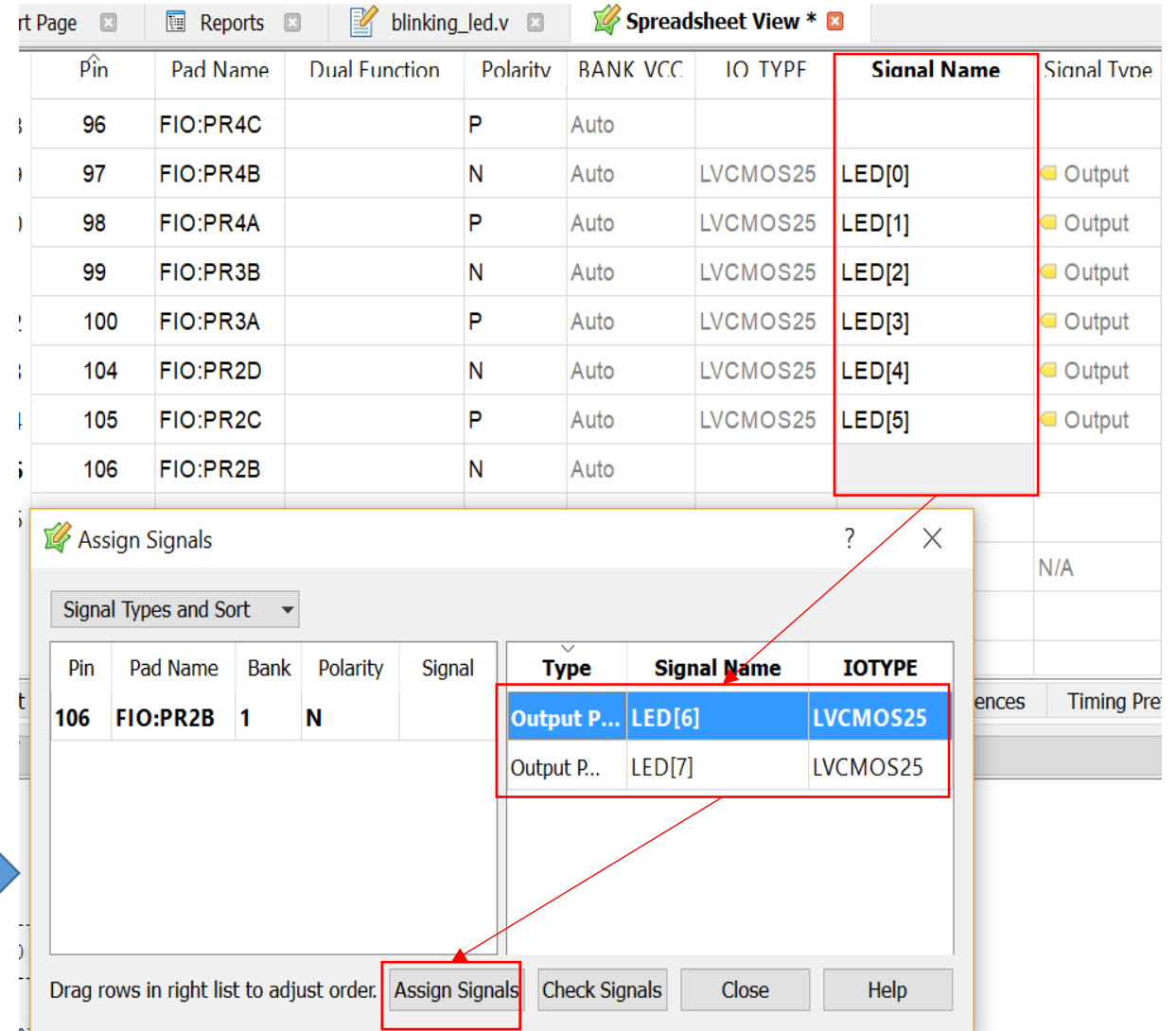
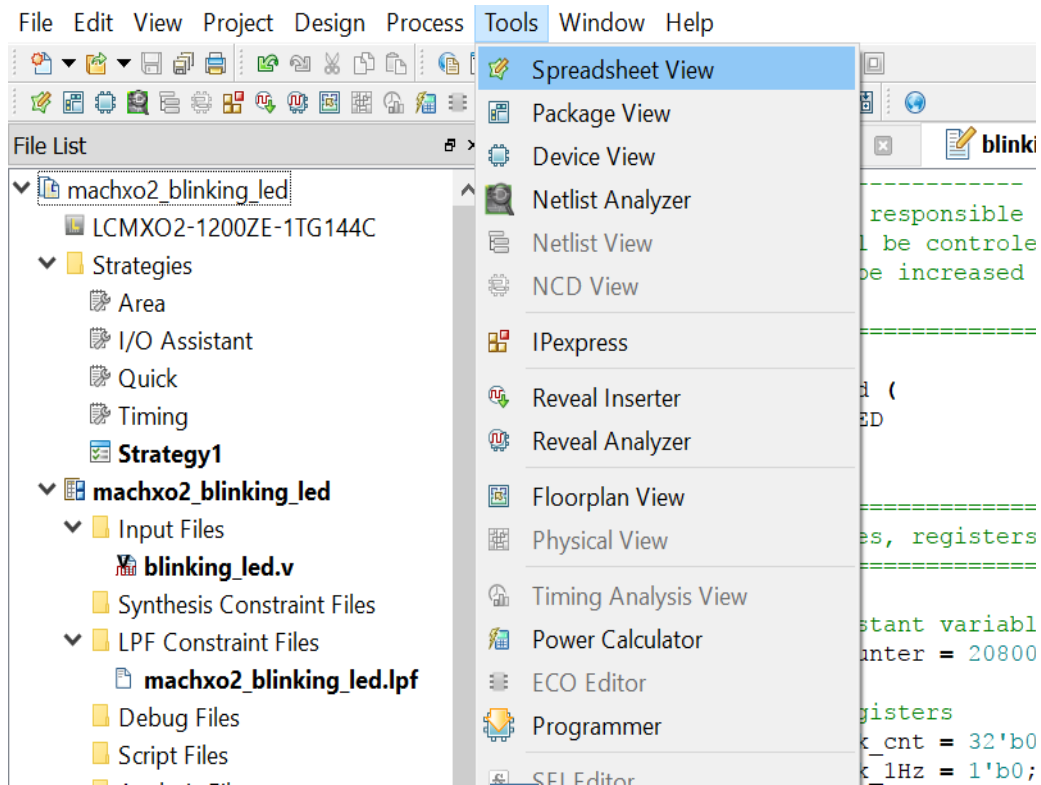
# Run Synthesizer

Double  
Click (2)

Click (1)

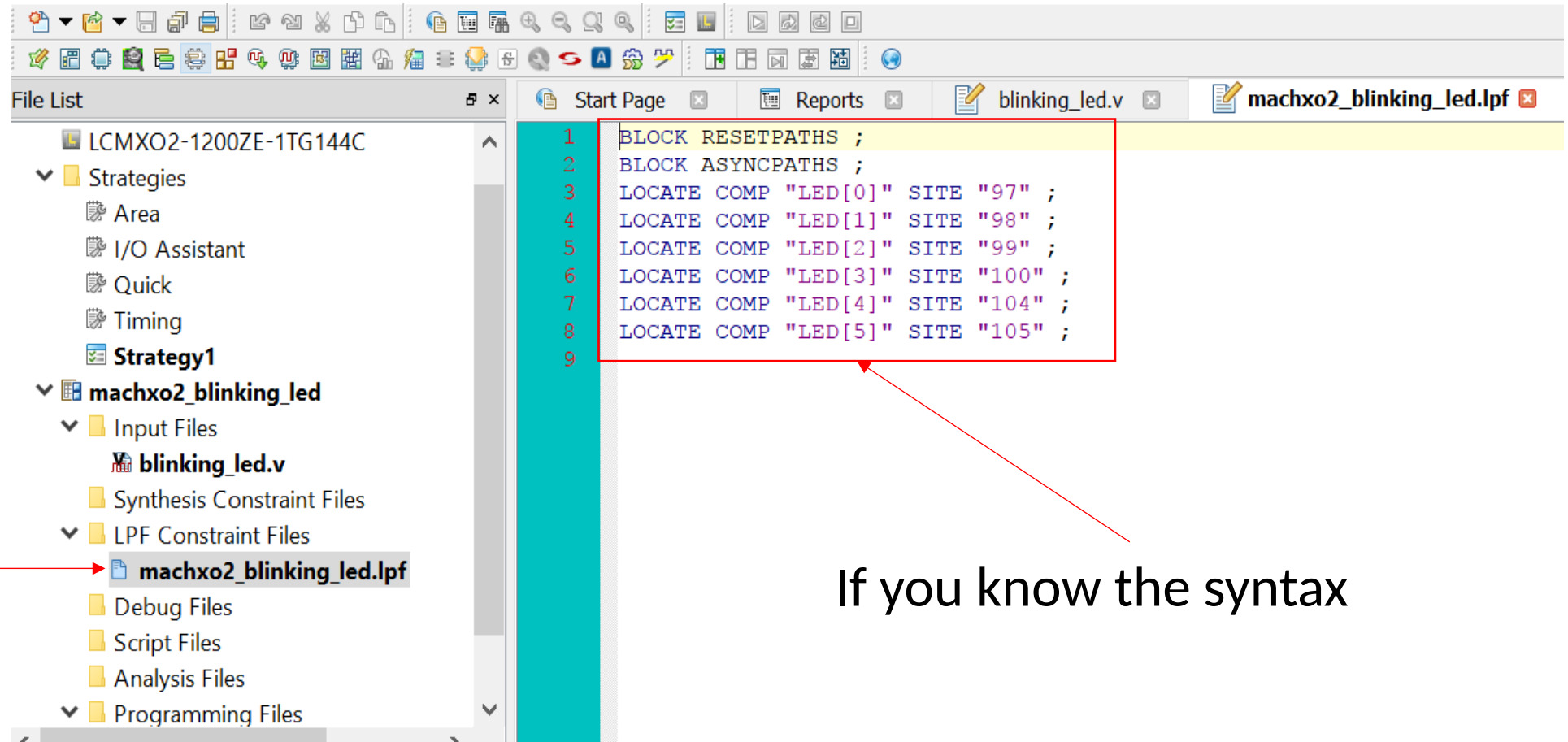


# Signal assignments (Pin assignments – Opt 1)



# Signal assignments (Pin assignments – Opt 2)

Double click



If you know the syntax

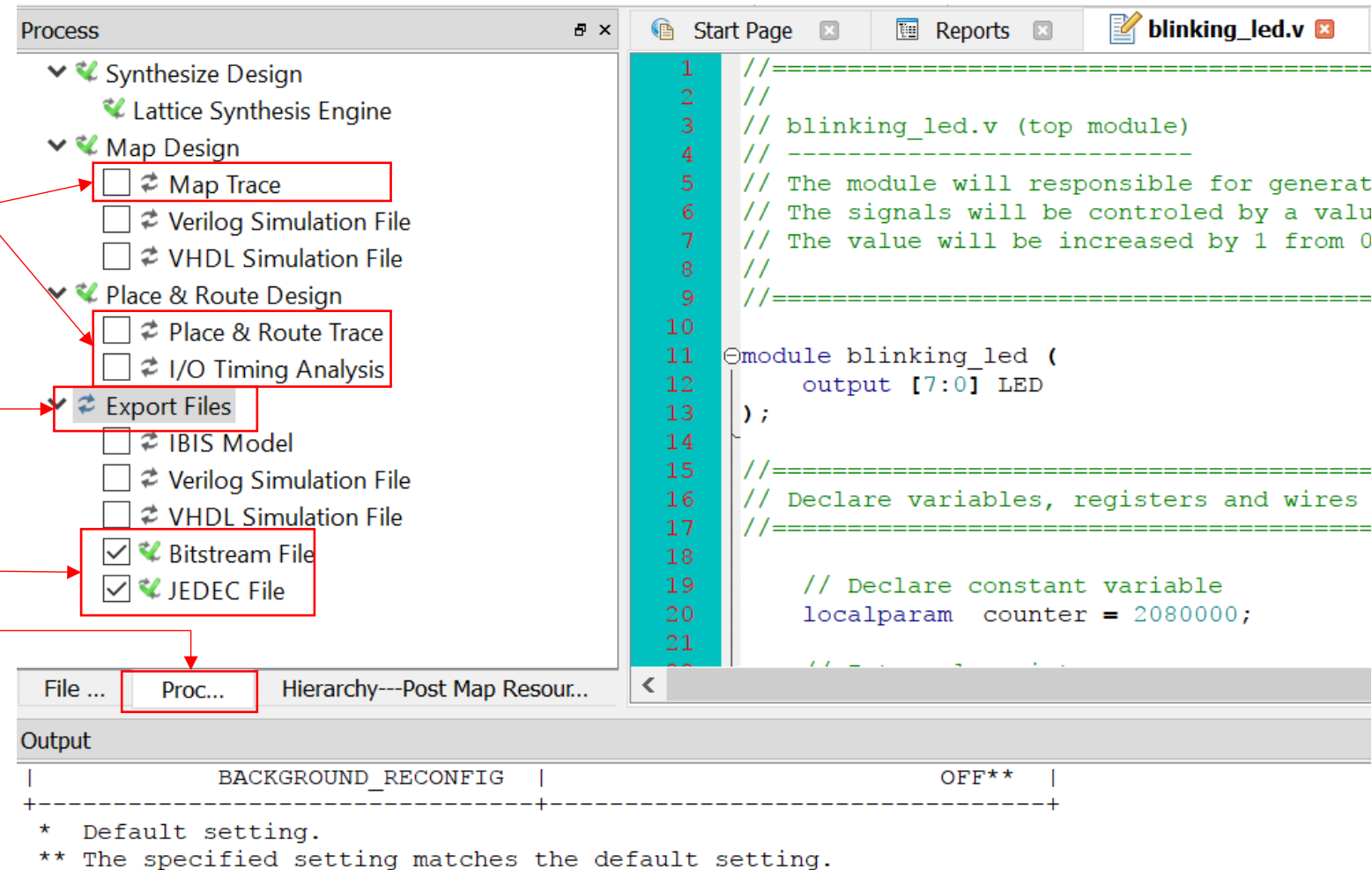
# Generating a Bitstream and a JEDEC file

Check if you want to look at the report

Double Click (3)

Check (2)

Click (1)



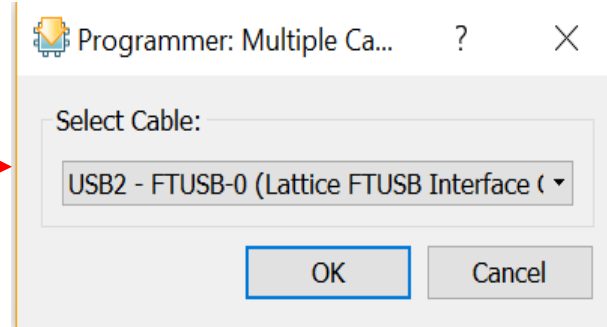
```
Creating bit map...  
Bitstream Status: Final          Version 1.94.  
Saving bit stream in "machxo2_blinking_led_machxo2_blinking_led.jed"
```

Bitstream and JEDEC are generated

# Program MachXO2 FPGA Chip



If the software can't recognize the connected device



Start Page Programmer - machxo2\_blinking\_led.xcf

Enable	Status	Device Family	Device	Operation
1	<input checked="" type="checkbox"/>	MachXO2	LCMXO2-1200ZE	FLASH Erase,Program,Verify

Cable and I/O Settings

Cable Settings

Detect Cable

Cable: HW-USB2-2

Port: FTUSB-0

Custom port:

Programming Speed Settings

☒ Use default Clock Divider

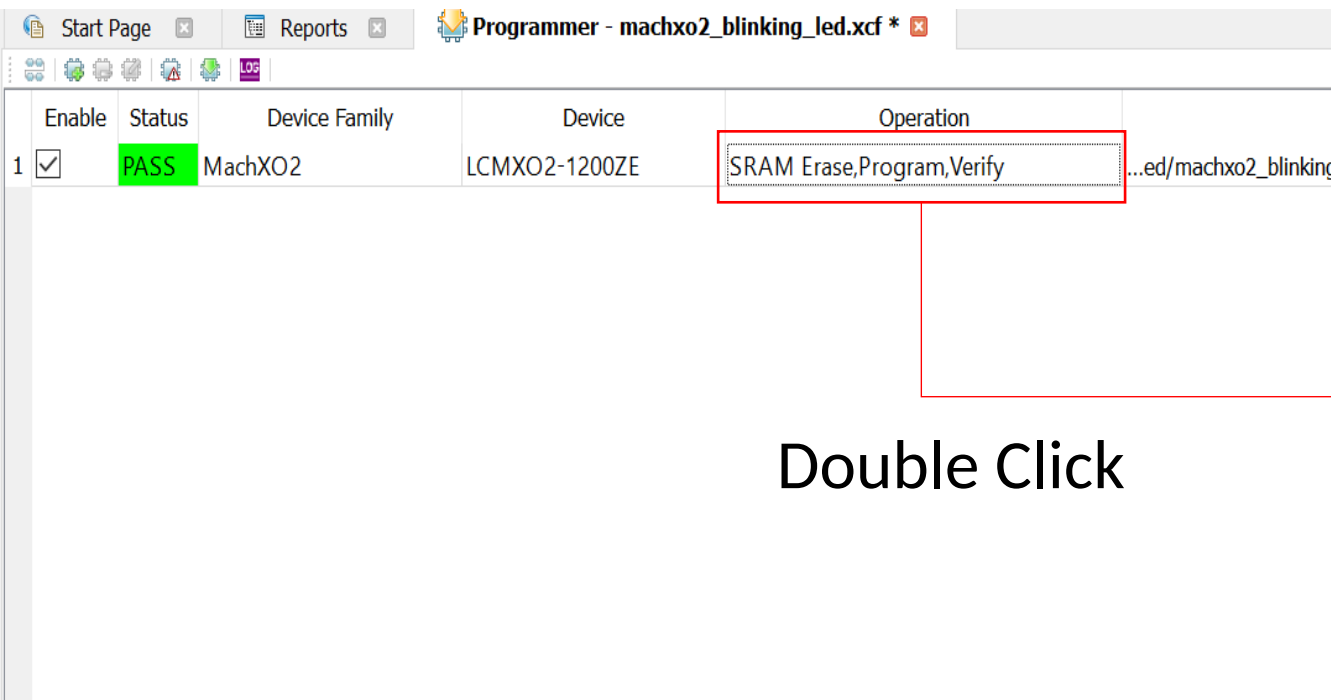
☐ Use custom Clock Divider

TCK Divider Settir 1

I/O Settings

Make sure that info of the device and type of operation are correct

# Programming Flash



Enable	Status	Device Family	Device	Operation
1	PASS	MachXO2	LCMXO2-1200ZE	SRAM Erase,Program,Verify

Double Click

MachXO2 - LCMXO2-1200ZE - Device Pro...

General Device Information

Device Operation

Access mode: Flash Programming Mode

Operation: FLASH Erase,Program,Verify

Programming Options

Programming file: king\_led\_machxo2\_blinking\_led.jed

Device Options

☐ Reinitialize part on program error

OK Cancel



# Programming SRAM

Start Page Reports Programmer - machxo2\_blinking\_led.xcf \*

Enable	Status	Device Family	Device	Operation	
1	PASS	MachXO2	LCMXO2-1200ZE	SRAM Erase,Program,Verify	...ed/machxo2_blinking

Double Click

MachXO2 - LCMXO2-1200ZE - Device Pro...

General Device Information

Device Operation

Access mode: Static RAM Cell Mode

Operation: SRAM Erase,Program,Verify

Programming Options

Programming file: king\_led\_machxo2\_blinking\_led.bit

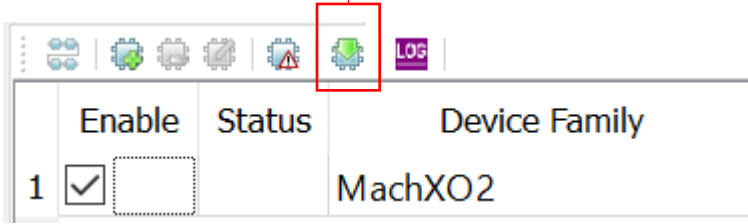
Device Options

☐ Reinitialize part on program error

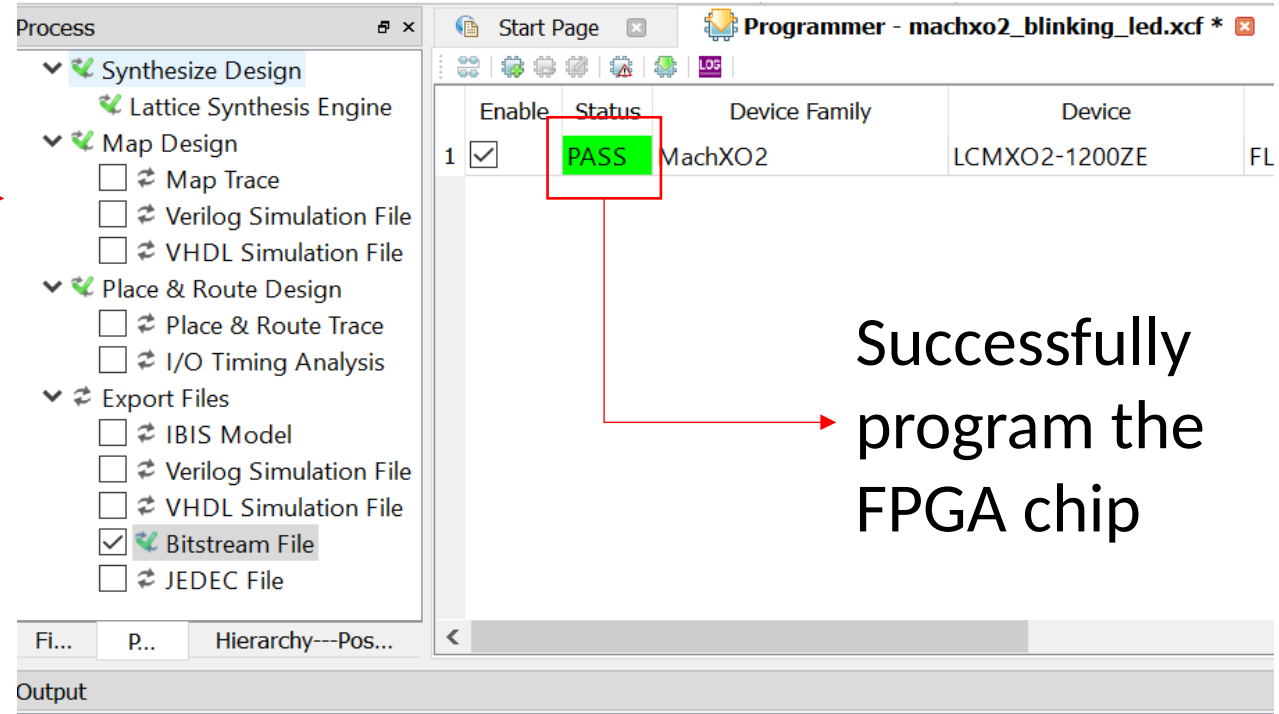
OK Cancel

# Program MachXO2 FPGA Chip

Click to program



	Enable	Status	Device Family
1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	MachXO2



The 'Process' window shows the following steps:

- ✓ Synthesize Design
  - ✓ Lattice Synthesis Engine
- ✓ Map Design
  - ☐ Map Trace
  - ☐ Verilog Simulation File
  - ☐ VHDL Simulation File
- ✓ Place & Route Design
  - ☐ Place & Route Trace
  - ☐ I/O Timing Analysis
- ✓ Export Files
  - ☐ IBIS Model
  - ☐ Verilog Simulation File
  - ☐ VHDL Simulation File
  - ☒ Bitstream File
  - ☐ JEDEC File

The 'Programmer' window shows the following table:

Enable	Status	Device Family	Device	FL
1	<input checked="" type="checkbox"/>	MachXO2	LCMXO2-1200ZE	FL

The 'Output' window shows the following log:

```
Starting: "pgr_program run"

INFO - Check configuration setup: Start.

INFO - JTAG Chain Verification. No Errors.

INFO - Check configuration setup: Successful.

INFO - Device1 LCMXO2-1200ZE: FLASH Erase,Program,Verify

INFO - Operation Done. No errors.

INFO - Elapsed time: 00 min : 14 sec

INFO - Operation: successful.
```

Successfully  
program the  
FPGA chip