33 PROCESSING OF INTEGRATED CIRCUITS

Review Questions

33.1 What is an integrated circuit?

Answer. An integrated circuit is a collection of electronic devices (e.g., transistors, diodes, resistors) that have been fabricated and electrically intraconnected onto the surface of a small flat chip of semiconductor material.

33.2 What is the most important semiconductor material?

Answer. The most important semiconductor material is silicon; others include germanium and gallium arsenide.

33.3 Describe the planar process.

Answer. The planar process refers to the fabrication of an IC chip by a sequence of layering processes - adding, altering, and removing layers to create the devices and their intraconnections on the IC chip.

33.4 What are the three major stages in the production of silicon-based integrated circuits?

Answer. The three stages are (1) silicon processing, to produce very pure silicon and shape it into wafers; (2) IC fabrication, in which layers are added, altered, and removed in selected regions to form electronic devices on the face of the wafer; and (3) IC packaging, in which the wafers are tested, cut into chips, and the chips are encapsulated in a package.

33.5 What is a clean room and explain the classification system by which clean rooms are rated?

Answer. A clean room is a room or rooms where the air is purified to reduce airborne particles. The U.S. classification system indicates the quantity of particles of size 0.5 microns or greater per cubic foot of air. For example, a class 100 clean room contains 100 or fewer particles of size 0.5 microns per cubic foot. The SI (metric) classification system indicates the quantity of particles of size 0.5 microns or greater per cubic meter of air.

33.6 What are some significant sources of contaminants in IC processing?

Answer. Sources of contaminants include humans (bacteria, cigarette smoke, viruses, and hair), and processing equipment (wear particles, oil, and dirt).

33.7 What is the name of the process most commonly used to grow single-crystal ingots of silicon for semiconductor processing?

Answer. The Czochralski process.

33.8 What are the alternatives to photolithography in IC processing?

Answer. Alternatives to photolithography are extreme ultraviolet lithography (although technically this is still a photolithography technique), electron lithography, X-ray lithography, and ion lithography.

33.9 What is a photoresist?

Answer. A photoresist is a polymer that is sensitive to light radiation in a certain wavelength range; the sensitivity causes either an increase or a decrease in solubility of the polymer to certain chemicals.

33.10 Why is ultraviolet light favored over visible light in photolithography?

Answer. Because it has a shorter wavelength, the transferred images are sharper.

33.11 Name the three exposure techniques in photolithography.

Answer. The three exposure techniques are (1) contact printing, (2) proximity printing, and (3) projection printing.

33.12 What layer material is produced by thermal oxidation in IC fabrication?

Answer. Thermal oxidation produces SiO_2 on the surface of the silicon wafer.

33.13 Define epitaxial deposition.

Answer. Epitaxial deposition involves growth of a crystalline structure on the surface of a substrate that is an extension of the substrate's structure.

33.14 What are the important design functions of IC packaging?

Answer. Design functions of IC packaging include (1) provide electrical connections to external circuits, (2) encase chip for protection, and (3) heat dissipation.

33.15 What is Rent's rule?

Answer. Rent's rule indicates the number of input/output terminals n_{io} required for an integrated circuit of a given number of internal circuits n_{ic}; the Rent's rule equation is: $n_{io} = C\, n_{ic}^{\ m}$, where C and m are constants for a certain circuit type.

33.16 Name the two categories of component mounting to a printed circuit board.

Answer. The two types are (1) through-hole mounting and (2) surface mount technology.

33.17 What is a DIP?

Answer. DIP stands for dual in-line package, an IC package with two rows of terminals on each side of a rectangular body containing the IC chip.

33.18 What does the term *multiprobe* mean?

Answer. Multiprobe refers to the computer-controlled testing procedure that uses a set of needle probes configured to match the connecting pads on the surface of the chip; when the probes contact the pads, a series of direct current tests are carried out to indicate short circuits and other faults; this is followed by a functional test.

33.19 What is the difference between *die bonding* and *wire bonding*?

Answer. Die bonding involves the attachment of the IC chip to the lead frame or package base. Wire bonding involves making electrical connections between the contact pads on the IC chip surface to the leads in the package.

33.20 What is the difference between *postmolding* and *premolding* in plastic IC chip packaging?

Answer. Postmolding refers to the use of transfer molding of epoxy around the chip and leadframe to form the package; a premolded package is one in which an enclosure is molded beforehand, and the chip and leadframe are then attached to it, adding a solid lid to complete the package.

33.21 What is the difference between *area defects* and *point defects* in IC wafer processing?

Answer. Area defects are defects that affect major areas of the wafer, possibly the entire surface. They are caused by variations or incorrect settings in process parameters. Examples include layers that are too thin or too thick, insufficient diffusion depths in doping, and over- or under-etching. Point defects occur in very localized areas on the wafer surface, affecting only one or a limited number of ICs in that area. They are commonly caused by dust particles either on the wafer surface or the lithographic masks.

Problems

Answers to problems labeled **(A)** are listed in an Appendix at the back of the book.

Silicon Processing and IC Fabrication

33.1 (SI units) A single-crystal boule of silicon is grown by the Czochralski process to an average diameter of 320 mm with length = 1500 mm. The seed and tang ends are removed, which reduces the length to 1150 mm. The diameter is ground to 300 mm. A 90-mm-wide flat is ground on the surface that extends from one end to the other. The ingot is then sliced into wafers of thickness = 0.50 mm, using an abrasive saw blade whose thickness = 0.33 mm. Assuming that the seed and tang portions cut off the ends of the starting boule were conical in shape, determine (a) the volume and weight of the original boule; (b) how many wafers are cut from it, assuming the entire 1150-mm length can be sliced; and (c) the volumetric proportion of silicon in the starting boule that is wasted during processing. (d) How much does one wafer weigh? Refer to Table 4.1 for the density of silicon.

Solution: (a) Total volume $V = V_1$ (tang) + V_2 (cylinder) + V_3 (seed)
$V_1 = V_3$ = (cone in which $h = 0.5(1500 - 1150) = 175$, $D = 320$, $R = 160$) = $\pi R^2 h/3$
$= 0.333\pi(160)^2(175) = 4{,}691{,}445$ mm^3
$V_2 = \pi R^2 L = \pi(160)^2(1150) = 92{,}488{,}488$ mm^3
Total $V = 2(4{,}691{,}445) + 92{,}488{,}488 =$ **101,871,378 mm^3**
From Table 4.1, the density of silicon = 7.15 g/cm^3
Weight of the boule $W = 101{,}871{,}378$ mm^3(cm^3/1000mm^3)(7.15 g/cm^3) = 728,380 g = **728.38 kg**

(b) Number of wafers = 1150/(0.50 + 0.33) = 1385.5 → **1385 wafers**

(c) Area of one wafer $A_w = A_c - A_s$, where A_c = area of the circle of radius R = 150 mm, and A_s = the area of the segment A_s created by the flat ground on the cylindrical surface.
$A_c = \pi R^2 = \pi(150)^2 = 70{,}685.8$ mm^2
The area of a segment of the circle created by the 170 mm chord $A_s = \pi R^2\theta/360 - 0.5R^2 \sin\theta$, where θ is the angle formed by two radii of the circle and the chord. $0.5\theta = \sin^{-1}(90/150) = 17.46°$. $\theta = 34.92°$
$A_s = \pi(150)^2(34.92)/360 - 0.5(150)^2 \sin 34.92 = 6{,}855.6 - 6{,}439.1 = 416.5$ mm^2
$A_w = A_c - A_s = 70{,}685.8 - 416.5 = 70{,}269.3$ mm^2
Volume of one wafer $V_w = A_w t = 70{,}269.3(0.5) = 35{,}134.7$ mm^3
Volume of 1385 wafers = 1385(35134.7) = 48,661,490 mm^3
Volume wasted = 101,871,378 – 48,661,490 = 53,209,888 mm^3
Proportion wasted = 53,209,888/101,871,378 = **52.23%**

(d) Weight of one wafer $W = 35{,}134.7$ mm^3(cm^3/1000mm^3)(7.15 g/cm^3)
= 251.2 g = 0.251 kg

33.2 (USCS units) A silicon boule is grown by the Czochralski process to a diameter of 5.25 in and a length of 5 ft. The seed and tang ends are cut off, reducing the effective length to 48.00 in. Assume that the seed and tang portions are conical in shape. The diameter is ground to 4.921 in (125 mm). A primary flat of width 1.625 in is ground on the surface the entire length of the ingot. The ingot is then sliced into wafers 0.025 in thick, using an abrasive saw blade whose thickness = 0.0128 in. Determine the (a) volume and weight of the original boule, (b) number of wafers cut from it, assuming the entire 4-ft length can be sliced, and (c) volumetric proportion of silicon in the starting boule that is wasted during processing. (d) How much does one wafer weigh? Refer to Table 4.1 for the density of silicon.

Solution: (a) Volume $V = V_1$ (tang) + V_2 (cylinder) + V_3 (seed)
$V_1 = V_3$ = (cone in which $h = 0.5(60 - 48) = 6.0$, $D = 5.25$) = $\pi R^2 h/3 = 0.333\pi(5.25/2)^2(6.0)$ = 43.295 in^3.
$V_2 = \pi D^2 L/4 = \pi(5.25)^2(48)/4 = 1039.082$ in^3
$V = 2(43.295) + 1039.082 =$ **1125.672 in^3**
From Table 4.1, the density of silicon = 0.258 lb/in^3
Weight of the boule $W = 1125.67$ in^3(0.258 lb/in^3) = **290.4 lb**

(b) Number of wafers = 48.0/(0.025 + 0.013) = 48/(0.038) = 1263.2 → **1263 wafers**

(c) Area of one wafer $A_w = A_c - A_s$, where A_c = area of the circle of radius $R = 4.921/2 = 2.4605$ in, and A_s = the area of the segment A_s created by the flat ground on the cylindrical surface.
$A_c = \pi R^2 = \pi(2.4605)^2 = 19.0194$ in^2
The area of a segment of the circle created by the 1.625 in chord $A_s = \pi R^2\theta/360 - 0.5R^2 \sin\theta$, where θ is the angle formed by two radii of the circle and the chord. $0.5\theta = \sin^{-1}(1.625/4.921) = 19.28°$. $\theta = 38.56°$
$A_s = \pi(2.4605)^2(38.56)/360 - 0.5(2.4605)^2 \sin 38.56 = 2.0372 - 1.8869 = 0.1503$ in^2
$A_w = A_c - A_s = 19.0194 - 0.1503 = 18.8691$ in^2
Volume of one wafer $V_w = A_w t = 18.8691(0.025) = 0.4717$ in^3
Volume of 1263 wafers = 1263(0.4717) = 595.76 in^3
Volume wasted = 1125.672 – 595.76 = 529.9 in^3
Proportion wasted = 529.9/1125.672 = **47.08%**

(d) Weight of one wafer $W = 0.4717$ in^3(0.258 lb/in^3) = 0.121 lb

33.3 **(A)** (SI units) A 250-mm-diameter silicon wafer has a processable area whose diameter = 225 mm. The IC chips that will be fabricated on the wafer surface are square with 20 mm on a side. However, the processable area on each chip is only 18 mm by 18 mm. The density of circuits within each chip's processable area is 465 circuits per mm^2. (a) How many IC chips can be placed on the wafer? (b) How many circuits can be fabricated on each chip?

Solution: (a) $n_c = 0.34(D_w/L_c)^{2.25} = 0.34(225/20)^{2.25} = 0.34(11.25)^{2.25}$
= 78.8 round to **78 chips**

(b) Each chip surface area = 18 × 18 = 324 mm^2
Number of internal circuits per chip $n_{ic} = 324(465) =$ **150,660**

33.4 (USCS units) A 15-in-diameter silicon wafer has a processable circular area with diameter = 14.4 in. The IC chips that will be fabricated on the wafer surface are square with 1.0 in on a side, including an allowance for subsequent chip separation. The processable area on each chip is only 0.80 in by 0.80 in. The density of circuits within each chip's processable area is 400,000 circuits per square inch. (a) How many IC chips can be placed on the wafer? (b) How many circuits can be fabricated on each chip?

Solution: (a) $n_c = 0.34(D_w/L_c)^{2.25} = 0.34(14.4/1.0)^{2.25} = 0.34(14.4)^{2.25} =$ **137 chips**

(b) Each chip surface area = $0.80 \times 0.80 = 0.64$ in^2
Number of internal circuits per chip $n_{ic} = 400{,}000(0.64) =$ **256,000**

33.5 (SI units) Two wafer sizes are to be compared: A 156-mm wafer with a processable area = 150-mm diameter circle and a 312-mm wafer with a processable area = 300-mm diameter circle. The IC chips in both cases are square with 10 mm on a side. Assume the cut lines (streets) between chips are of negligible width. What is the percent increase in (a) wafer diameter, (b) processable wafer area, and (c) number of chips for the larger wafer size?

Solution: (a) Increase in wafer diameter = (300 – 150)/150 = 1.0 = **100% increase**

(b) For the 156 mm wafer, $A = \pi(150)^2/4 = 17{,}671$ mm^2
For the 312 mm wafer, $A = \pi(300)^2/4 = 70{,}686$ mm^2
Increase in processable wafer area = (70,686 – 17,671)/17,671 = 3.0 = **300% increase**

(c) For the 156 mm wafer, $n_c = 0.34(150/10)^{2.25} = 0.34(15)^{2.25} = 150$ chips
For the 312 mm wafer, $n_c = 0.34(300/10)^{2.25} = 0.34(30.0)^{2.25} = 716$ chips
Increase in number of chips = (716 – 150)/150 =3.77 = **377% increase**

Note: These results indicate the advantages of increasing wafer size. For a 300% increase in processable area, a 377% increase in number of chips is achieved. This is a principal motivation for using larger wafer diameters.

33.6 **(A)** (USCS units) Two silicon wafer sizes are to be compared: A 6.0-in wafer with a processable area = 5.85-in-diameter circle and a 12.0-in wafer with a processable area = 11.75-in-diameter circle. The IC chips in both cases are square with 0.50 in on a side. Assume the cut lines (streets) between chips are of negligible width. What is the percent increase in (a) processable area on the wafer and (b) number of chips on the wafer compared to the 200% increase in wafer diameter?

Solution: (a) For the 6-in wafer, $A = \pi(5.85)^2/4 = 26.88$ in^2
For the 12-in wafer, $A = \pi(11.75)^2/4 = 108.43$ in^2
Increase in processable area = (108.43 – 26.88)/26.88 = 3.03 = **303% increase**

(b) For the 6-in wafer, $n_c = 0.34(5.85/0.5)^{2.25} = 0.34(11.7)^{2.25} = 86$ chips
For the 12-in wafer, $n_c = 0.34(11.75/0.5)^{2.25} = 0.34(23.5)^{2.25} = 413$ chips
Increase in number of chips = (413 – 86)/86 = 3.81 = **381% increase**

Note: The wafer diameter increases by 100%, the wafer area increases by 303%, and the number of chips increases by 381%. This is a principal motivation for using larger wafer diameters.

33.7 (SI units) A silicon boule has been processed through grinding to provide a cylinder whose diameter = 285 mm and whose length = 900 mm. Next, it will be sliced into wafers 0.7 mm

thick using a cut-off saw with a kerf = 0.5 mm. The wafers thus produced will be used to fabricate as many IC chips as possible for the personal computer market. Each IC has a market value to the company of $98. Each chip is square with 15 mm on a side. The processable area of each wafer is defined by a diameter = 270 mm. Estimate the value of all of the IC chips that could be produced, assuming an overall yield of 80% good product.

Solution: First determine the number of wafers that can be obtained from the cylinder. Each wafer takes 0.7 + 0.5 mm = 1.2 mm of the cylinder's length. Thus, the number of wafers is given by: $n_w = 900/1.2 = 750$ wafers
Next determine the number of chips per wafer: $n_c = 0.34(270/15)^{2.25}$
$= 0.34(18)^{2.25} = 227$ IC chips
The total number of chips on 750 wafers, accounting for the yield of 80% is given by:
Total number of chips = 750(227)(0.80) = 136,200 good chips.
At $98/chip, the total value = 136,200($98) = **$13,347,600**.

33.8 (SI units) It is desired to etch out a region of a silicon dioxide film on the surface of a silicon wafer. The SiO_2 film is 100 nm thick. The width of the etched-out area is specified to be 650 nm. (a) If the degree of anisotropy for the etchant in the process is known to be 1.25, what should be the size of the opening in the mask through which the etchant will operate? (b) If plasma etching is used instead of wet etching, and the degree of anisotropy for plasma etching is infinity, what should the size of the mask opening be?

Solution: (a) Anisotropy degree $A = d/u = 1.25$, $u = d/1.25 = 100/1.25 = 80$ nm
Mask opening size = 650.0 – 2(80) = **490 nm**

(b) $A = d/u = \infty$. $u = d/\infty = 0$ nm
Mask opening size = 650.0 – 2(0) = **650 nm**

IC Packaging

33.9 **(A)** An integrated circuit used in a microprocessor will contain 50,000 logic gates. Use Rent's rule to determine the approximate number of input/output terminals required in the package. Use Table 33.4 for parameter values.

Solution: From Table 33.4, $C = 0.89$ and $m = 0.45$
Rents rule: $n_{io} = Cn_{ic}^{m} = 0.89(50{,}000)^{0.45}$ = **116 input/output terminals**

33.10 A static random access memory uses a dual-in-line package that has a total of 36 leads. Use Rent's rule to determine the approximate number of transistors that could be fabricated in the chip for this package. Use Table 33.4 for parameter values.

Solution: From Table 33.4, $C = 6.9$ and $m = 0.12$
Rents rule: $36 = 6.9(n_{ic})^{0.12}$
$n_{ic}^{0.12} = 36/6.9 = 5.217$ $\quad n_{ic} = (5.217)^{8.333}$ =**951,786 transistors**

Comment: Because 6 transistors are required for each memory cell in SRAM, the total number of memory cells would be 158,631.

33.11 It is desired to determine the effect of package style on the number of circuits that can be fabricated onto a microprocessor chip to which the package is assembled. Using Rent's rule, compute the estimated number of circuits that could be placed on the chip in the following cases: (a) a DIP with 16 I/O terminals on a side - a total of 32 terminals; (b) a square chip

carrier with 16 terminals on a side - a total of 64 I/O terminals; and (c) a ball grid array with 16 by 16 terminals - a total of 256 terminals. Use Table 33.4 for parameter values.

Solution: (a) From Table 33.4, $C = 0.89$ and $m = 0.45$
Rent's rule: $n_{io} = 0.89(n_{ic})^{0.45}$, find n_{ic} if $n_{io} = 32$
$n_{ic}^{0.45} = 32/0.89 = 35.96$
n_{ic} = **2866 logic gates**

(b) Find n_{ic} if $n_{io} = 64$
$n_{ic}^{0.45} = 64/0.89 = 71.91$
n_{ic} = **13,372 logic gates**

(c) Find n_{ic} if $n_{io} = 256$
$n_{ic}^{0.45} = 256/0.89 = 287.64$
n_{ic} = **291,142 logic gates**

33.12 **(A)** To produce a 1-megabit memory chip, how many I/O terminals are predicted by Rent's for (a) a static random access memory, which requires six transistors per bit, and (b) a dynamic random access memory, which requires only one transistor per bit? Use Table 33.4 for parameter values.

Solution: (a) Rent's rule for SRAM: $n_{io} = 6.9\, n_{ic}^{0.12} = 6.9(6 \times 1{,}000{,}000)^{0.12}$
$= 44.9 \rightarrow$ **45 terminals**

(b) Rent's rule for DRAM: $n_{io} = 7.8\, n_{ic}^{0.07} = 7.8(1{,}000{,}000)^{0.07} = 20.5 \rightarrow$ **21 terminals**

33.13 The first IBM personal computer was based on the Intel 8088 CPU, which was released in 1979. The 8088 had 29,000 transistors and 40 I/O terminals. The final version of the Pentium III (1 GHz) was released in 2000. It contained 28,000,000 transistors and had 370 I/O terminals. (a) Determine the Rent's rule coefficient values m and C, assuming that a transistor can be considered a circuit. (b) Use the value of m and C to predict the number of I/O terminals required for the first Pentium 4, assuming that it is manufactured with 42,000,000 transistors. (c) The first Pentium 4, released in 2001, used 423 I/O terminals. Comment on the accuracy of your prediction.

Solution: (a) $n_{io} = C\, n_{ic}^{m}$; rearranging, $C = n_{io}/\, n_{ic}^{m}$. Two equations can be constructed from the data: (1) For the 8088: $C = 40/29{,}000^{m}$ and (2) for the Pentium III: $C = 370/28{,}000{,}000^{m}$
$40/29{,}000^{m} = 370/28{,}000{,}000^{m}$
$40/370 = (29 \times 10^{3})^{m}/(28 \times 10^{6})^{m}$
$0.108108 = (29 \times 10^{3}/28 \times 10^{6})^{m}$
$\ln(0.108108) = m \ln(0.001036)$
$m = -2.2246/(-6.8727) = 0.3237$
$C = 40/(29{,}000^{0.3237}) = 40/27.8277 = 1.437$
$\boldsymbol{n_{io} = 1.437\, n_{ic}^{0.3237}}$

(b) $n_{io} = 1.437\ (42{,}000{,}000)^{0.3237} = 421.8 =$ **422 terminals**

(c) The actual and predicted values are almost too close to believe. Note that an updated Pentium 4 (2.2 GHz) released 6 months later increased to 55,000,000 transistors and remained at 423 I/O terminals, so it does not fit as well for these coefficients of m and C. In very large integrated circuits that must remain backward compatible, the I/O terminals are

often frozen until the next generation. However, designers will add transistors to increase the functionality and speed of the processors. Therefore, there are discontinuities in the I/O terminal count as new generations are released.

Yields in IC Processing

33.14 On a particular production line in a wafer fabrication facility, the crystal yield is 60%, the crystal-to-slice yield is 60%, wafer yield is 90%, multiprobe is 70%, and final test yield is 80%. (a) What is the overall yield for the production line? (b) If wafer yield and multiprobe yield are combined into the same reporting category, what overall yield for the two operations would be expected?

Solution: (a) Overall $Y = Y_c\ Y_s\ Y_w\ Y_m\ Y_t$ = (0.60)(0.60)(0.90)(0.70)(0.80) = 0.1814 = **18.14%**

(b) $Y_w\ Y_m$ = (0.90)(0.70) = 0.63 = **63%**

33.15 **(A)** (SI units) A silicon wafer with a diameter of 300 mm is processed over a circular area whose diameter = 285 mm. The chips to be fabricated are square with 15 mm on a side. From previous experience, the density of point defects in the surface area is 0.003 defects/cm^2. Determine an estimate of the number of good chips using the Bose-Einstein yield computation.

Solution: $n_c = 0.34(285/15)^{2.25} = 0.34(19)^{2.25}$ = 256 chips
Processable wafer area $A = \pi(285)^2/4$ = 63,794 mm^2 = 637.94 cm^2
$Y_m = 1/(1 + AD) = 1/(1 + 637.94 \times 0.003) = 1/2.914 = 0.3432$
Number of good chips = 0.3432(256) = 87.9 $\rightarrow$ **88 good chips**

33.16 (SI units) The yield of good chips in multiprobe for a certain batch of wafers is 75%. The wafers have a diameter of 300 mm with a processable area that is 280 mm in diameter. If the defects are all assumed to be point defects, determine the density of point defects using the Bose-Einstein method of estimating yield.

Solution: $Y_m = 1/(1 + AD)$
Processable area $A = \pi(280)^2/4$ = 61,575 mm^2 = 615.75 cm^2
$0.75 = 1/(1 + 615.75\ D)$
$0.75(1 + 615.75\ D) = 0.75 + 461.8\ D = 1$
$461.8\ D = 1 - 0.75 = 0.25$ $\quad D = 0.25/461.8 =$ **0.00054 defects/cm^2**

33.17 (USCS units) A silicon wafer has a processable area of 75.0 in^2. The yield of good chips on this wafer is Y_m = 80%. If the defects are all assumed to be point defects, determine the density of point defects using the Bose-Einstein method of estimating yield.

Solution: $Y_m = 1/(1 + AD)$
Processable area A = 75 in^2
$0.80 = 1/(1 + 75\ D)$
$0.80(1 + 35\ D) = 0.80 + 60\ D = 1$
$60\ D = 1 - 0.80 = 0.20$ $\quad D = 0.20/60 =$ **0.00333 defects/in^2**