

TFE4188 - Introduction to Lecture 8

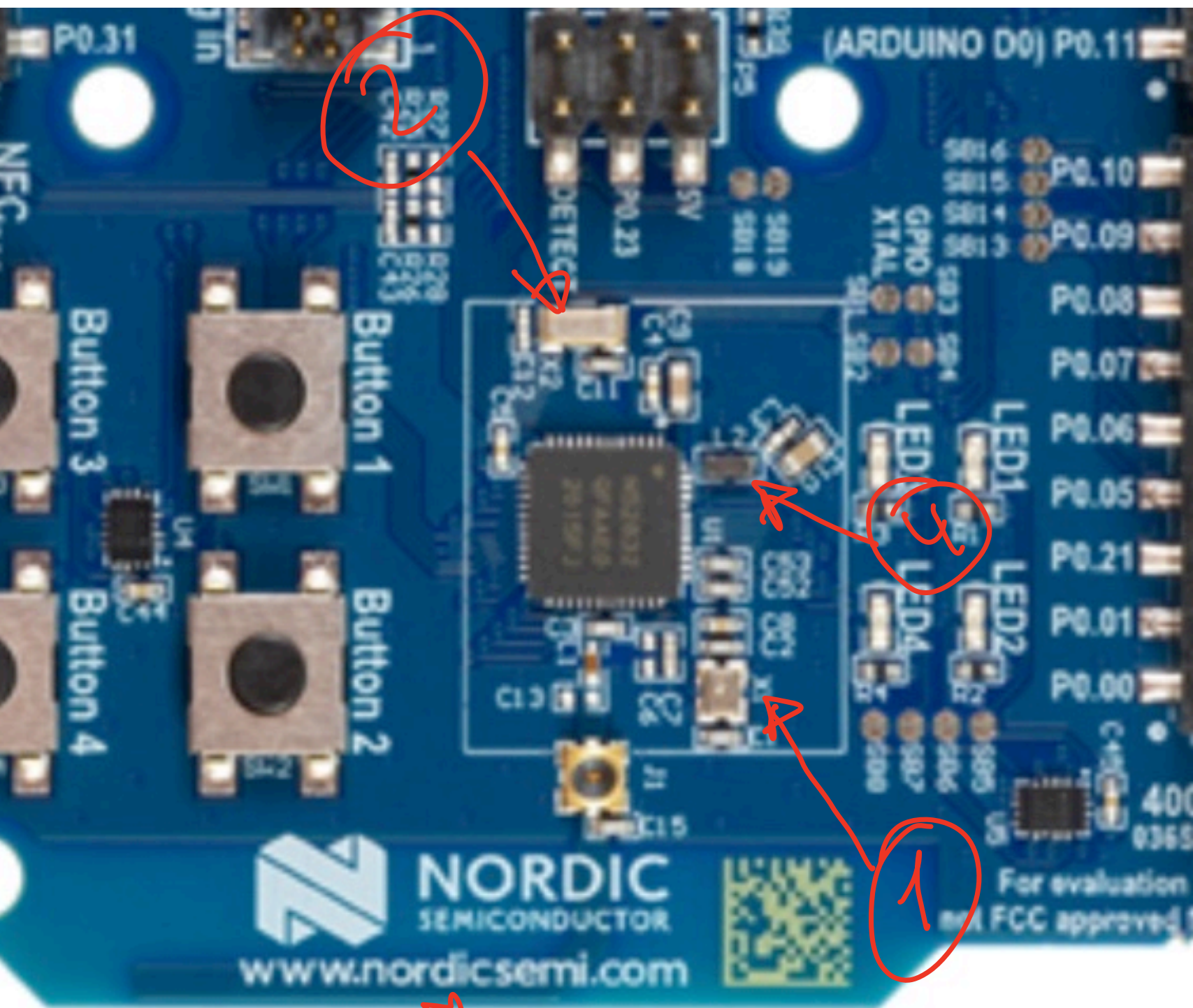
Clocks and PLLs

Goal

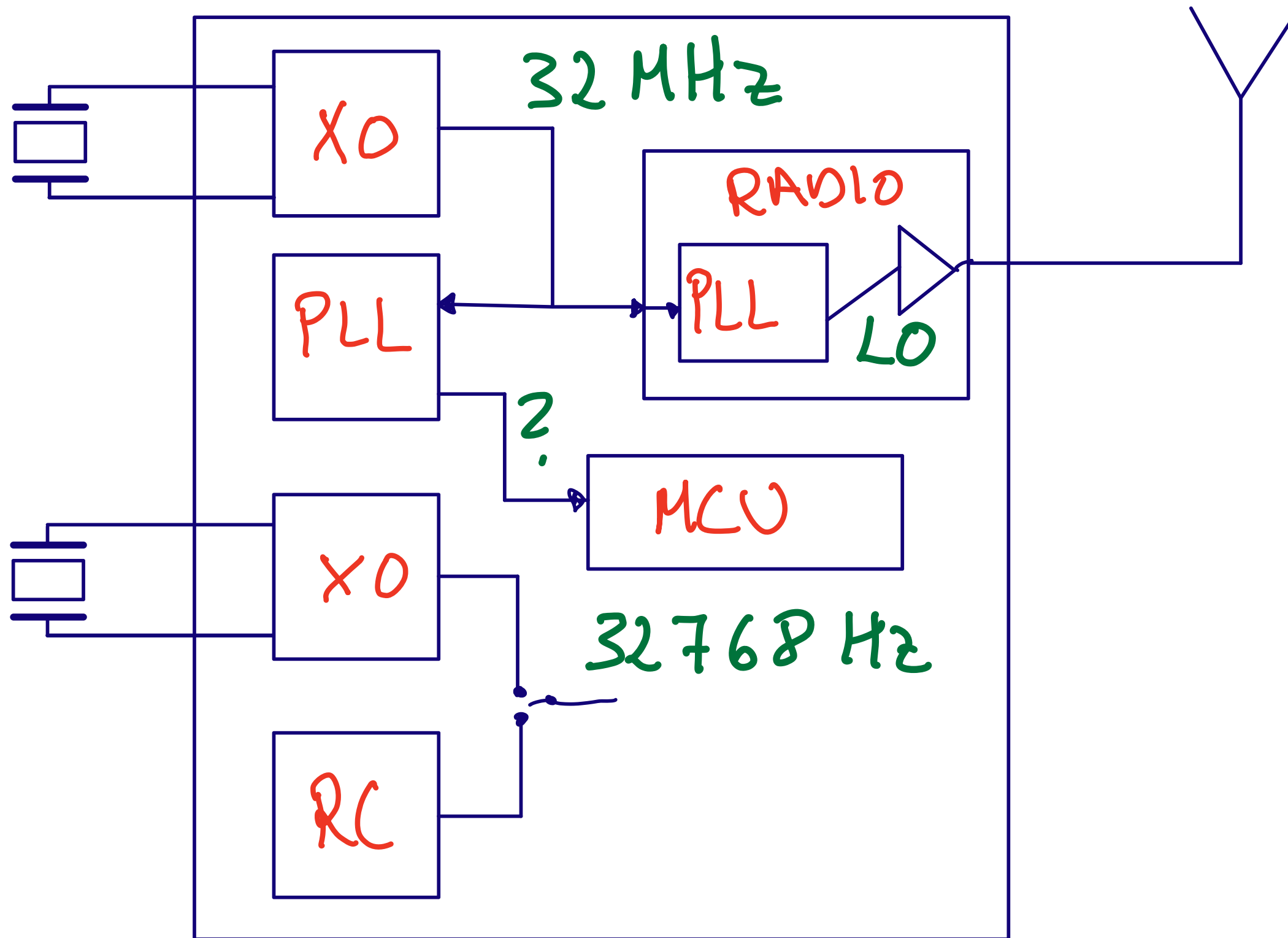
Why do we need to generate clocks

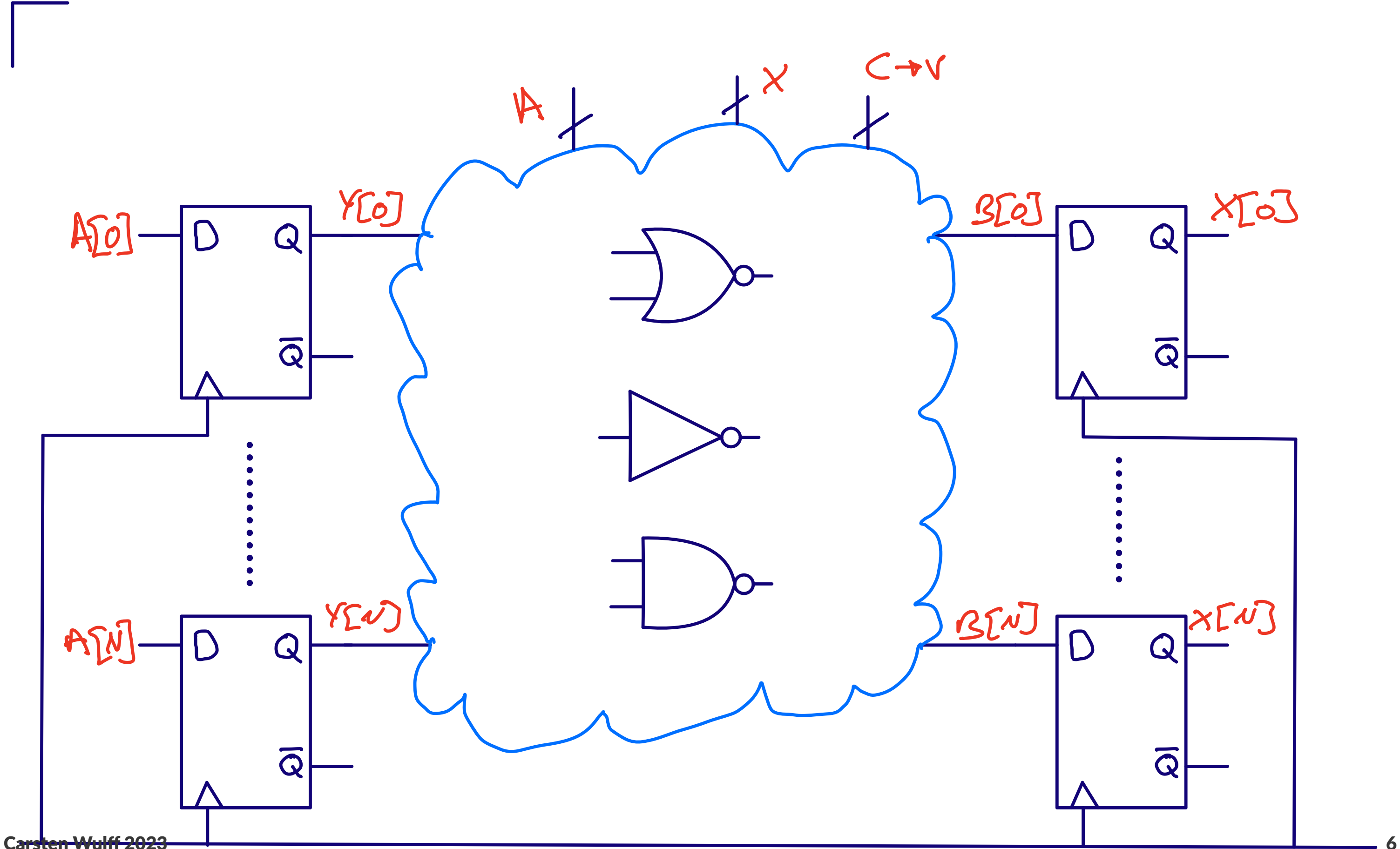
Introduction to **PLLs**

why

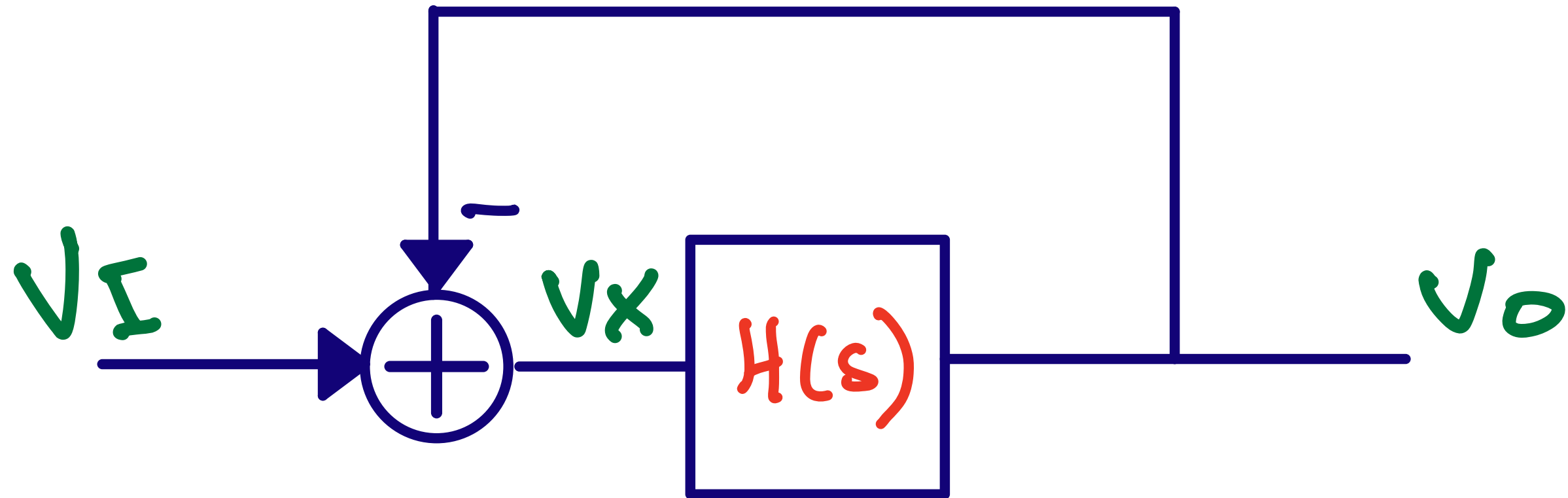


1. 32 MHz crystal
2. 32 KiHz crystal
3. In PCB antenna
4. DC/DC inductor



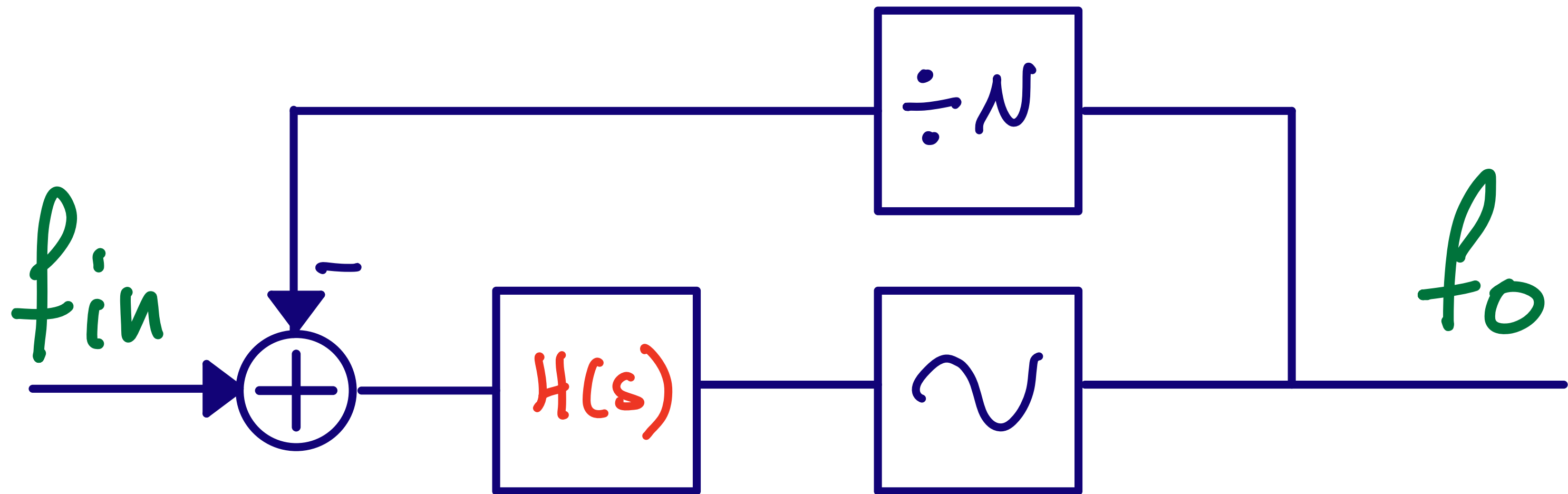


PL

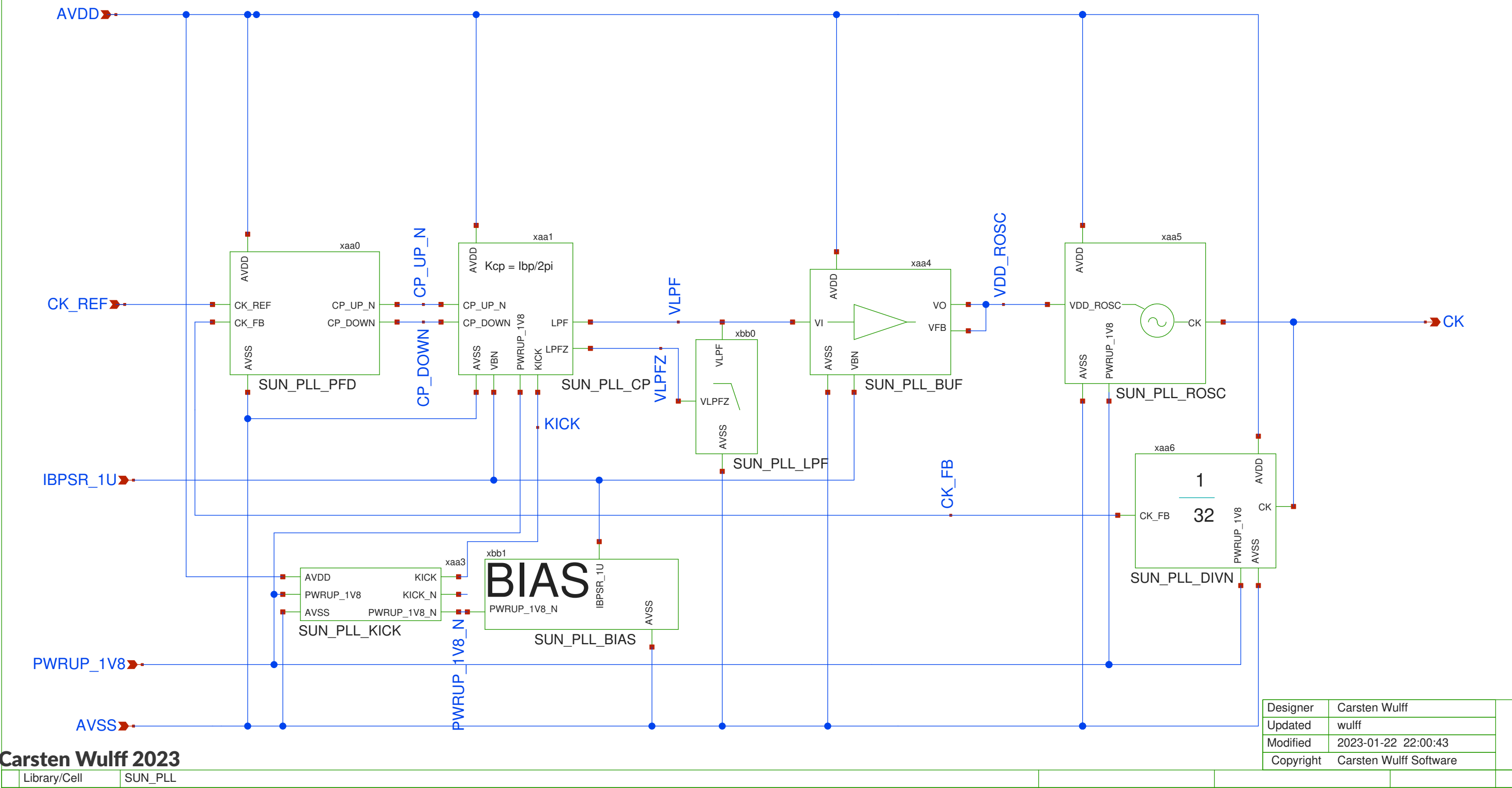


$$V_I - V_O = V_X \quad V_O = V_X H(s)$$

$$V_I \approx V_O + \frac{V_O}{H(s)} \quad \Rightarrow \quad H(s) = \infty \quad V_O = V_I$$



16 MHz x 32 = 512 MHz PLL

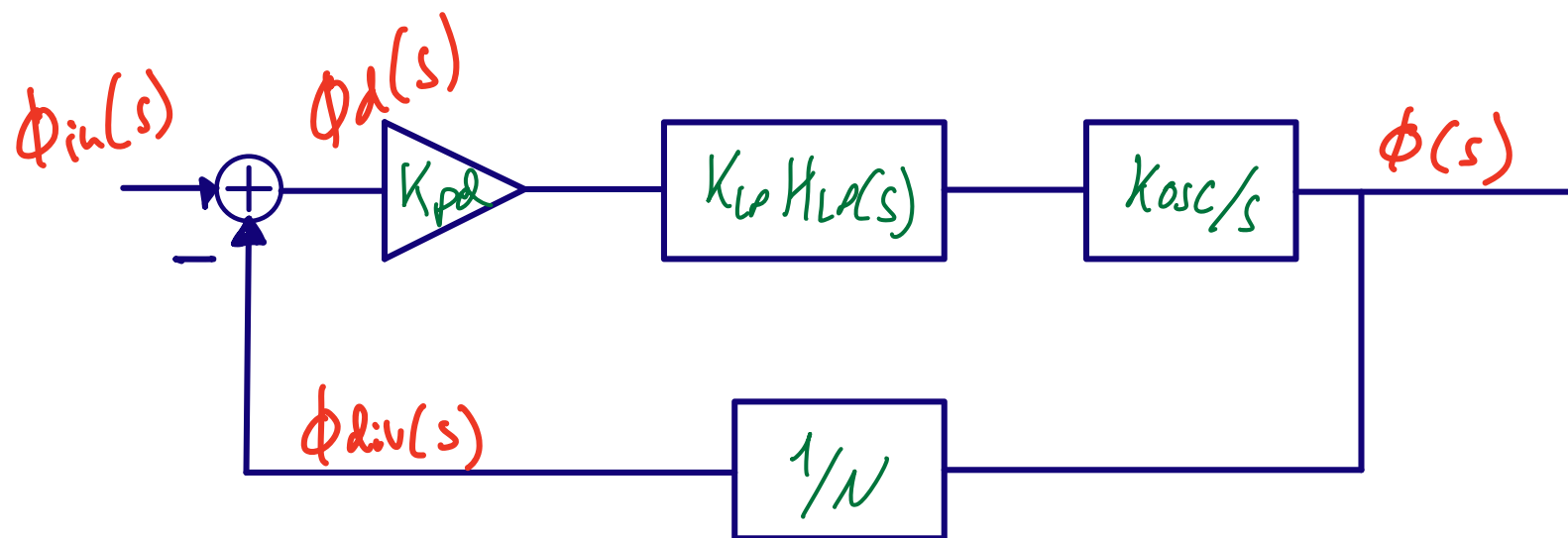


PLLs need calculation!

#noCowboyDesign

$$\phi(t) = 2\pi \int_0^t f(t) dt$$

PLLs are assumed to be linear in phase

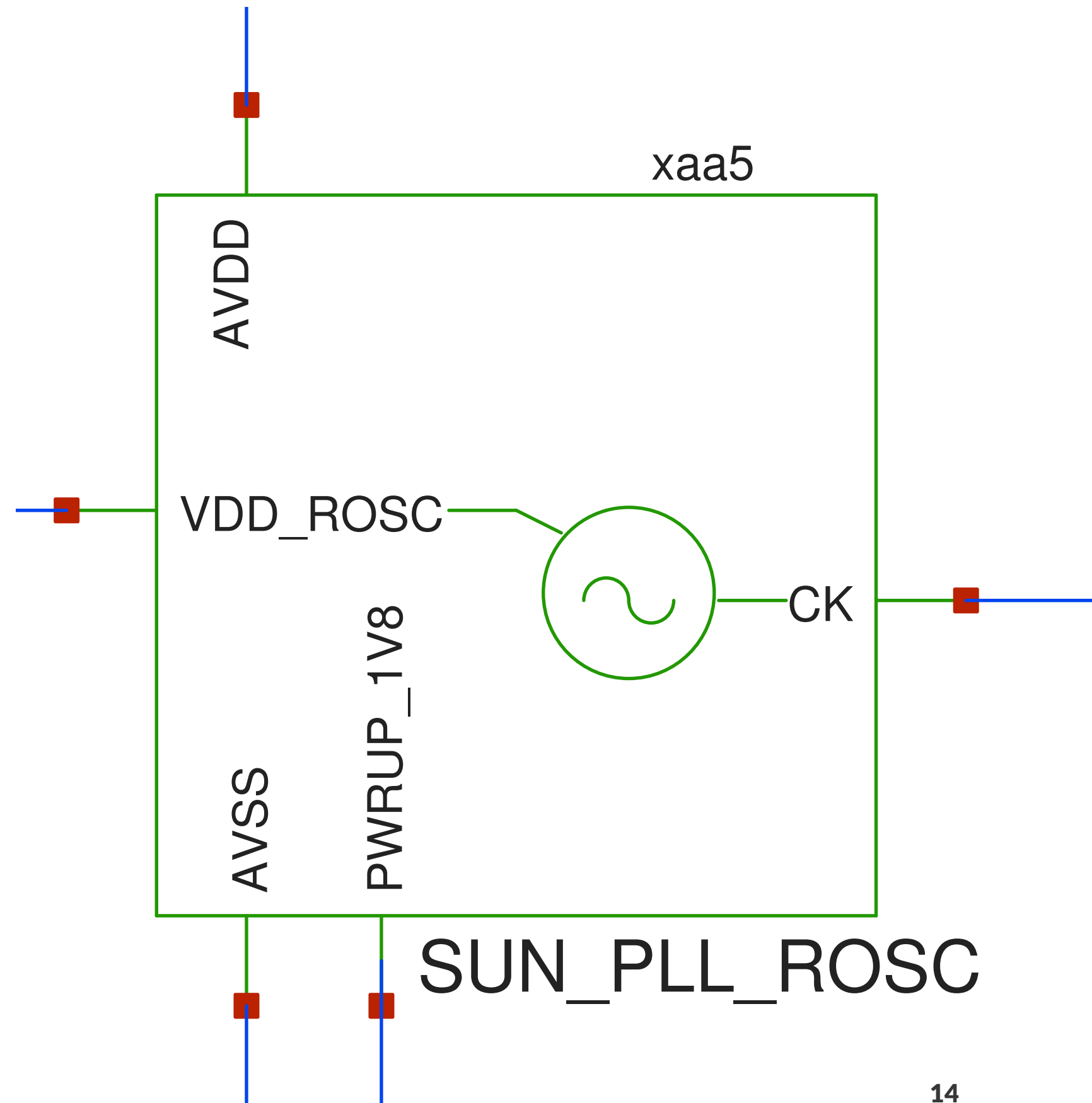


$$\frac{\phi_d}{\phi_{in}} = \frac{1}{1 + L(s)}$$

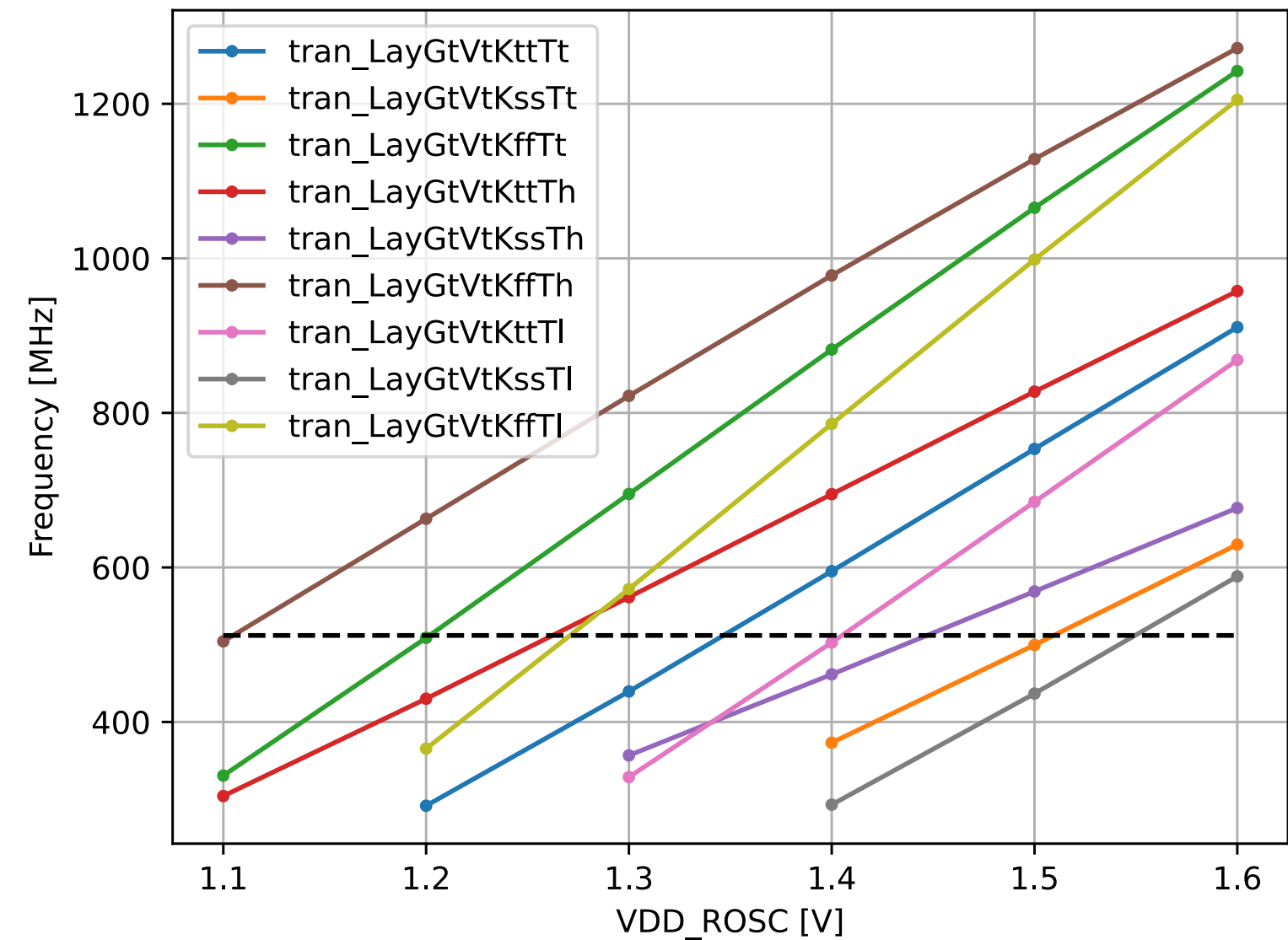
$$L(s) = \frac{K_{osc} K_{pd} K_{lp} H_{lp}(s)}{Ns}$$

Voltage controlled oscillator

$$K_{osc} = 2\pi \frac{df}{dV_{cntl}}$$

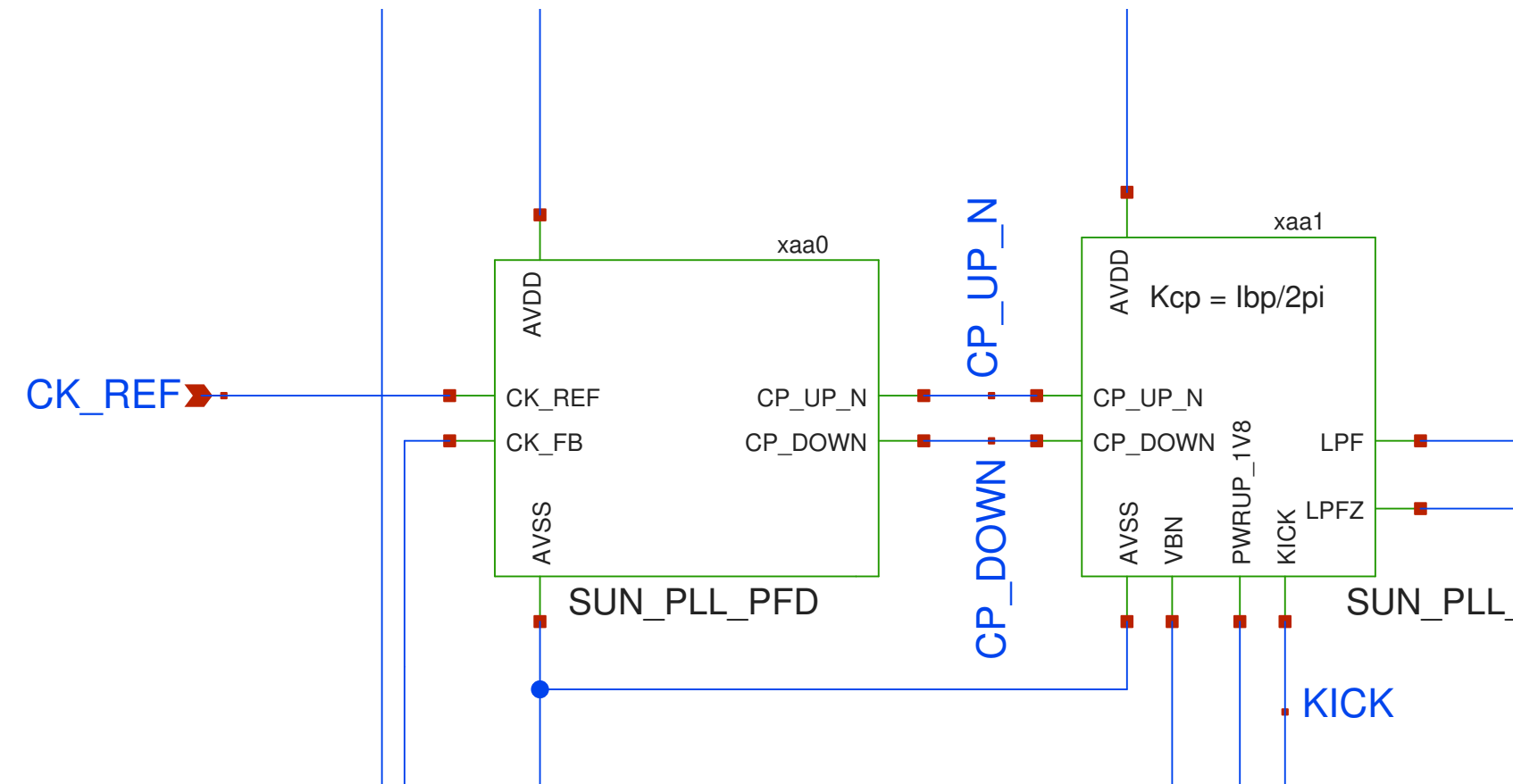


SUN_PLL_SKY130NM/ sim/ROSC/



Phase detector and charge pump

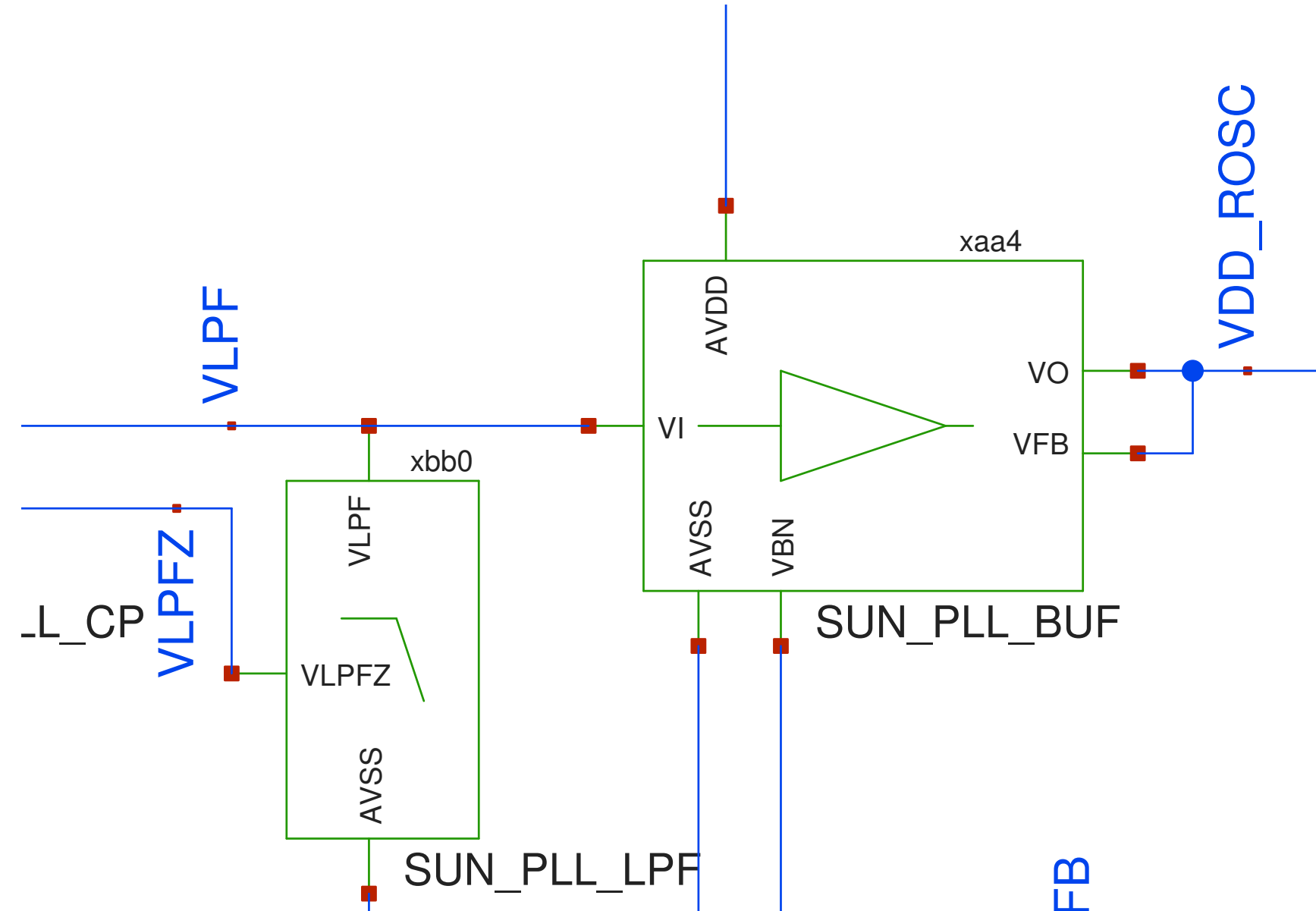
$$K_{pd} = \frac{I_{cp}}{2\pi}$$



Loop filter

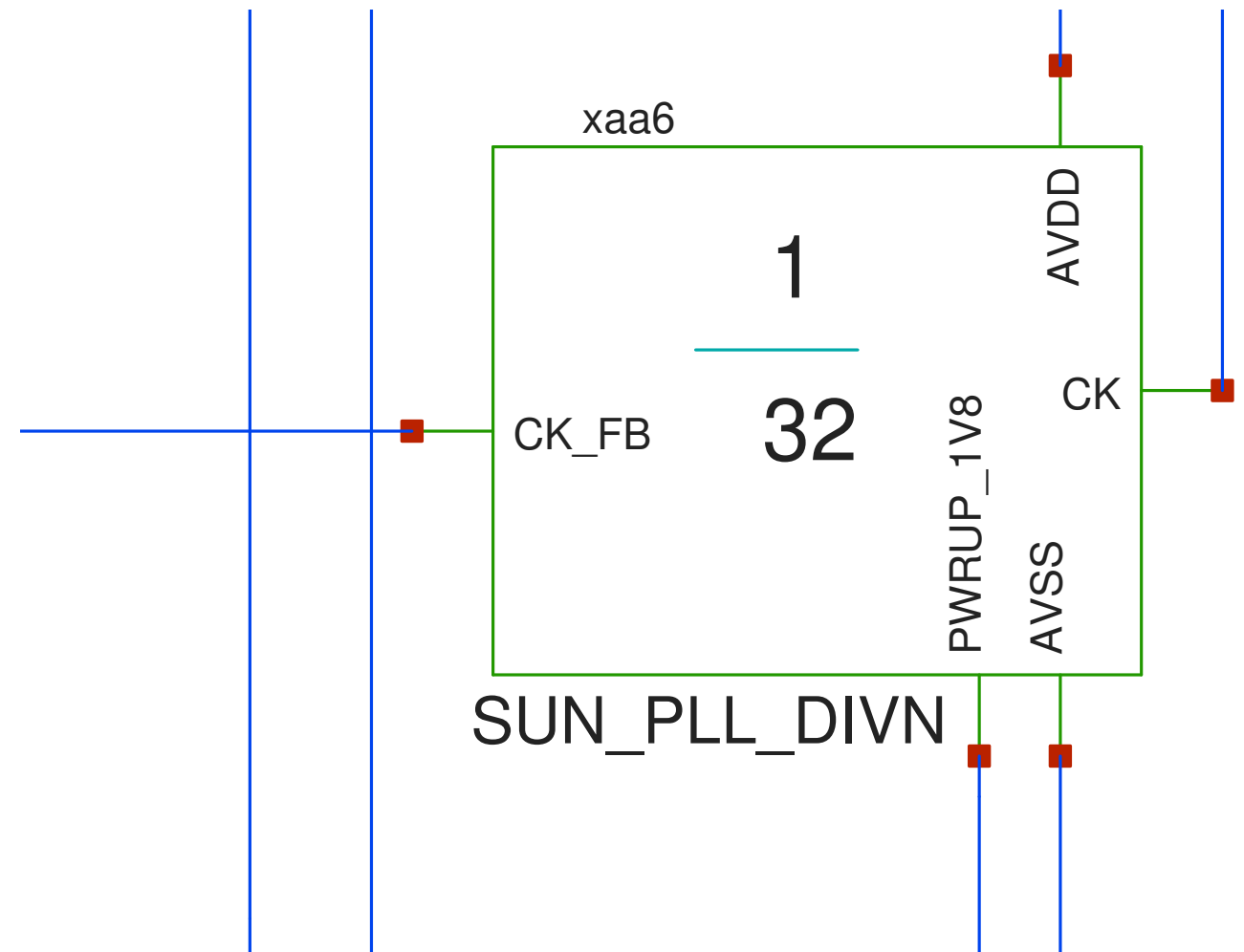
$$K_{lp}H_{lp}(s) = K_{lp} \left(\frac{1}{s} + \frac{1}{\omega_z} \right)$$

$$K_{lp}H_{lp}(s) = \frac{1}{s(C_1 + C_2)} \frac{1 + sRC_1}{1 + sR\frac{C_1C_2}{C_1+C_2}}$$



Divider

$$K_{div} = \frac{1}{N}$$

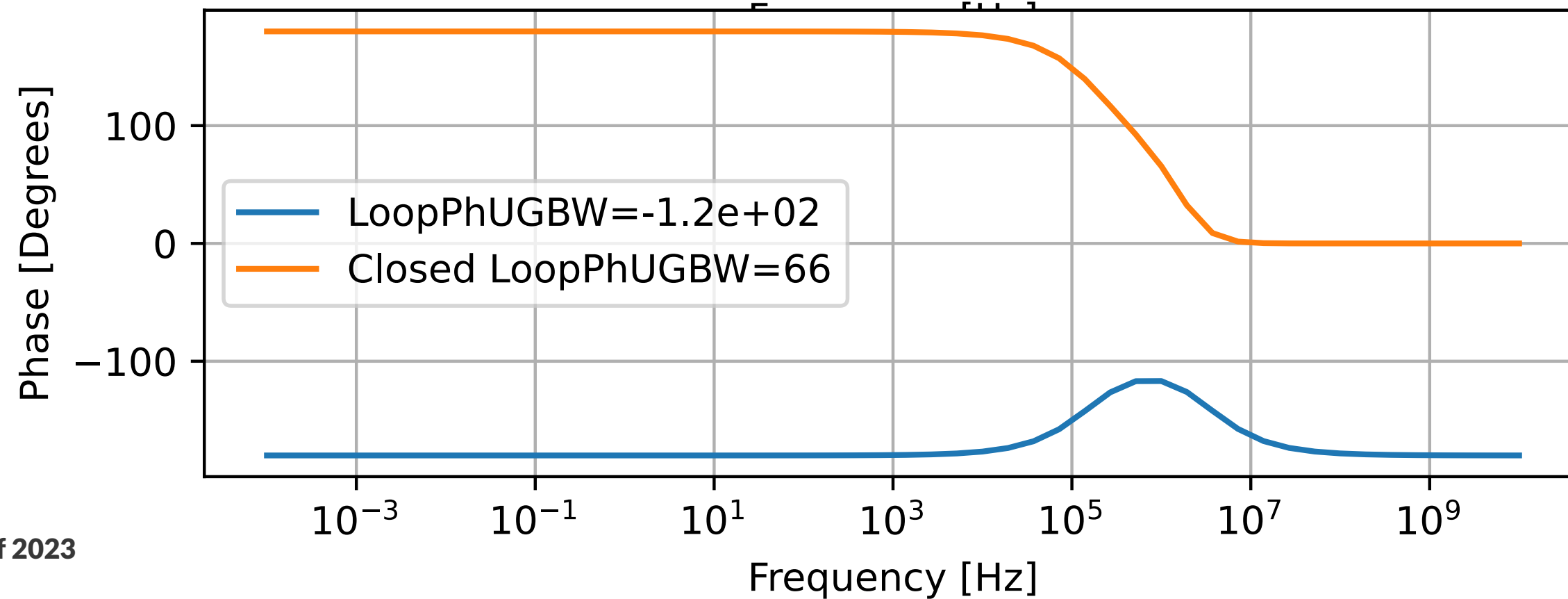
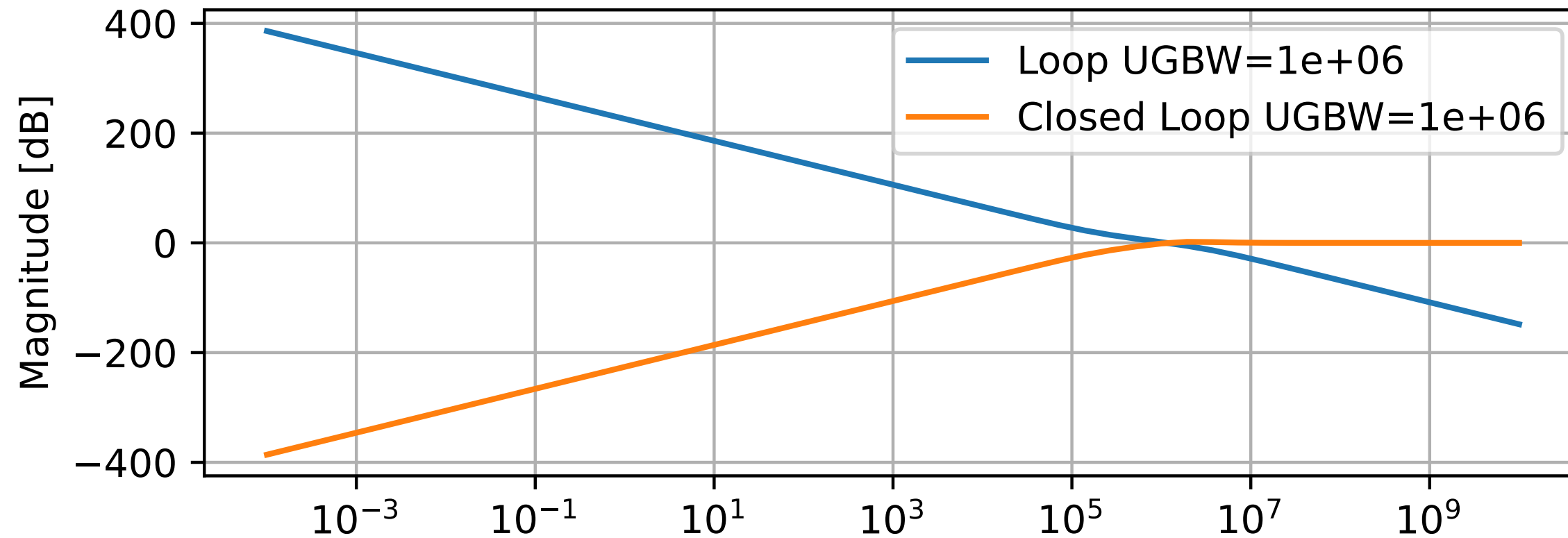


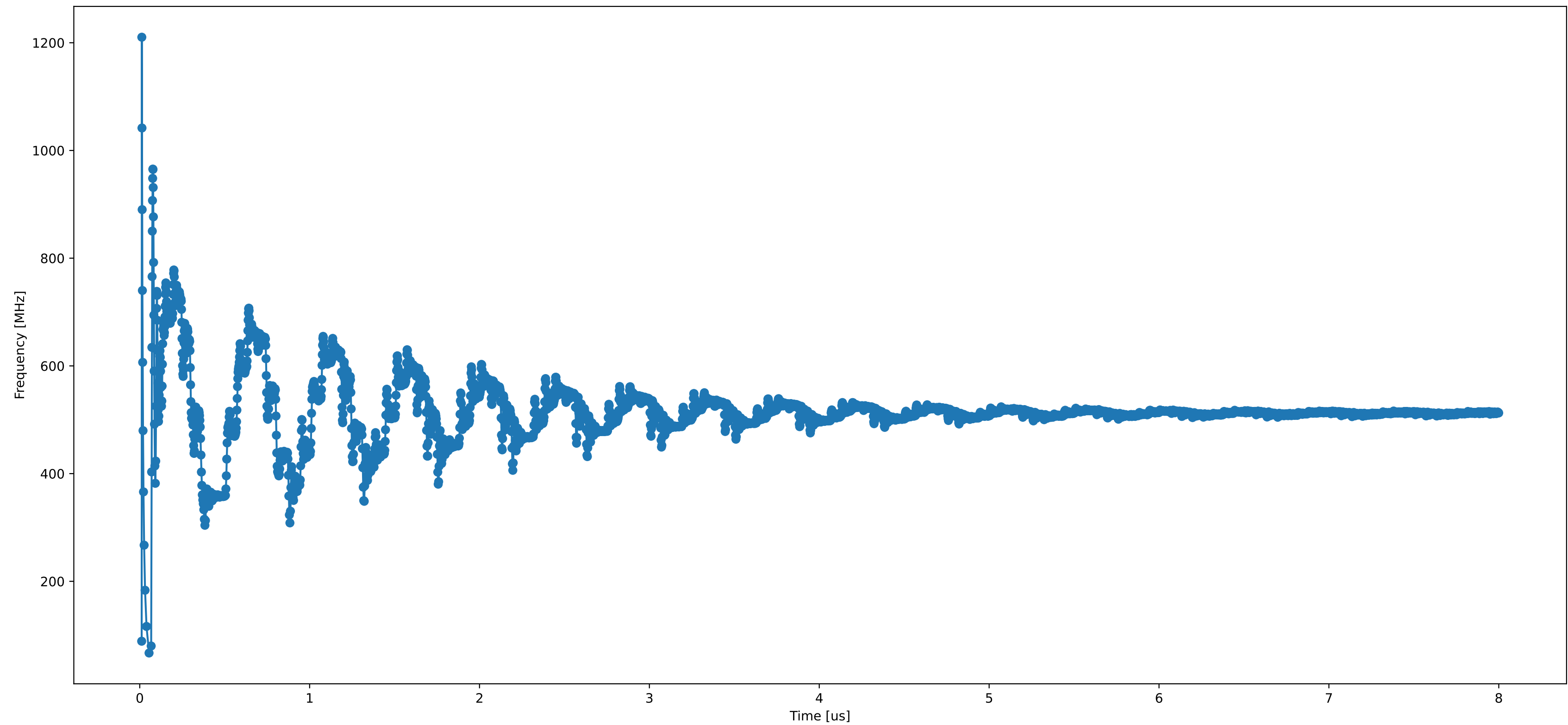
Loop function

$$L(s) = \frac{K_{osc} K_{pd} K_{lp} H_{lp}(s)}{Ns}$$

Python model

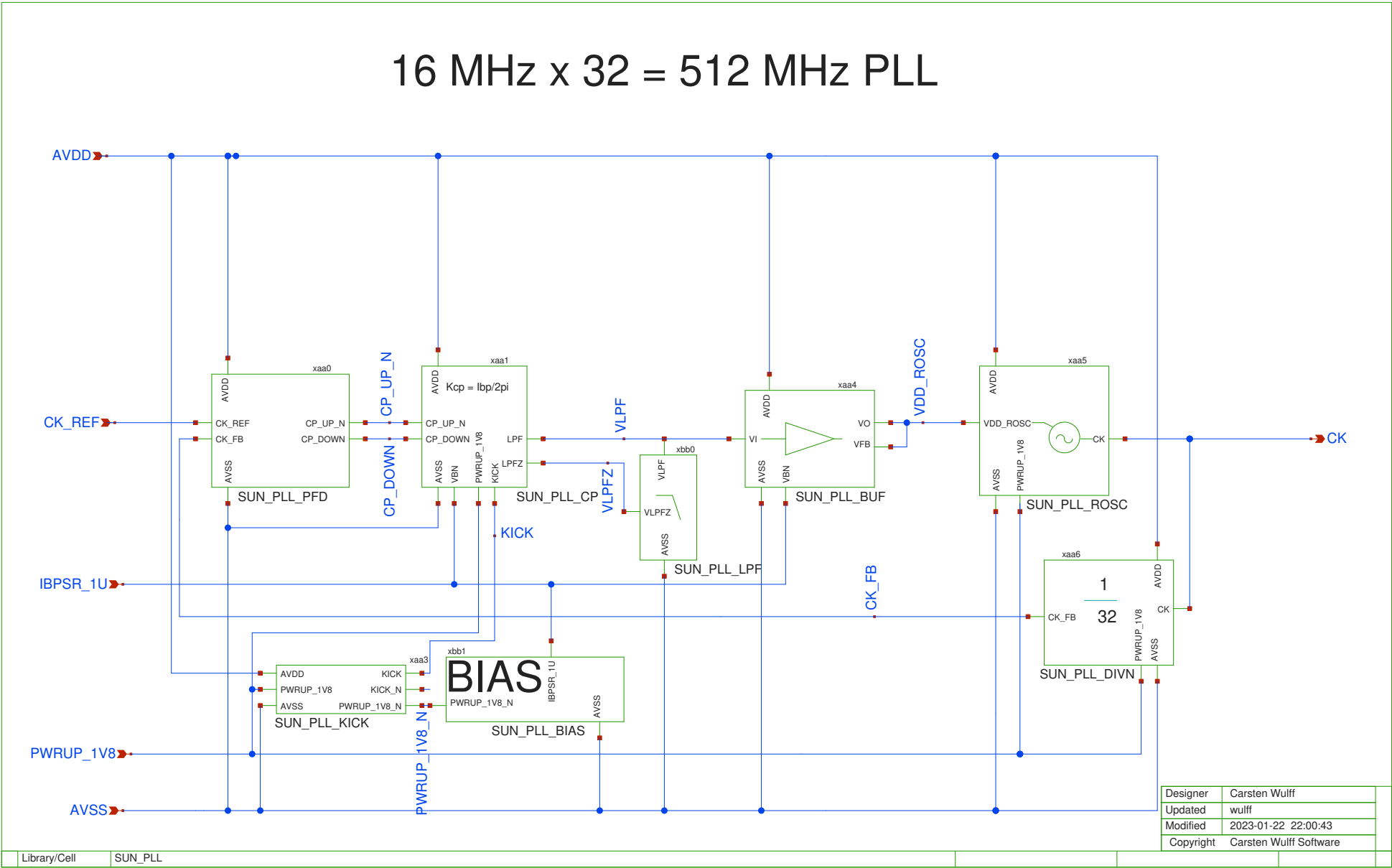
[sun_pll_sky130nm/py/pll.py](#)



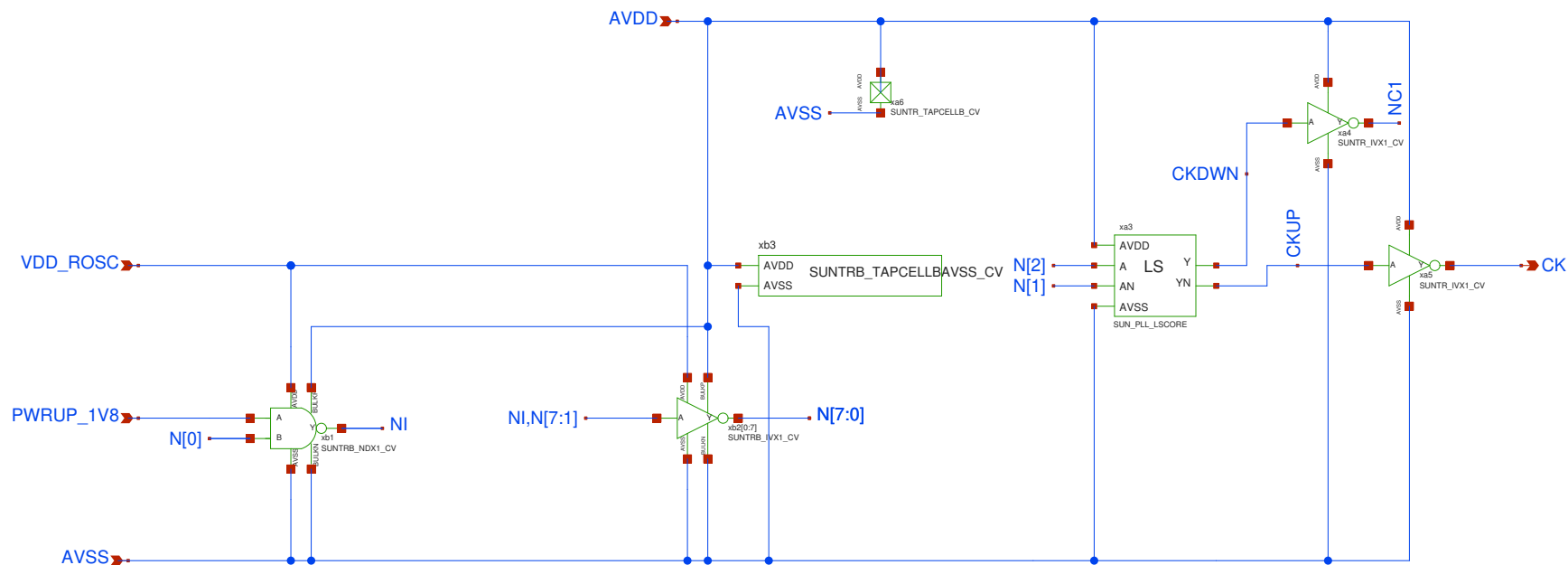


SUN_PLL_SKY130NM

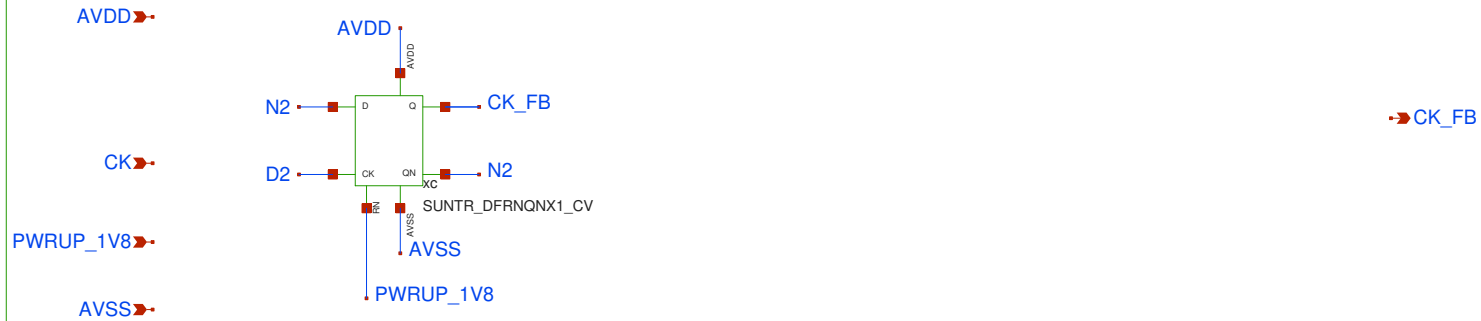
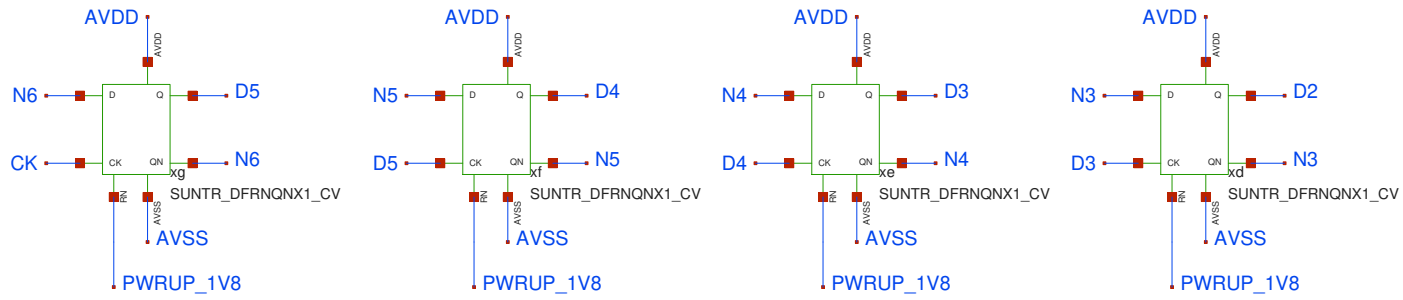
16 MHz x 32 = 512 MHz PLL



Ring oscillator with level shifter.



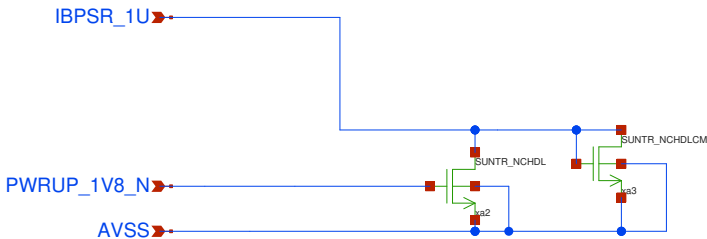
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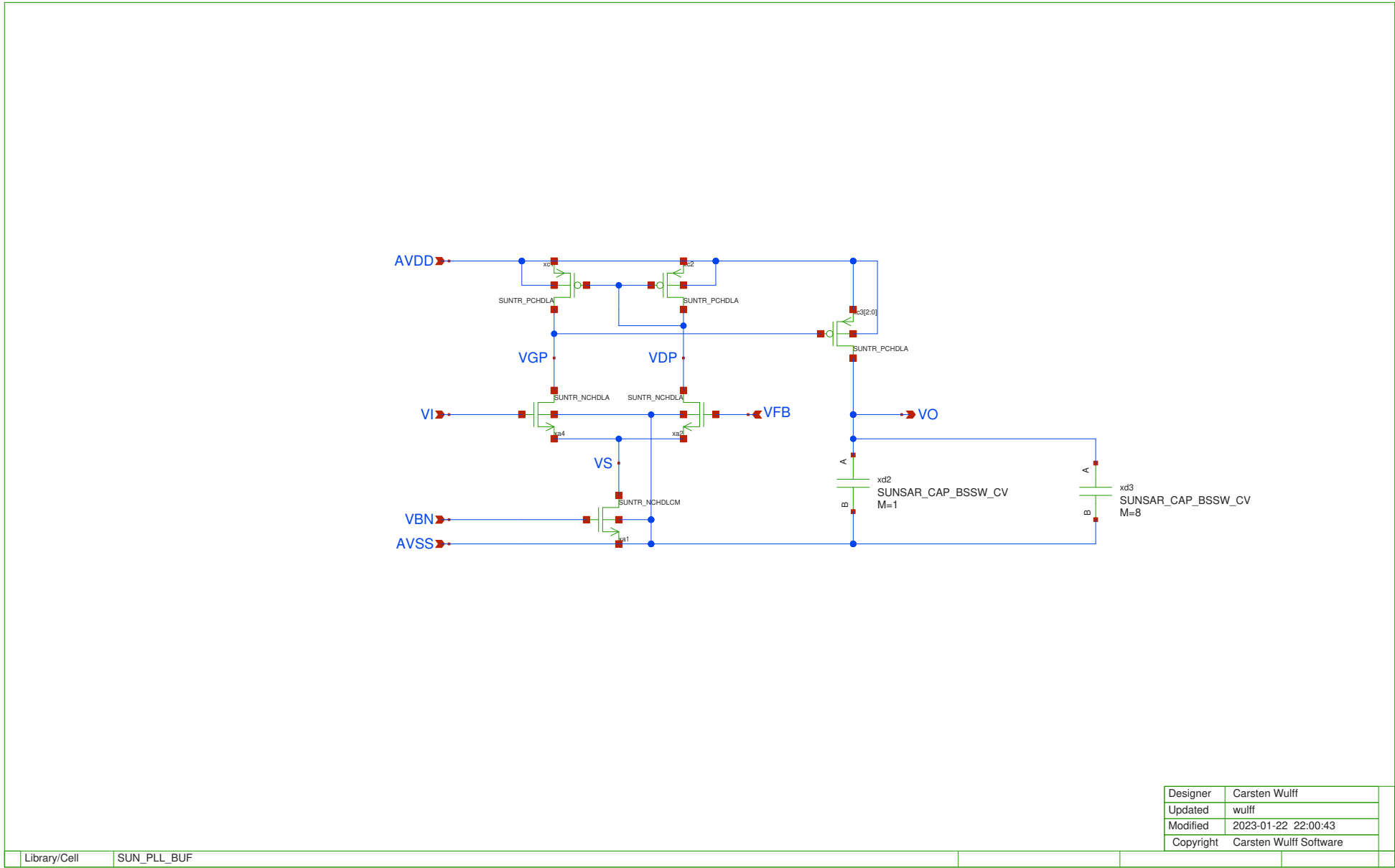
Divide by 32

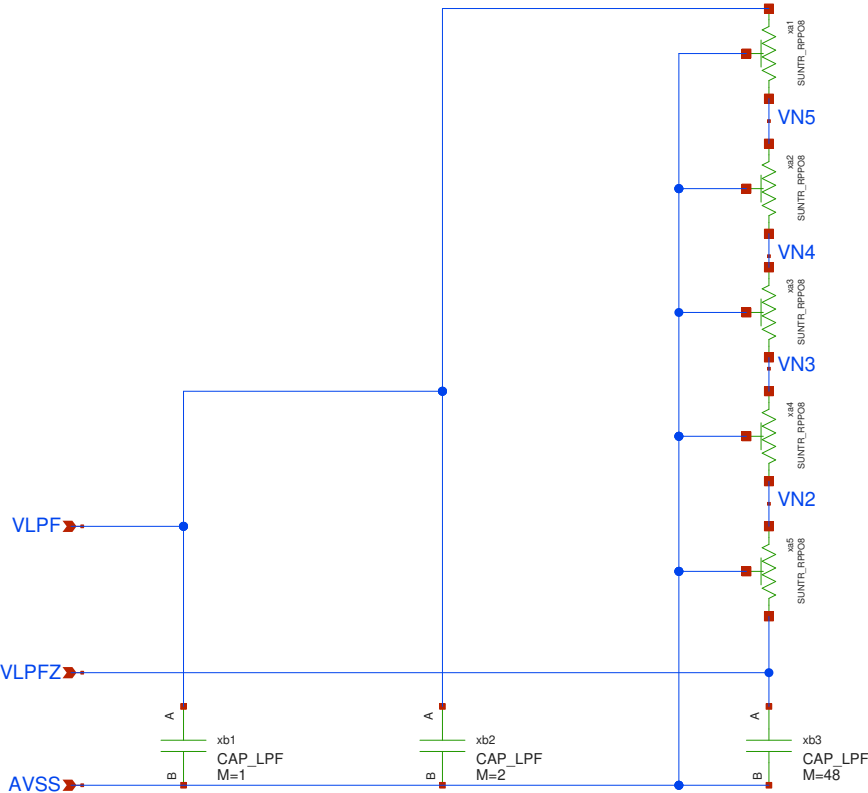
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Current bias



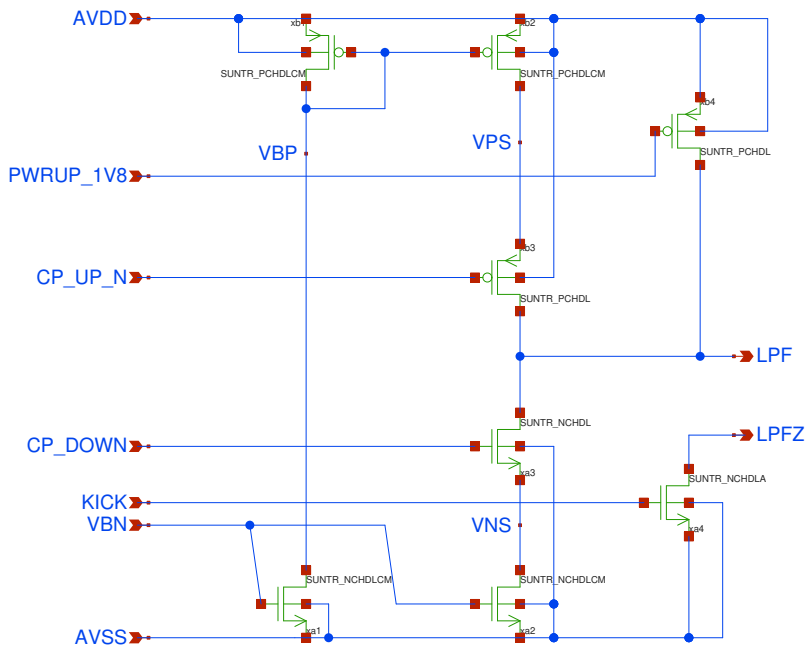
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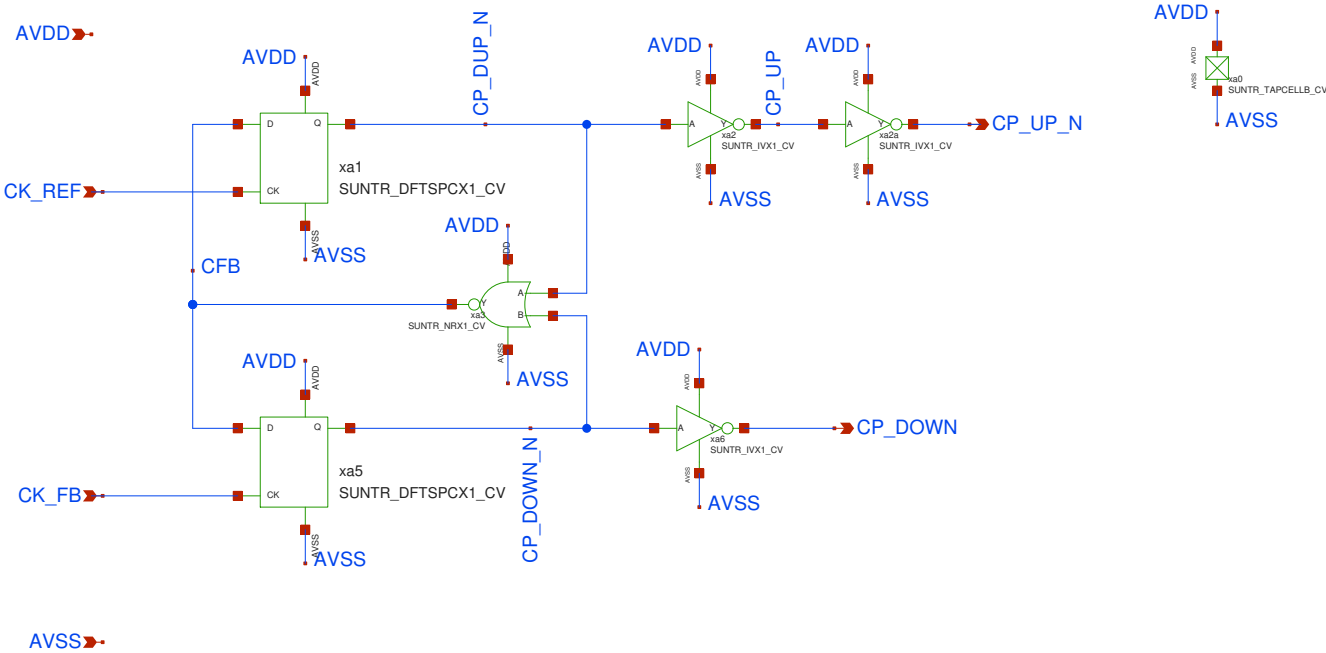
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Charge pump

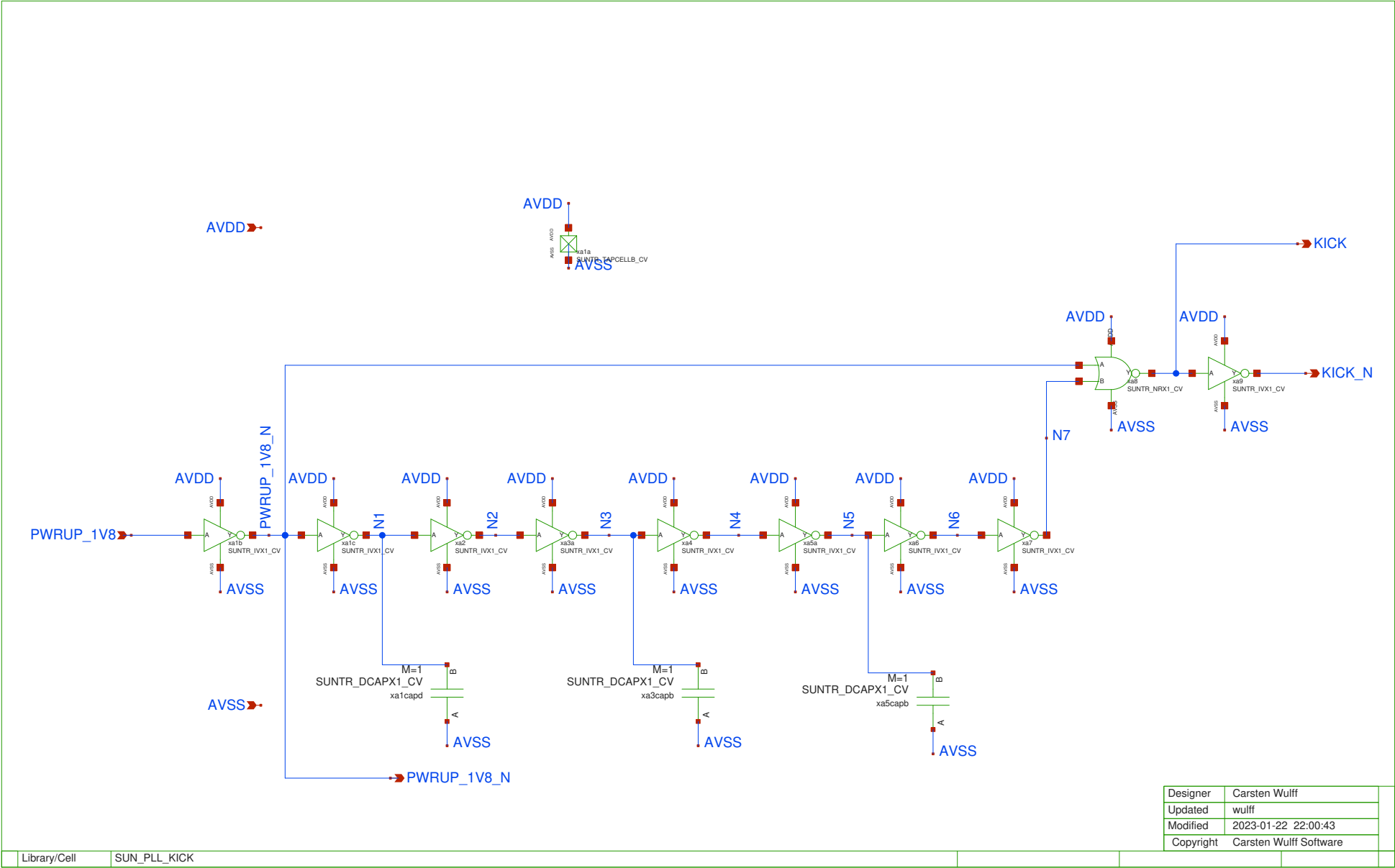


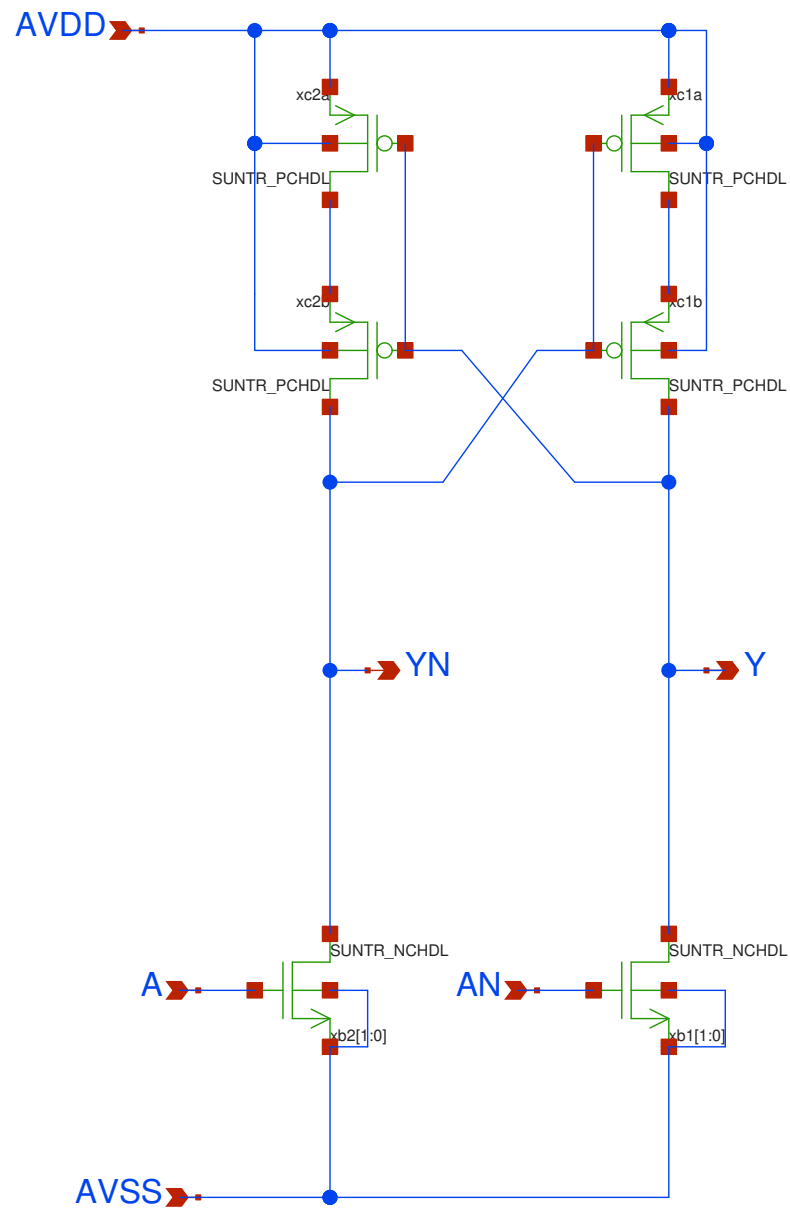
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Phase-Frequency Detector (PFD)



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Thanks!!