Faculty of Engineering and Applied Sciences

BS: Bio Medical Engineering

Department of Bio Medical Engineering

Digital Logic Design Project

Submitted By:

Zahra Batool

Engr. Zahra Batool

Objective

Designing a traffic signal using logic gates as combinational logic circuit and flip flops

Equipment

Multisim software

Theory

Traffic lights are used to control the vehicular traffic, making it easier for drivers and pedestrians. In a two-way traffic, traffic lights will be present on two sides. This controls six lights (two red, two yellow and two green) for two-way traffic. When a red light is displayed (ON) on one way, a green light will be displayed (ON) automatically on the other side. The yellow light (amber) will act as a caution to drivers that the signal is going to open (green light) or close (red) on their side signifying vehicles what to do next. This helps to control the flow of traffic more efficiently. It is based on two way traffic system at an intersection. Since it is an intersection, there will be four situations that is:

- When the first road is open for traffic (green), the second road is closed for traffic (red).
- when the first road open for traffic, displays amber (yellow) to halt traffic at that road, the second road is still closed for traffic (red) waiting to let traffic stop on first road.
- When the first road stops traffic (red), the second road signals (yellow) the drivers about the traffic will open on their road.
- When first road is closed for traffic (red), the second road is open for traffic (green)

In D flip flops, when the clock impulse is enabled, enable acts as positive edge and when clock impulse is disabled, it will remain as of its previous state.

According to requirement, Boolean expression required to transfer input data to D flip flops:

$\overline{A} = \overline{A}B + A\overline{B} = A \oplus B$

$\overline{B} = \overline{B}t + \overline{A}\overline{B}\,\bar{x}y + A\overline{B}x\bar{y}$

According to requirement, Boolean expression required to display output:

Red1	Yellow1	Green1	Red2	Yellow2	Green2
$\overline{A}\,\overline{B}$	$\overline{A}B$	A	$A\overline{B}$	AB	$\overline{A}$

Procedure

On Multisim

1. On opening the Multisim software, select Place and then, select Component (use this window for selection of all the components).
2. Select <All groups> and type component

- 74LS04N to select six NOT gates
- 74LS86N to select a XOR gate of two inputs
- 74LS00N to select four NAND gates of two inputs
- 74LS10N to select two NAND gates of three inputs
- 74LS08N to select four AND gates of two inputs.
- 7474N to select two D flip flops
- TRAFFIC_LIGHT_SIGNAL to select two traffic lights

3. Select the Sources group and from POWER_SOURCES, select two VCC of 5V and two grounds. In the same group, from SIGNAL_VOLTAGE_SOURCES, select CLOCK_VOLTAGE.
4. Select Basic, then select Switch to select five SPDT switches. Flip the switches horizontally and place them (S1, S2, S3, S4 and S5) vertically parallel to each other and join them by connecting lines. Ground all five from one of their terminals.
5. A VCC is given between the heads of the switches. By this, the DC voltage of 5V approaches the switches.
6. Make four sets of two pathways such that one is a simple wire (1) and the other has a NOT gate on it (complement - 0). Connect S1, S2, S3 and S4 to such set of pathway respectively. Connect S5 to a simple wire.
7. Let first set be A (connected to S1), second set be B (connected to S2), third set be x (connected to S3), fourth set be y (connected to S4) and let S5 connection to wire be t.
8. Connect the input 1 of the XOR gate to the first set of pathways and its input 2 to simple wire of set B.
9. Connect input 1 of first NAND gate with three inputs to complement of A, input 2 to complement of B and input 3 to simple wire of y. Connect input 1 of second NAND gate with three inputs to simple wire of A, input 2 to simple wire of x and input 3 to complement of y.
10. Connect outputs of both NAND gates with three inputs as input 1 and 2 of the first NAND gate with two inputs.
11. Connect output of first NAND gate with two inputs, as input 1 of the second NAND gate with two inputs and its input 2 is connected to the complement of B.
12. Connect input 1 of the third NAND gate with two inputs, to complement of B and its input 2 to simple wire t.
13. Connect the output of the second and third NAND gates with two inputs as input 1 and 2 to the fourth NAND gate with two inputs.
14. Place the two D flip flops and provide a VCC connection to the set (PR) of the first D flip flop and the reset (CLR) of the second D flip flop.

15. Connect the reset (CLR) of first D flip flop and the set (PR) of the second D flip flop together and provide them VCC as well.
16. Set the Clock Voltage (clock impulse) at a frequency of 1 kHz, duty cycle of 50% and voltage of 5V.
17. Provide the clock voltage to the clock impulse of both D flip flops. Ground the clock voltage from other terminal.
18. Connect output of the XOR gate to D1 (data) of the first D flip flop and output of the fourth NAND gate of two inputs to D2 (data) of the second D flip flop.
19. The output (Q complement) is detached is both flip flops.
20. Each flip flop is attached to two AND gates with two inputs.
21. First AND Gate - The output from the first D flip flop is connected to a NOT gate (complement) and then connected to input 1 of the first AND gate. Its input 2 is connected to the output of the second D flip flop that is complemented by the NOT gate.
22. Second AND Gate - The output from the first D flip flop is connected to a NOT gate (complement) and then connected to input 1 of the second AND gate. Its input 2 is connected to the output of the second D flip flop.
23. Third AND Gate – The output from the first D flip flop is connected to input 1 of the third AND gate. Its input 2 is connected to the output of the second D flip flop that is complemented by the NOT gate.
24. Fourth AND Gate - The output from the first D flip flop is connected to input 1 of the fourth AND gate. Its input 2 is connected to the output of the second D flip flop.
25. Select Indicators, then select probe to select 2 red probes (PROBE_RED), 2 yellow probes (PROBE_YELLOW) and 2 green probes (PROBE_GREEN). Each probe is attached to the output of the 8 NAND gates.
26. Attach first red probe to output of first AND gate, first yellow probe to output of second AND gate and first green probe to output of the first D flip flop.
27. Attach second red probe to output of third AND gate, second yellow probe to output of the fourth AND gate and second green probe to output of the first D flip flop that is complemented by the NOT gate.
28. Connect first traffic light to first red, yellow and green probes respectively and then, connect second traffic light to second red, yellow and green probes.
29. Run the simulation.

Observation

1. For the representation of traffic lights at the intersection/two way traffic

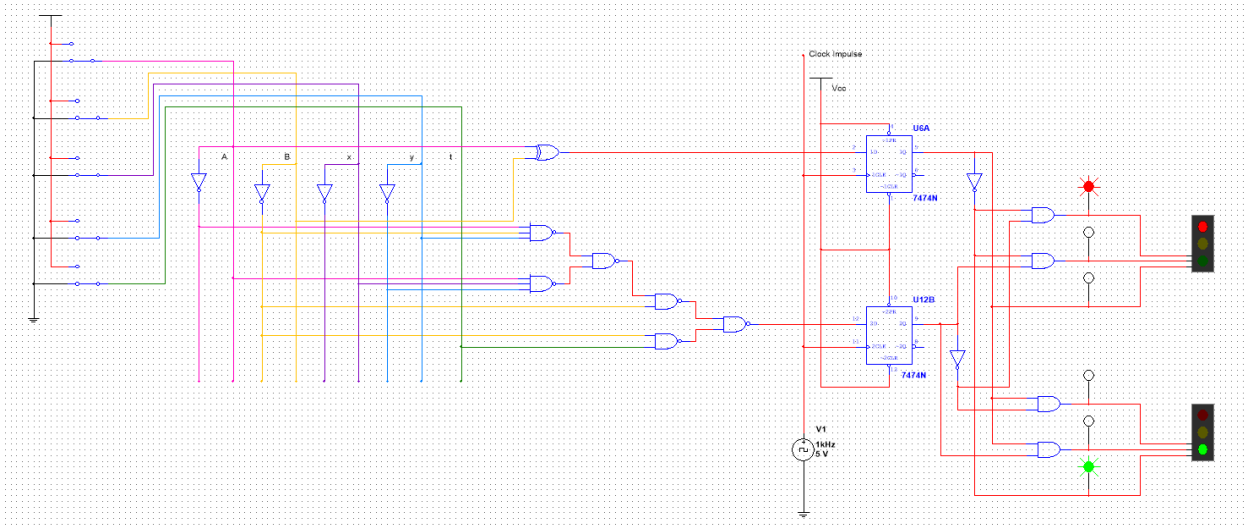
Inputs		Outputs					
A	**B**	**RED1**	**YELLOW1**	**GREEN1**	**RED2**	**YELLOW2**	**GREEN2**
0	0	0	0	1	1	0	0
0	1	0	1	0	1	0	0
1	0	1	0	0	0	0	1
1	1	1	0	0	0	1	0

2. To give proper input on the D flip flop

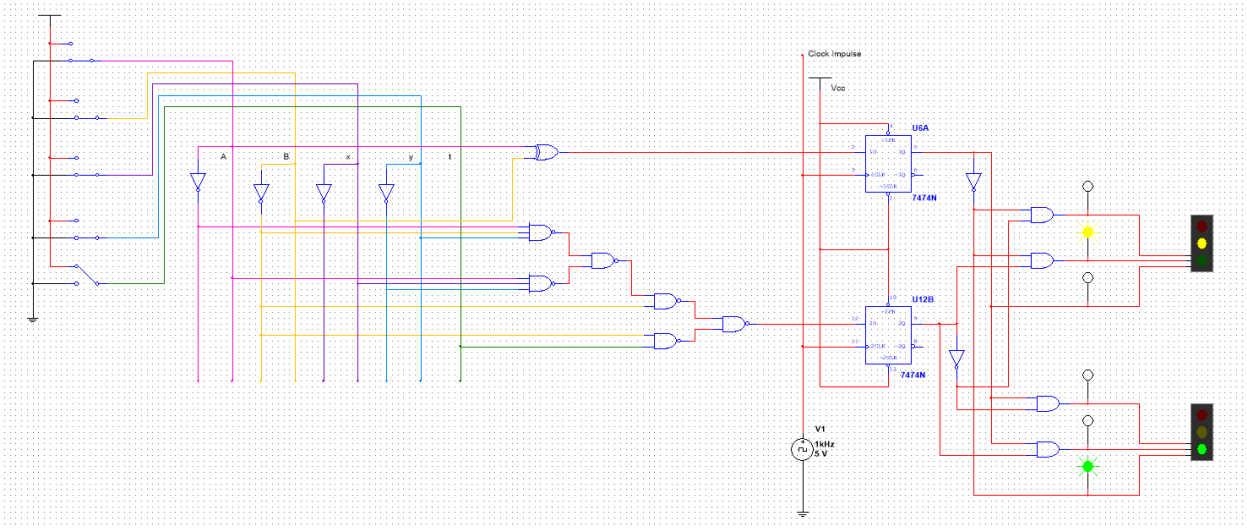
Truth table with D Flip-Flops								
Present States		**Inputs**			**Next States**		**Flip-Flop Input**	
A	B	x	y	t	$\overline{A}$	$\overline{B}$	D1	D2
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	1
0	0	0	1	0	0	1	0	1
0	0	0	1	1	0	1	0	1
0	0	1	0	0	0	0	0	0
0	0	1	0	1	0	1	0	1
0	0	1	1	0	0	0	0	0
0	0	1	1	1	0	1	0	1
0	1	X	X	X	1	0	1	0
1	0	0	0	0	1	0	1	0
1	0	0	0	1	1	1	1	1
1	0	0	1	0	1	0	1	0
1	0	0	1	1	1	1	1	1
1	0	1	0	0	1	1	1	1
1	0	1	0	1	1	1	1	1
1	0	1	1	0	1	0	1	0
1	0	1	1	1	1	1	1	1
1	1	X	X	X	0	0	0	0

MULTISIM

When input applied according to truth table:

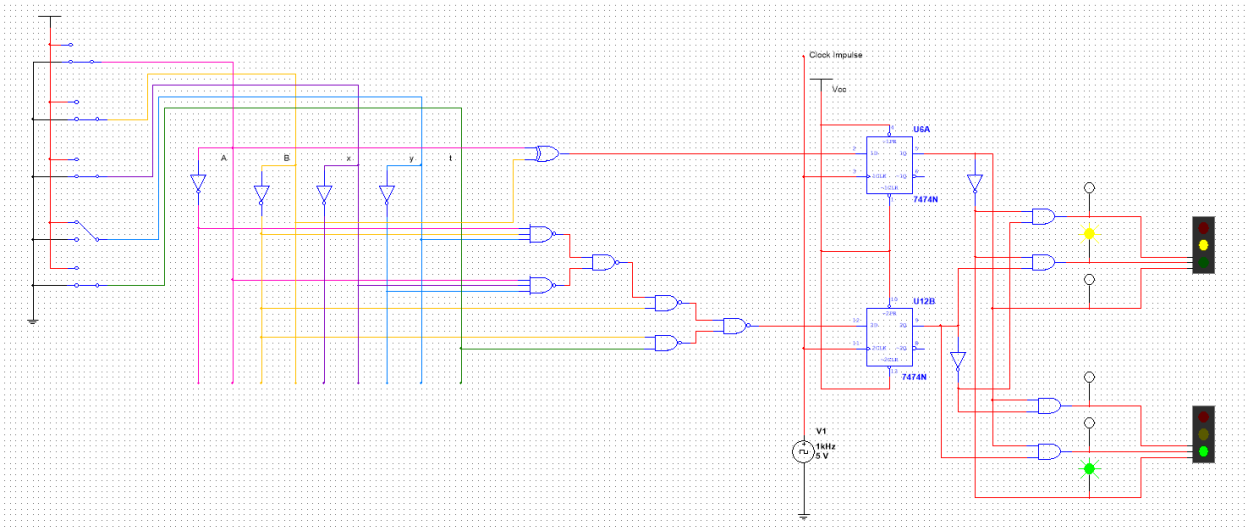


S1, S2, S3, S4 and S5 are OFF

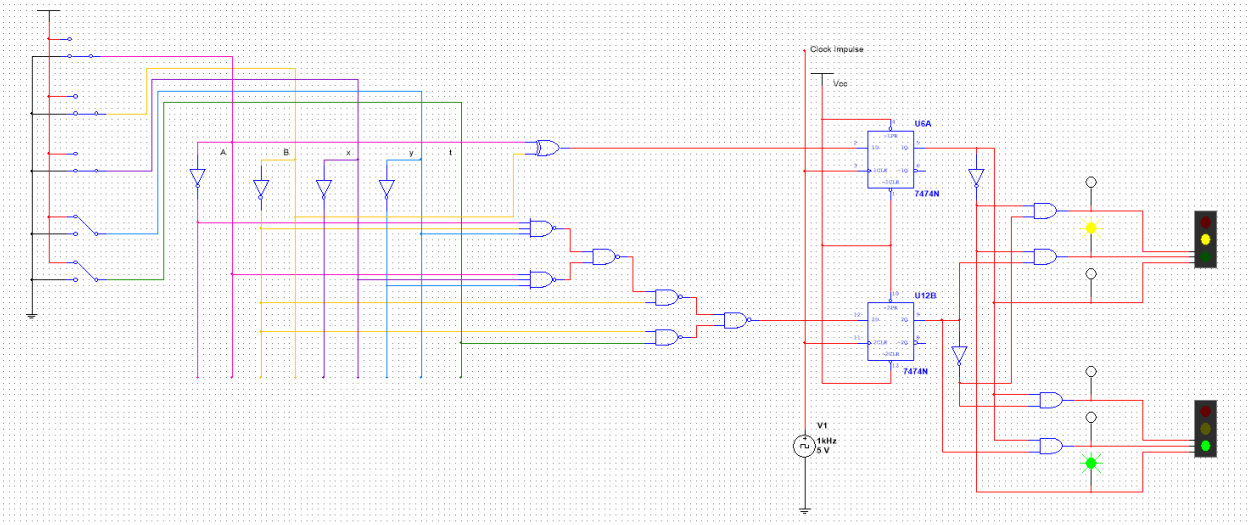


S1, S2, S3, S4 are OFF and S5 is ON

Engr. Zahra Batool

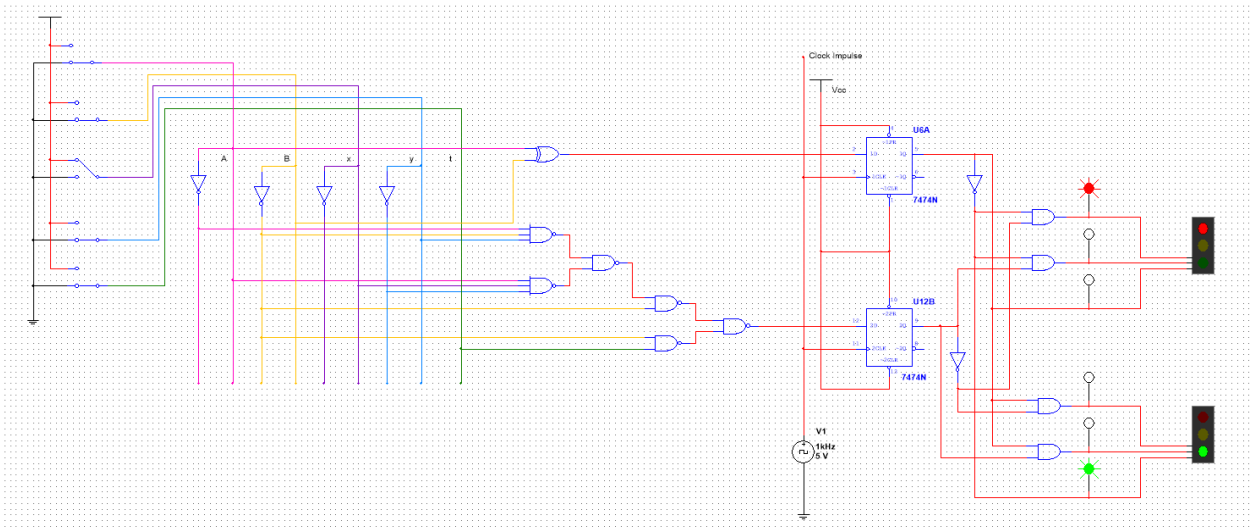


S1, S2, S3 and S5 are OFF and S4 is ON

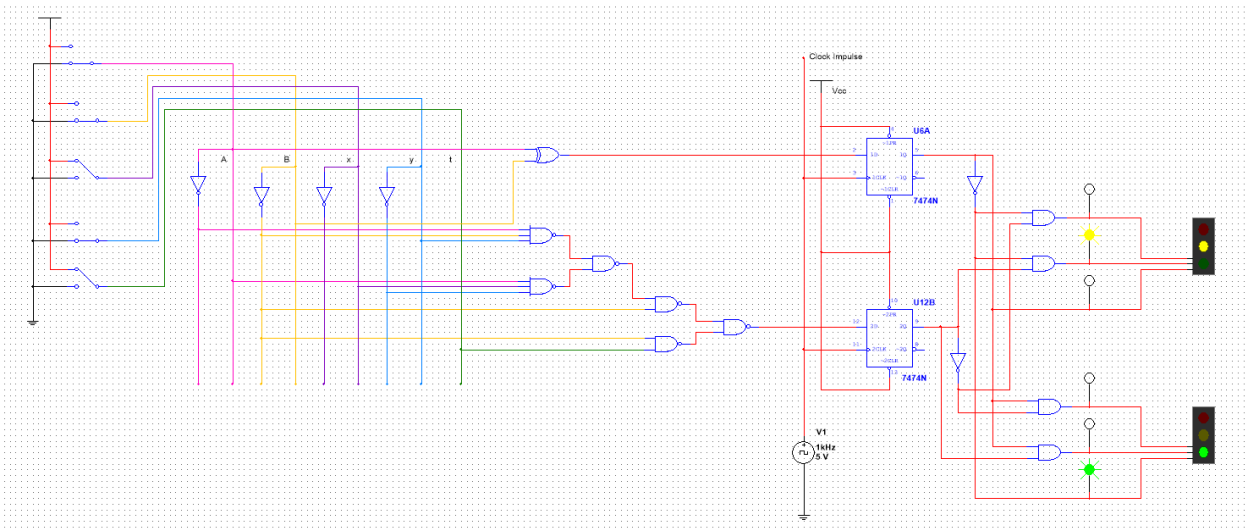


S1, S2 and S3 are OFF & S4 and S5 are ON

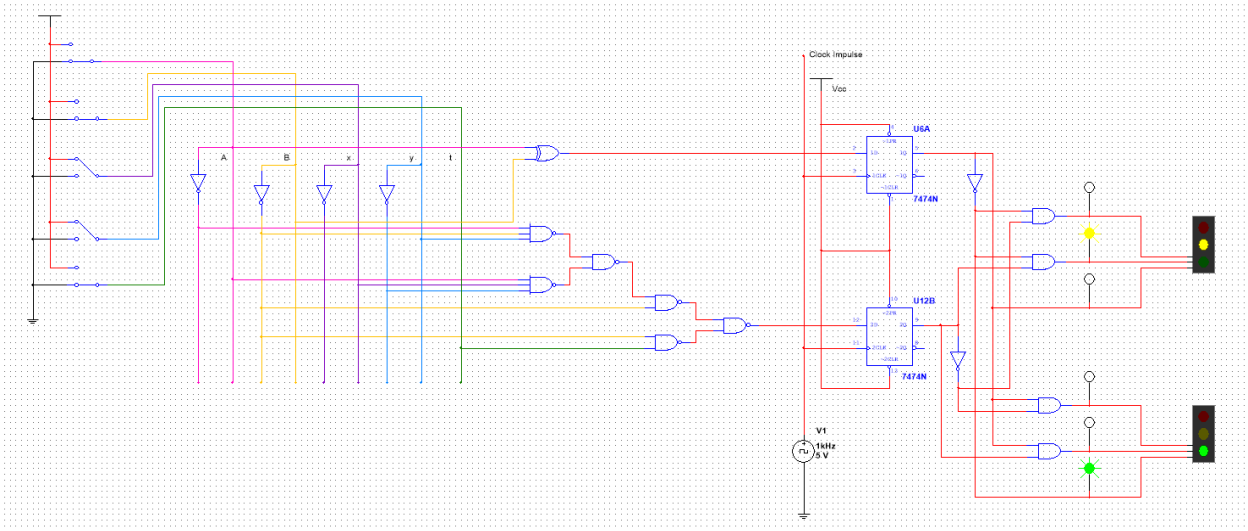
Engr. Zahra Batool



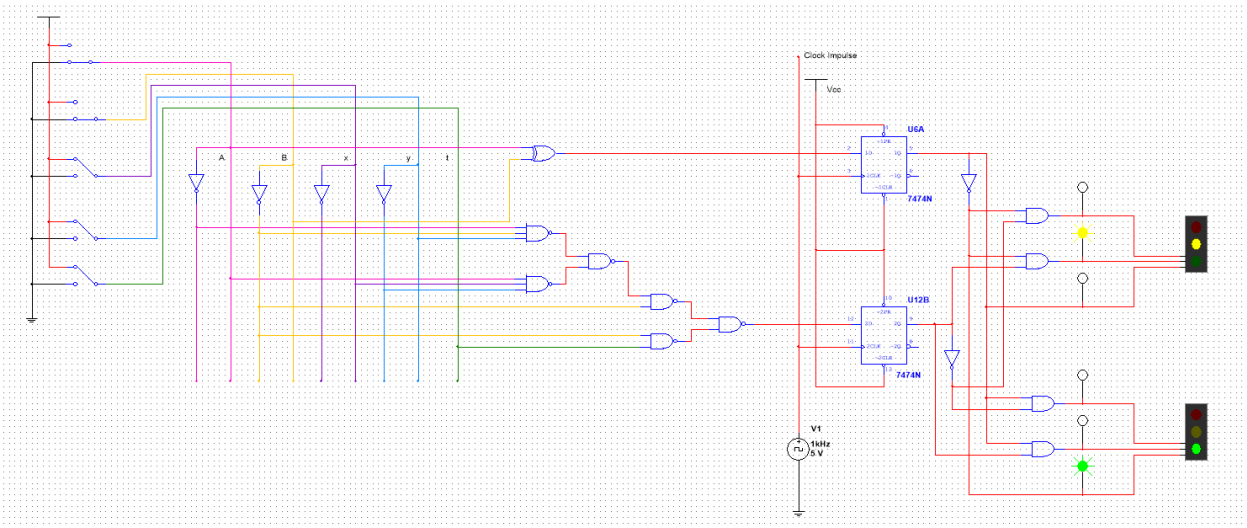
S1, S2, S4 and S5 are OFF & S3 is ON



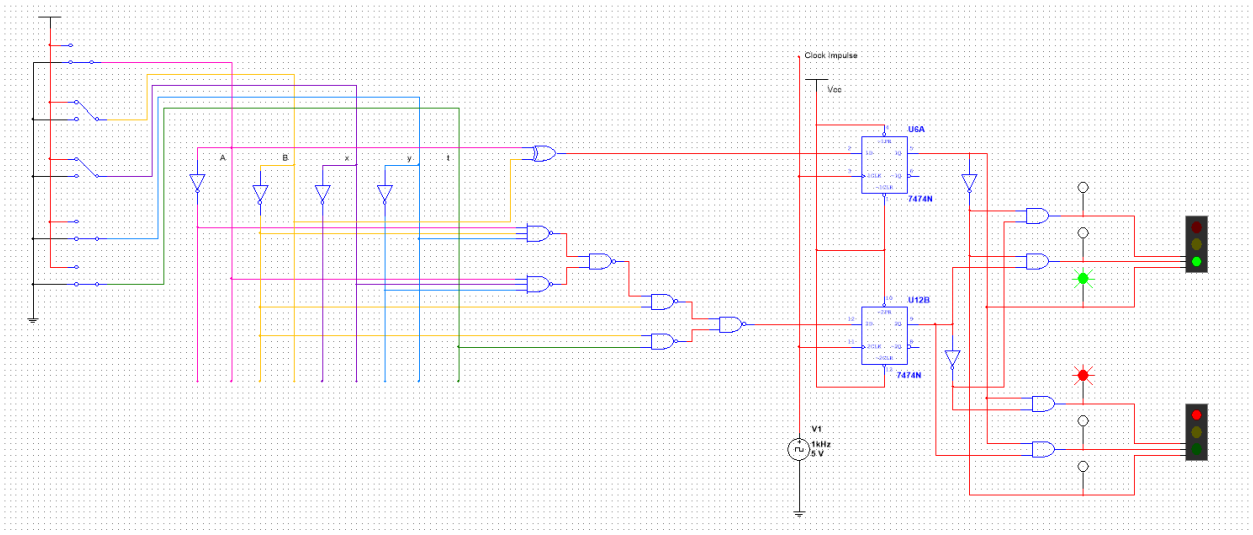
S1, S2 and S4 are OFF & S3 and S5 are ON



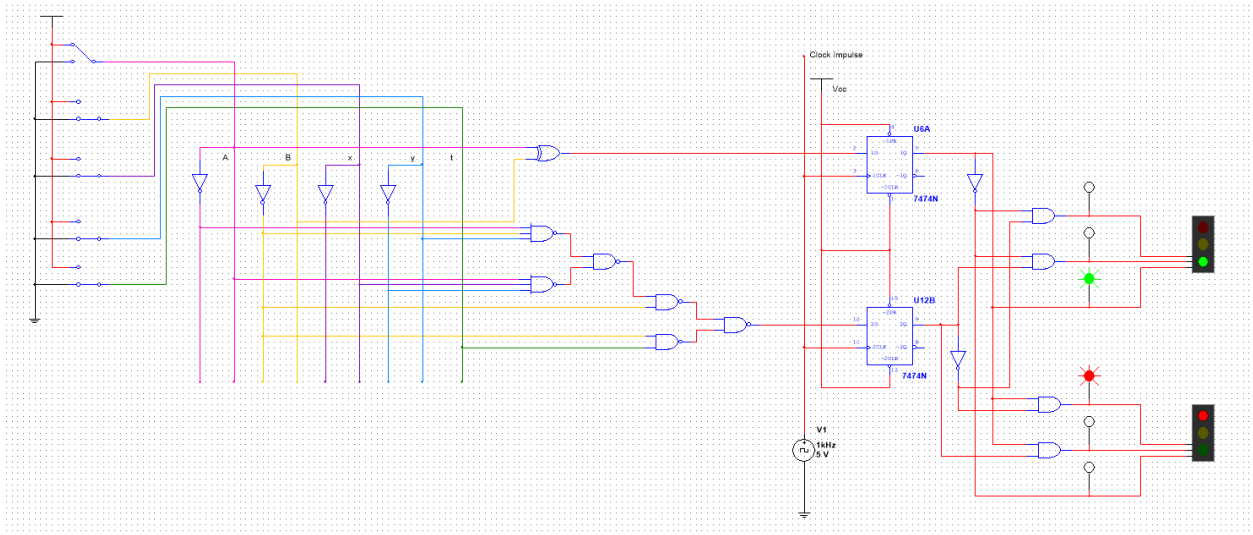
S1, S2 and S5 are OFF & S3 and S4 are ON



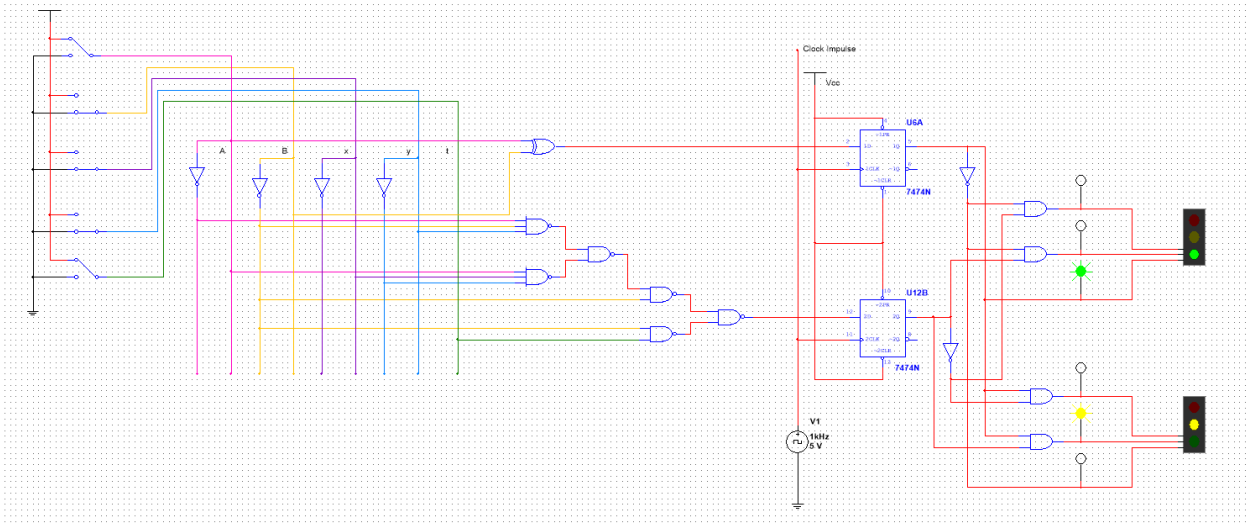
S1 and S2 are OFF & S3, S4 and S5 are ON



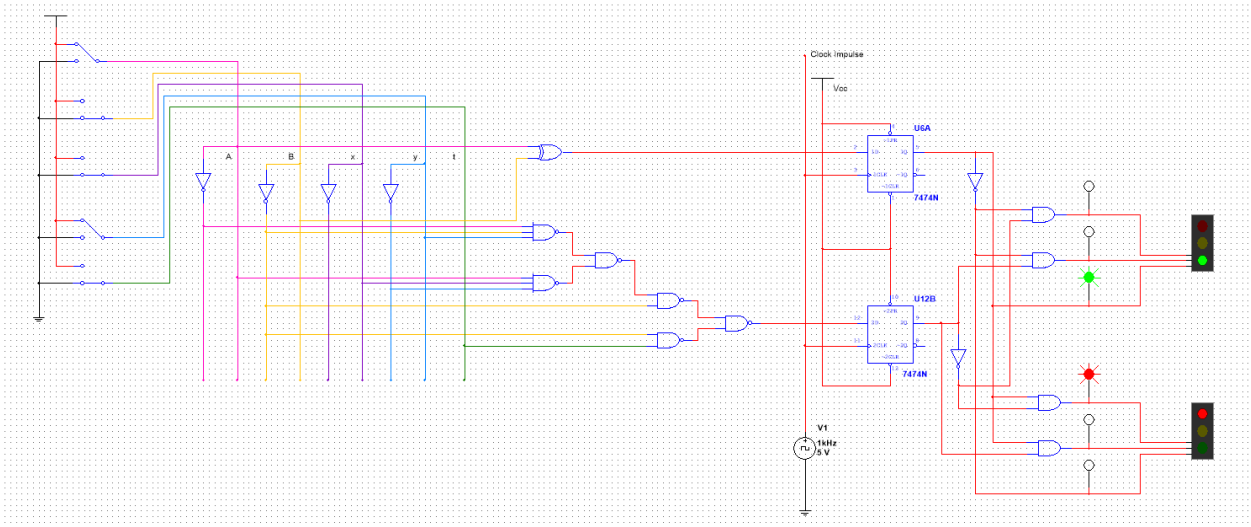
When S1 is 0 but S2 is 1, data to flip flop remains same. So output is also same



S1 is ON & S2, S3, S4 and S5 are OFF

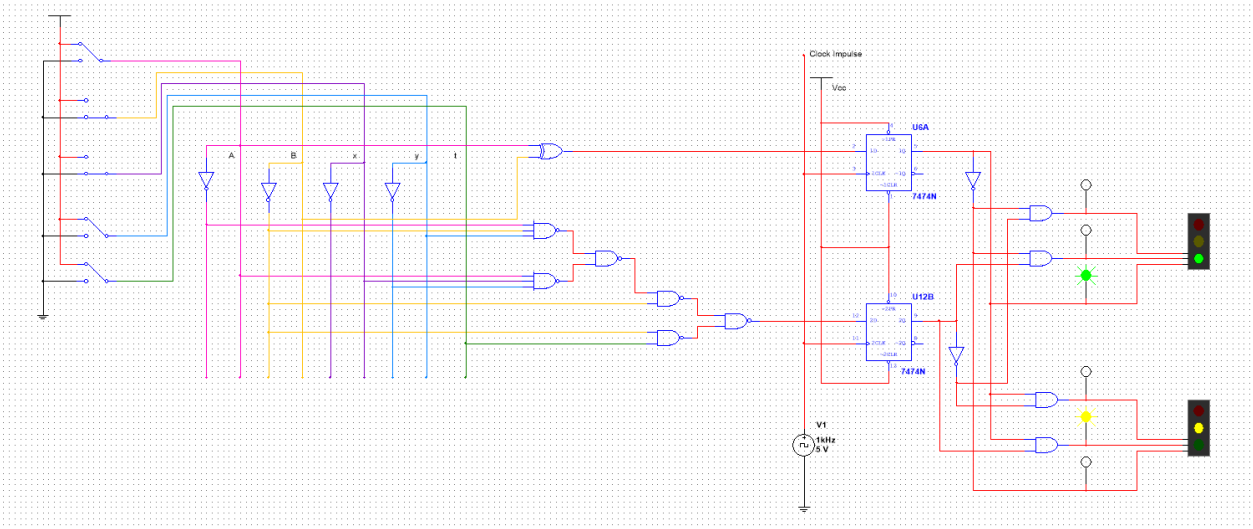


S1 and S5 are ON & S2, S3 and S4 are OFF

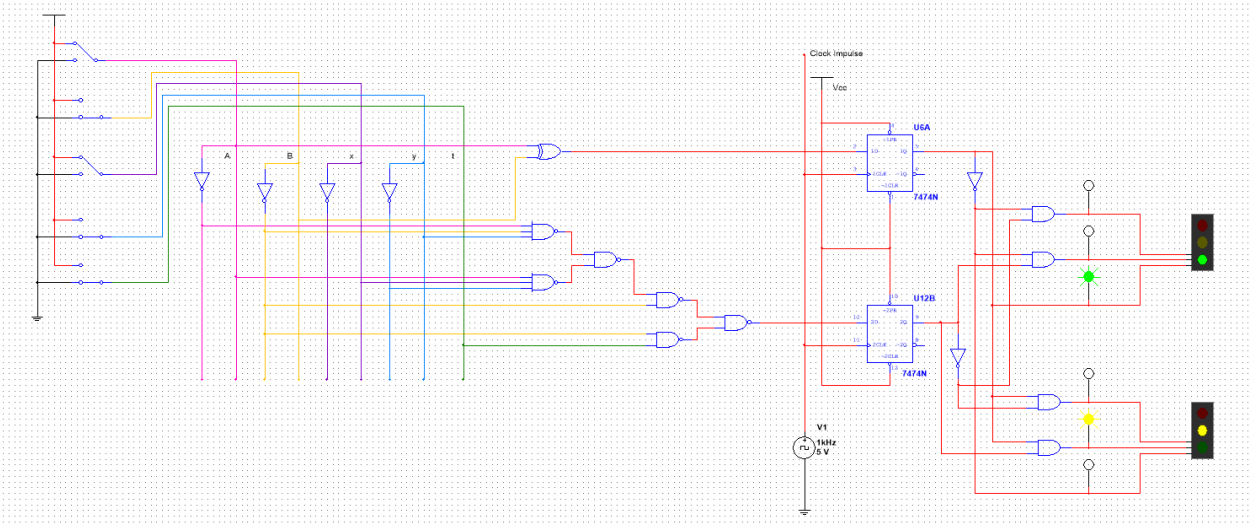


S1 and S4 are ON & S2, S3 and S5 are OFF

Engr. Zahra Batool

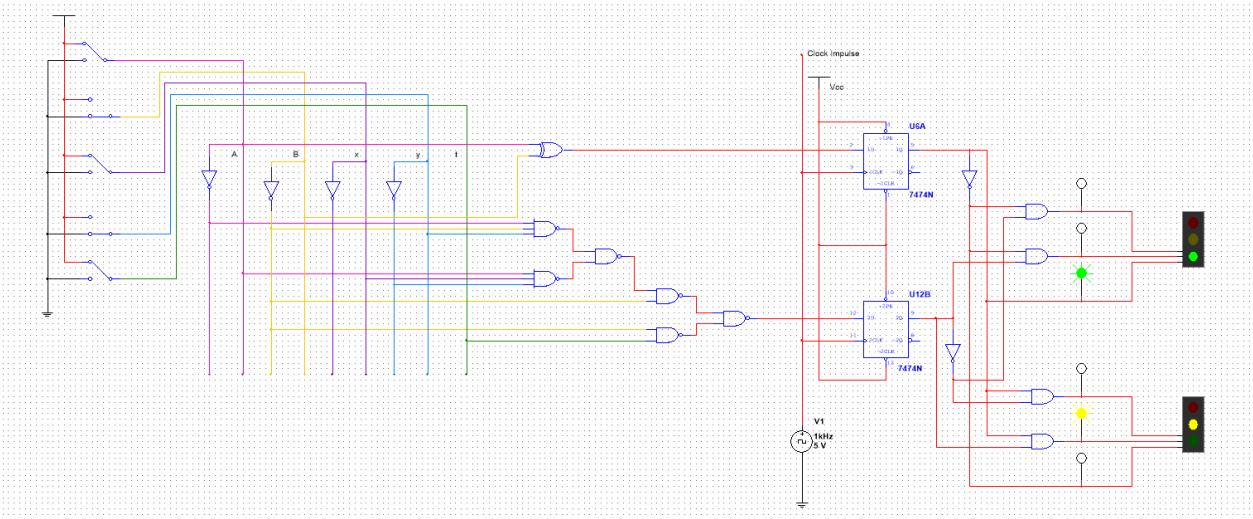


S1, S4 and S5 are ON & S2 and S3 are OFF

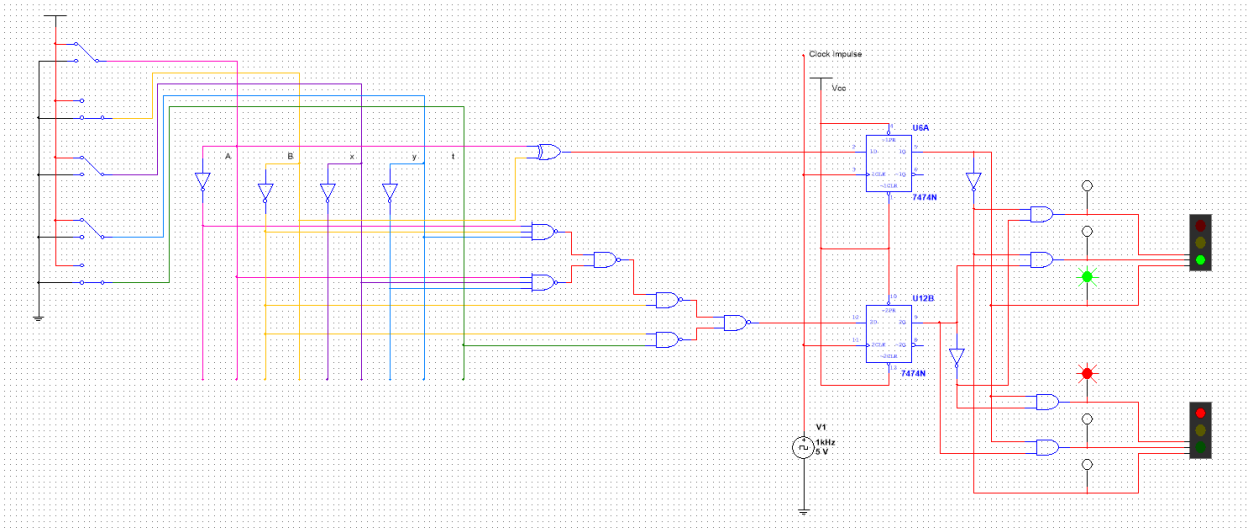


S1 and S3 are ON & S2, S4 and S5 are OFF

Engr. Zahra Batool

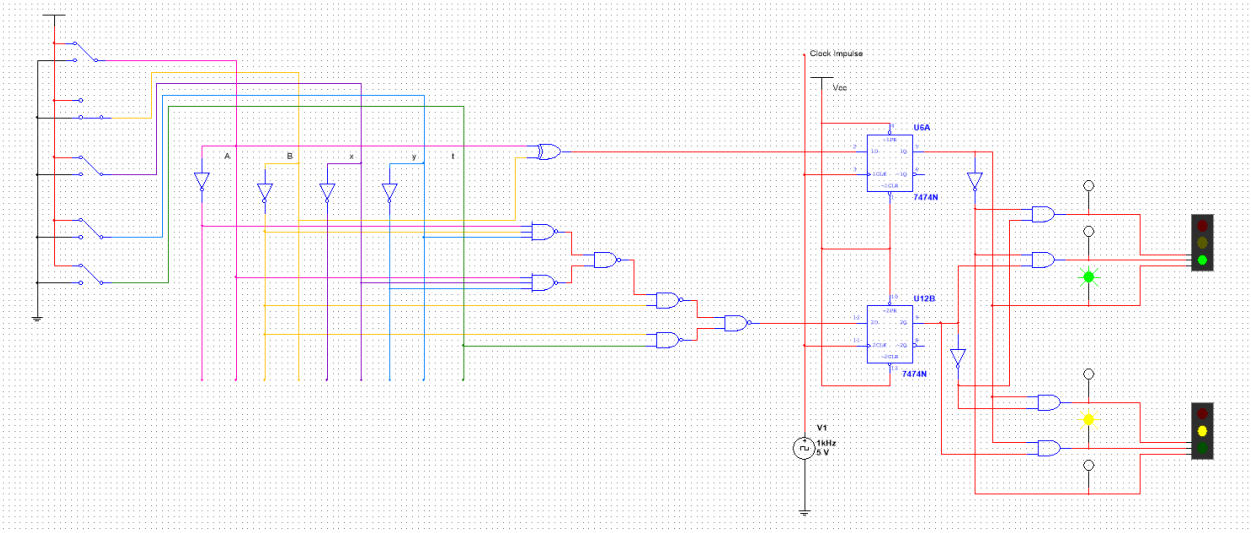


S1, S3 and S5 are ON & S2 and S4 are OFF

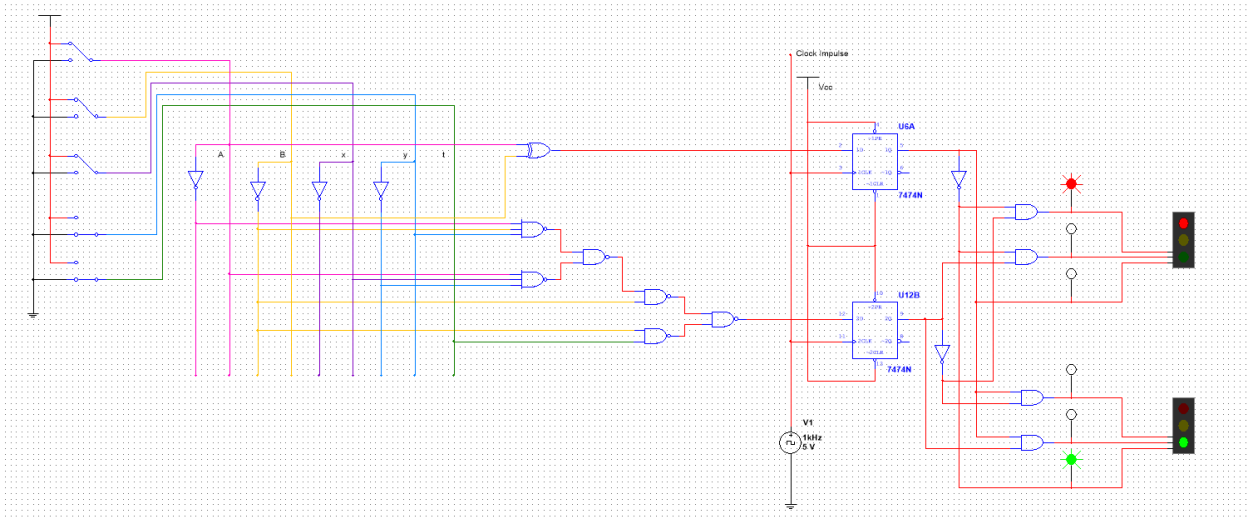


S1, S3 and S4 are ON & S2 and S5 are OFF

Engr. Zahra Batool



S1, S3, S4 and S5 are ON & S2 is OFF



When S1 is 1 and S2 is also 1, data to flip flop remains same. So output is also same

Conclusion

This project displayed the two-way traffic system when different inputs given manually, gives the proper output as observed on the traffic lights. The clock impulse connected to the D flip-flop decides the logic provided to the D flip flop. All four situations mentioned above are satisfied.