

A Review on High Performance Architecture for Packet Classification for Secure Communication Network

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Abstract- Packet Classification is a core function used in an internet router, firewall, network security and quality of services. Packet classification technique is very crucial since various unauthorized and malicious networks are being exposed to. For secure networking and avoiding unauthorized access, incoming packets flow based on predefined rules available in a classifier. Available software solution's performance is not efficient for wire speed processing in high speed networks. To meet the line-card requirement and wire speed processing hardware solution is more efficient and secure than software solution. For implementing hardware architecture for wire speed processing different algorithms have been proposed. This paper presents review on different algorithm and technique used to implement packet classification architecture. High performance packet classification architecture can be implemented using Field programmable gate array (FPGA) and large number of rules can be stored using on-chip memory resource of FPGA.

Index Terms- Packet classification, 5-tuple, Quality of services, latency, throughput.

I. INTRODUCTION

Modern packet processing system uses technique known as packet classification in place of de-multiplexing due to various advantages like high speed and ability to cross multiple layers. Various services like firewalls, Virtual Private Network (VPN), network security, policy-based-routing, traffic shaping and Quality of Services (QoS) require packet classification. This makes packet classification an integrated part of network intrusion detection system (NIDS) [7-11]. To access various services, it is required to figure out which rule matches with incoming packet and depending on it necessary action is taken. In other words, flows are decided by rules applied to incoming packets and

each rule in a rule-set specifies a flow to which a packet may belong based on values in header fields. Packet classification process involves inspection of multiple fields against a rule-set may be containing thousands of rules. This is one of the challenge and difficulty in the process of classification [8]. Each rule in a classifier has a priority and action is taken according to their priority. Basic 5-tuple are present in the standard packets header which include destination and source IP address field, destination and source port number field and the protocol type field as depicted in figure.1. For different combination of values of the fields require different matches like prefix match for destination and source IP address field, range match for destination and source port field and exact match for protocol field [11]. For better performance, packet classification system must support all the type of match [14-16].

| Source Address | Destination Address | Source Port | Destination Port | Protocol |
|----------------|---------------------|-------------|------------------|----------|
| 32 Bit | 32 bit | 16 bit | 16 bit | 8 bit |

Figure.1 Standard 5-tuple packet header fields

Considering the fact that packet classification system is the central part of firewalls, internet routers and various intrusion detection systems. Various packet classification algorithms have been proposed to perform packet classification; just because of special computational method most of the existing algorithms may not be suitable for hardware implementation. The main performance metrics that should be taken into an account while designing algorithms for implementing hardware packet classification system are as follow:

- Memory requirement: memory requirement for storing number of rules is limited in hardware solution. The on-chip SRAM of FPGAs can be used to store large number of rules.
- Multi match classification: packet classification algorithm should support exact match, prefix

match and range match. It should also avoid the use of prefix to range match conversion which is memory inefficient.

High speed: algorithm must meet the in-line requirement of 100/200/400 Gbps while supporting large number of rules.

Update, modify and delete rules: Dynamic modification, updating and removing of out-dates rules is required for supporting various new applications.

Latency: low latency application requires parallel orientation in cost of memory while in some application series orientation is feasible. It is important that algorithm should be flexible in orientation for supporting all types of application.

Above performance matrices are very crucial while designing hardware packet classification architecture to avoid degradation of performance of the architecture. However, performance of architecture depends on an algorithm used for designing it. INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN TECHNOLOGY reserves the right to do the final formatting of your paper.

II. DETAIL STUDY ON PACKET CLASSIFICATION TECHNIQUES

From literature survey and review of related work, it is observed that researchers have designed the packet classification architecture using algorithms based on these four methods: exhaustive search, decision tree based, tuple search and decomposition based method. Decision tree based approach and decomposition based approach are desirable for hardware implementation of packet classification system. Efforts have been undertaken by researchers for designing of multi-match packet classification architecture for firewalls and all type of intrusion detection systems. Researchers put their best to implement hardware solution for packet classification.

For one-dimensional packet classification, Ternary Content Addressable Memory (TCAM) is the desirable hardware solution because of its simple management and speed. To check all fields at a time used. For multi-dimensional packet classification

using TCAM, Yen-Kuan Chang and Cheng-Chien Su have proposed an efficient range-encoding Scheme for Packet Classification using Gray code [3]. Experimental result's shows the proposed binary reflected gray code-based (BRGC) encoding scheme requires less TCAM storage than parallel packet classification encoding (PPCE) scheme. The BRGC based encoding scheme is proposed for range values of source and destination port number but it is also used for source and destination address field of packets having prefix addresses. Problems like limited scalability and the range to prefix blowout for large number of rule-set have solved using BRGC based encoding scheme.

Lu Sun, Hoang Le, Viktor K. Prasanna have proposed optimizing decomposition-based packet classification on FPGA [4]. Decomposition-based IP classification algorithms consist of two phase: in first phase, independent searches are performed on each field of packets, while in second phase: results from the first phase are combined. Due to limited resources and limited on-chip memory on FPGAs, the second phase of the decomposition based algorithms become challenging. To solve this problem they have proposed a systolic-array-based architecture which efficiently combines the results of the first phase in the second phase. The proposed architecture on set intersection and compact representation of matching rules yields better performance in second phase of the algorithm. The design is more efficient, feasible and attractive in logic resources, in handling large rulesets and in area than any other decomposition based algorithm. The proposed architecture has implemented on Xilinx Virtex-6 XC6VLX760 with -2 speed grade as a target in Verilog using Xilinx ISE 12.4 tool. The implemented design achieves high throughput of 107 Gbps while supporting rules upto 64K of minimum packet size of 80 bytes.

Weirong Jiang and Victor K. Prasanna have introduced Field-Split Parallel Bit Vector (FSBV) based architecture [2]. The FSBV architecture is suitable for Snort rule and it is a novel SRAM-based architecture which exploited the use of BlockRAMs of current FPGA. It supports multi match packet classification and also handles the negation and value list problem. The architecture is memory efficient because range to prefix conversion is not used for range values. Proposed architecture used TCAM algorithm for source and destination address fields,

CAM algorithm for protocol field and Bit Vector (BV) algorithm for source and destination port fields. The FSBV architecture achieved clock frequency of 167 MHz and processed two packets every clock cycle with the use of dual-port RAMs on a Xilinx Virtex-5 XC5VFX200T device. Using SRAM-based architecture and low memory requirement, one fourth power reduction can be achieved over BV-TCAM.

Researchers have developed various software solutions for packet classification, but hardware solutions yield high performance and supports dynamic updates. Yun R Qu, Shijie Zhou, and Viktor K. Prasanna have proposed a high performance 2-dimensional pipelined architecture for packet classification on FPGA which supports dynamic updates of rules [6]. The proposed architecture consists of self-reconfigurable processing elements. A modular processing element (PE) can handle range match as well as prefix match and does not need range to prefix conversion. Multiple modular processing elements (PEs) are used in the architecture to construct a 2-dimensional architecture for handling large number of rules. Striding and clustering technique is used in the implemented architecture to vary size of sub-field and number of rules. The architecture can perform packet classification of s-bit subfield against a set of n rules using striding and clustering technique. A set of algorithm supports modification, deletion and insertion operations on the proposed architecture. Dynamic updatable of rules on hardware is possible without deteriorating the pipeline performance. The architecture is scalable with respect to large input length. The Proposed architecture maintains very high clock frequency of 324 MHz and can achieve throughput of 190 Gbps with 1K 15-tuple rule-set on Virtex-6 XC6VLX760 FGQ1760-2 FPGA device.

A scalable and modular architecture for high performance packet classification have been proposed by Thilan Ganegedara, Weirong Jiang, and Viktor K. Prasanna [1]. They have proposed a novel modular Bit-Vector based architecture on field programmable logic array (FPGA) using StrideBV algorithm. Range integration search in the architecture avoids the use of range-to-prefix conversion and supports all type of match. The priority encoder is used for extracting highest priority match. Proposed serial and parallel versions of

StrideBV based architecture are ruleset-feature independent solution. Their solution is flexible in orientation depending on an application and latency requirement. Proposed architecture is memory efficient, achieves 100+ Gbps throughput while supporting upto 28K rules using only on-chip resources. on a state-of-the-art Xilinx Virtex-7 2000T FPGA device and evaluates the performance of both serial and parallel version of strideBV using post place-and-route

III. CONCLUSION

Packet classification technique is very important to secure communication network and to avoid unauthorized access. Software based packet classification is not much efficient to meet wire speed requirement. So it is concluded that, hardware based packet classification will be required to meet wire speed requirements with low latency and high throughput. Literature survey has been done by studying various existing techniques with their advantages and disadvantages

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Design of High Performance Packet Classification Architecture for Secure Communication Networks Using VHDL

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Abstract— Packet classification is a crucial technique for secure communication and networking. Security tools and internet services use packet classification technique which involves checking of packets against predefined rules stored in a classifier. Performance of the available software solutions of classification is not desirable and efficient for wire speed processing in high speed networks. Ternary Content Addressable Memory (TCAM), Bit-Vector (BV), field split bit vector (FSBV) and StrideBV algorithm are hardware based packet classification algorithms. In this paper, we have proposed simple and memory efficient approach for packet filtering using Xnor gate instead of using lookup tables called XnorBV approach. Packet header fields of Internet protocol (IP) addresses and protocol layer are classified using Xnor gate against predefined ruleset which also support ternary bit pattern of '1', '0' and '*' while port numbers of packet header support range match by comparing port numbers against lower bound and upper bound. Our proposed parallel pipelined architecture can sustain a high throughput of +100 Gbps and low latency. Proposed method is memory efficient than other existing techniques, also supports prefix, range and exact match without use of range to prefix conversion. Also proposed XnorBV architecture is independent of ruleset feature and supports multiple dimension classification.

Index Terms—firewall; network intrusion detection system; packet classification; quality of services.

I. INTRODUCTION

A sequence of packets coming from the source system to a destination system is popularly labeled as traffic flow or packet flow and a sequence of packets from particular source to a particular destination is called a flow. A flow can be identified by using technique called packet classification which categorizes the incoming packets into different flows by inspecting values of header fields of packets within a certain time [1]. For identification and arranging packets into different flows, each incoming packet is checked against a set of rule [2], if an incoming packet is matched with any rule of a rule-set then only it is accepted otherwise rejected. After categorizing incoming packets into different classes, each flow can be processed differently to differentiate the services suggested for the user. Each application and service requested by the user requires packets of same class. Packet classification technique helps to provide respective packets to respective services efficiently using predefined rule-set. Also, various services like firewalls, Virtual private network, network security, policy-based-routing, traffic shaping and quality of services incorporated the packet classification technique to detect threats and to prevent unauthorized access to the network [3][4]. Due to these manifold advantages of packet classification technique in modern communication, packet classification has become an integrated part of all type of intrusion detection systems, firewalls, internet routers and virtual private networks[5].

Software solutions are available to perform classification of packets but they are insufficient for high speed network applications [4]. In software tools, classification is generally done by checking only port numbers or IP addresses or protocol layer. Performance of software solutions which support inspection of multiple fields is not desirable for wire speed processing. For wire-speed processing and secure networking, hardware solutions are desirable and classification of packets can be done by checking all fields of packet header. In hardware packet classification solution, multiple fields of an incoming packet are checked against each rule of a rule-set. A size of ruleset may vary from hundred to thousand rules. The challenge and difficulty for hardware implementation of packet classification system is memory requirement to store large number of rules [2]. Each rule in a classifier is stored in a decreasing order of their priority and action is taken according to their priority. Figure 1 depicted below shows a standard 5-tuple packet header having destination and source Internet Protocol (IP) address field, destination and source port number field and the protocol field [3]. For different combination of values of the fields require different matches like prefix match for destination and source Internet Protocol address field, range match for destination and source port field and exact match for protocol field.

| Source IP address | Destination IP address | Source port | Destination port | Protocol |
|-------------------|------------------------|-------------|------------------|----------|
|-------------------|------------------------|-------------|------------------|----------|

Figure 1: Standard 5-tuple packet header

Considering the fact that packet classification system is the central part of various security tools and applications over internet and computer systems [6]. Various packet classification methods have been proposed to perform classification of packets just because of special computational method and certain limitations most of the existing technique may not be suitable for hardware implementation. The main performance metrics that should be taken into account while designing algorithms and architecture for implementing hardware of packet classification system are summarized below [3] [4] [7]:-

- Memory requirement: memory requirement for storing number of rules is limited in hardware solution. The on-chip static random access memory of field programmable gate arrays (FPGA) can be used to store large number of rules.
- Multi match classification: packet classification algorithm should support exact match, prefix match and range match. It should also avoid the use of prefix to range match conversion which is memory inefficient.
- High speed: algorithm must meet the in-line requirement of 100/200/400 Gbps while supporting large number of rules.
- Latency: low latency application requires parallel orientation while in some application series orientation is feasible. It is important that algorithm should be flexible in orientation for supporting all types of applications.

II. PROBLEM IN PACKET CLASSIFICATION

Important issue of packet classification architecture is Power consumption. As throughputs of trillions of bits per second achieved by routers, power consumption becomes an increasingly critical concern. Power efficiency depends on number of rules used to classify incoming packet. This is one of aspect used for evaluation of power efficiency of packet classification system. The power consumed by the router to drive away the extremely large heat created by the router components extensively assist to the operating costs [8]. The power consumption in search engines is becoming an increasingly important evaluation parameter because each port of routers contains packet classification devices and router lookup [4].

Memory requirement is another important issue of packet classification. Nowadays, researchers aim to find out solutions for large ruleset. Method of classification and number of rules stored in classifier is related to amount of memory required. Due to limited resources available on FPGA, memory has become very important issue of hardware solution to support large number of rules [9].

Speed and pliability in specifications is another issue in packet classification devices. In packet classification process, packets are categorized based on a set of predefined rules also called as packet filters. Rules or filters define patterns that are to be matched against incoming packets for arranging packets for different flows [6] [10]. Packet filters or rules specify possible values for each field of a standard 5-tuple packet header [8] [11]. The address fields of a packet header are often used prefixes to define the addresses, although in address fields arbitrary bit masks are acceptable in a classifier or ruleset and this feature is widely used in real filter sets. Rules or Filters specify a range value for port-fields of packet header for matching incoming packets. Protocols can be in two ways either exact value or as a wildcard. Values specified by bit masks are allowed in some system for protocol field of incoming packet, even if it's not clear how convenient that feature is [8][12].

III. PROPOSED WORK

In this work, we performed classification of each field or tuple of incoming packet using Xnor gates instead of using look-up tables called XnorBV. A XNOR gate can be used as basic comparator for comparing two bits to make the architecture simple and efficient. Using Xnor gate, the proposed design achieves good results on same operating platform with frequency of 300MHz. Each field of a packet header generates a bit vector which will be ANDing with bit vector generated by others' field to get final result. In our proposed method, we performed checking of each bit of a field against each bit of a rule stored in a ruleset. Using behavioral modeling of VHDL, our design supports ternary bit format of '1', '0' and '*' (wildcard entry). Our proposed method illustrated in figure.2, same ruleset and field value=1101 is used as that of Field split bit vector (FSBV) and StrideBV. After XNORing operation, each bit of obtained output after XNORing is ANDing to get one bit which indicates the status of a rule for incoming packet field [5]. A 5-tuple standard packet header having five fields which are source Internet Protocol (IP) address, destination Internet Protocol (IP) address, source port number, destination port number and protocol layer. We have performed the classification of IP address fields and protocol field using Xnor gate i.e. using XnorBV method. We can use XnorBV module for source Internet Protocol (IP) address (32 bits), destination Internet Protocol (IP) address (32 bits) and protocol field (8 bits). Proposed XnorBV module supports prefix and exact match for Internet Protocol (IP) addresses and protocol layer respectively.

A field of 5-tuple incoming packet is checked against N rules of a ruleset. To understand the generation of bit vector using XnorBV method with the help of circuit diagram, let the length of rule and a field of an incoming packet is k bits. Let the first rule of a ruleset is given by $R_1 = W_{k-1}W_{k-2}\dots W_0$ and a field of an incoming packet is given by $F_1 = T_{k-1}T_{k-2}\dots T_0$. Each bit of a rule and a field is XNORing and after completion of XNORing operation, result of k-bits is ANDing to get single bit indicating the matching or mismatching of field with a rule. Same operation is performed for each and every rules of a ruleset of size N to get N-bit vector for the particular field of a packet.

To support range match for port numbers, we compared the field value against lower bound and upper bound value. Figure.3 shows the range module to perform range match for port numbers. For range match we have to define two values i.e. lower bound and upper bound as shown in figure.3. We defined ruleset set containing lower and upper bound and assume field value = 1000. In this work, field value is to compare against lower bound, if field value is greater or equal to lower bound then it gives '1' otherwise '0' similarly if a field value is lower than or equal to upper bound then it gives '1' otherwise '0'. Bit values obtained after comparing field value against lower bound and upper bound are ANDing to get one bit which indicates that field value is lying in the range of lower bound and upper bound. Range search module can support source port number and destination port number each of 16 bits. Our method supports prefix match for IP addresses, range match for port numbers and exact match for protocol field. Our architecture is independent of ruleset feature and supports multiple dimension classification.

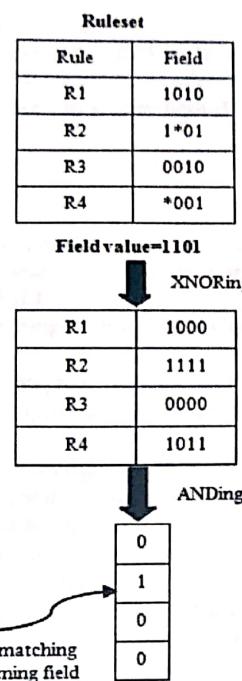


Figure2: Proposed XnorBV Algorithm

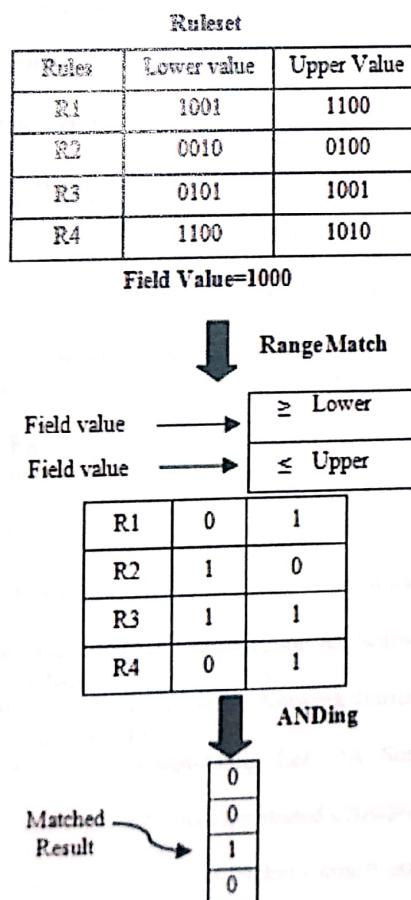


Figure3. Range Search Module for Range Match

IV. CONCLUSION

Proposed method XnorBV architecture using Xilinx ISE 13.1 suite selecting Virtex 6 XC6VLX760 as target device is memory efficient requires 15 byte/rule less than any other existing technique of packet classification. Architecture supports prefix, exact and range match without use of range to prefix conversion and is independent of ruleset feature. Power efficiency is also improved with power increment in addition of one rule. Proposed architecture can sustain high throughput of +100 Gbps at low latency which is desirable for low latency applications.

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List of Publication

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| Journal Name | Paper Title | Date | ISSN | Status |
|---|--|----------------|-------------|---------------|
| International Journal of Innovative Research Technology | A Review on High Performance Architecture For Packet Classification For Secure Communication Network | 8 January 2019 | 2369-6002 | Published |
| International Journal of Novel Research And Development | Design of high performance Architecture For Packet Classification For Secure Communication Network | 3 March 2019 | 2456-4184 | Published |