UNIVERSIDADE TECNOLÓGICA FEDERAL DO PARANÁ

ENGENHARIA ELÉTRICA/CONTROLE E

AUTOMAÇÃO/MESTRADO EM SISTEMAS DE ENERGIA

JOSÉ MÁRIO NISHIHARA DE ALBUQUERQUE

RELATÓRIO 1

INTRODUÇÃO AO SOFTWARE QUARTUS

CURITIBA

2025

Sumário

1 PROJETO 1

Código 1: VHDL do projeto 1.

```
-------------------------------------------------+
-- Aula 1                                        |
-- Projeto Digital com logica programavel em VHDL  |
-- Jose Mario Nishihara                          |
-- CPGEI/UTFPR                                   |
-------------------------------------------------+

LIBRARY ieee;
USE ieee.std_logic_1164.all;

----------------------------------------

ENTITY aula1 IS

  PORT(
      a, b   : IN STD_LOGIC ;
      s      : OUT STD_LOGIC
      );

END aula1;

----------------------------------------

ARCHITECTURE behavior OF aula1 IS
BEGIN

  s <= (a AND NOT b) OR (NOT a AND b);

END behavior;
```

Figura 1: Sumário de compilação do projeto 1.

Flow Status	Successful - Mon Jun 09 15:02:22 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	aula1
Top-level Entity Name	aula1
Family	Cyclone IV E
Device	EP4CE22F17C8
Timing Models	Final
Total logic elements	1 / 22,320 (< 1 %)
Total registers	0
Total pins	3 / 154 (2 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)

Figura 2: Simulação funcional do projeto 1.

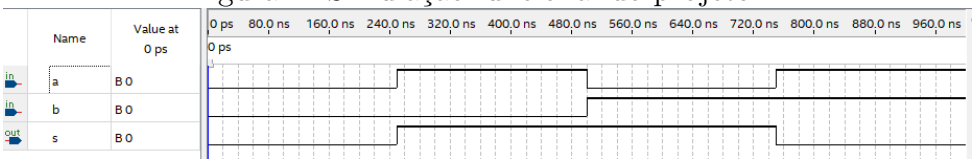
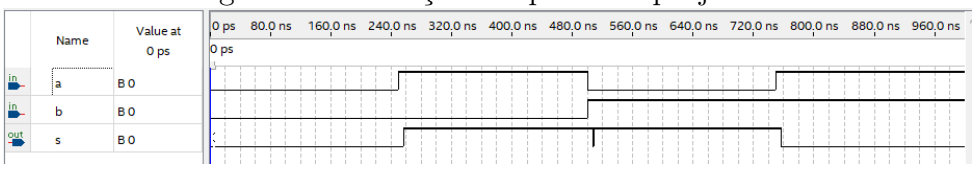


Figura 3: Simulação temporal do projeto 1.



2 PROJETO 2

Figura 4: Diagrama de blocos do projeto 2.

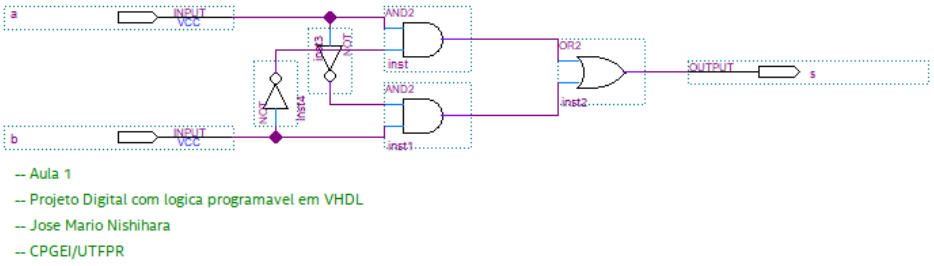


Figura 5: Sumário de compilação do projeto 2.

Flow Status	Successful - Mon Jun 09 15:25:14 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	aula1_2
Top-level Entity Name	aula1_2
Family	Cyclone IV E
Device	EP4CE22F17C6
Timing Models	Final
Total logic elements	1 / 22,320 (< 1 %)
Total registers	0
Total pins	3 / 154 (2 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)

Figura 6: Simulação funcional do projeto 2.

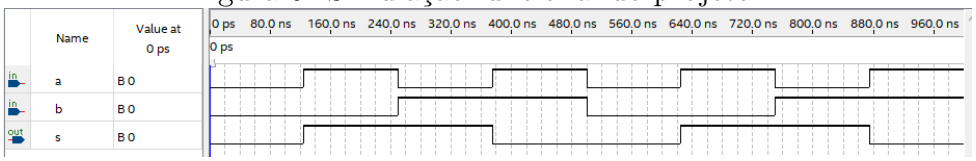
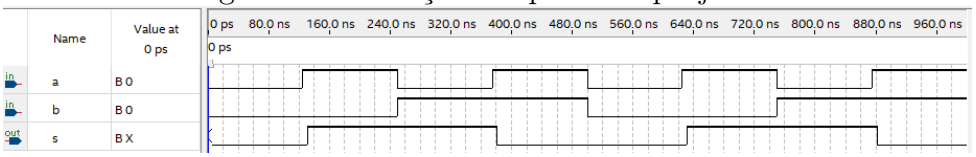


Figura 7: Simulação temporal do projeto 2.



3 PROJETO 3

Código 2: VHDL do projeto 3.

```
1  ----------------------------------------------------+
2  -- Aula 1                                           |
3  -- Projeto Digital com logica programavel em VHDL   |
4  -- Jose Mario Nishihara                             |
5  -- CPGEI/UTFPR                                      |
6  ----------------------------------------------------+
7
8  library ieee;
9  use ieee.std_logic_1164.all;
10
11 ---------------------------------------
12
13 entity aula1_3 is
14   port(
15       d,rst,clk : in std_logic;
16       q         : out std_logic
17       );
18 end aula1_3;
19
20 ---------------------------------------
21
22 architecture behavior of aula1_3 is
23 begin
24   process (clk,rst)
25   begin
26     if (rst = '1') then
27       q <= '0';
28     elsif (rising_edge(clk)) then
29       q <= d;
30     end if;
31   end process;
32 end behavior;
```

Figura 8: Sumário de compilação do projeto 3.

Flow Status	Successful - Mon Jun 09 15:21:03 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	aula1_3
Top-level Entity Name	aula1_3
Family	Cyclone IV E
Device	EP4CE22F17C6
Timing Models	Final
Total logic elements	1 / 22,320 (< 1 %)
Total registers	1
Total pins	4 / 154 (3 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)

Figura 9: RTL viewer do projeto 3.

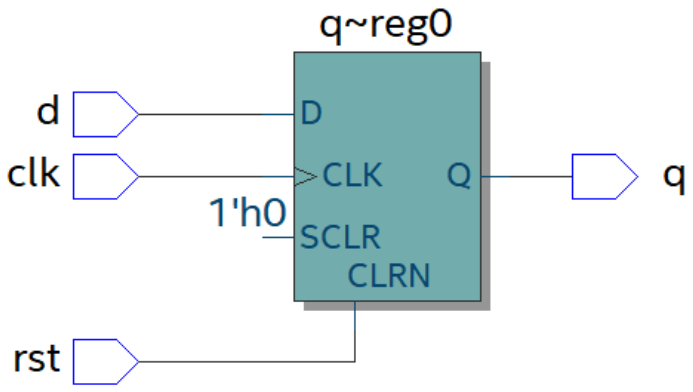


Figura 10: Simulação funcional do projeto 3.

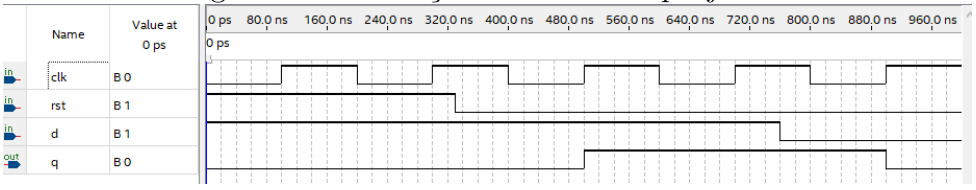


Figura 11: Simulação temporal do projeto 3.