RAK310 802.11b/g/n Wi-Fi® Module Data Sheet

Content

Revision History

Date Modified	Revision	Summary of Changes
2012.09.12	V1.0.1	1. PCB mechanical size, added size labels to module. 2. Added power management content.
2013.03.21	V1.0.2	1. Update 22th pin definition and schematic symbol pin definition 2. Update SDIO interface reference design 3. Modify PCB footprint dimension

Devices Overview

RAK310is an ultra-low-power, low-cost module that fully supports of major encryption modes as well as WAPI encryption mode, a Wi-Fi ® module with SDIO interface that supports 802.11b/g/n protocol. The module internally integrates RF station, balun, RF switch, crystal oscillator and power switch circuit, enabling fast hardware design. Plus, maturely powered by Linux and Android environmentsimplifies customer software design.

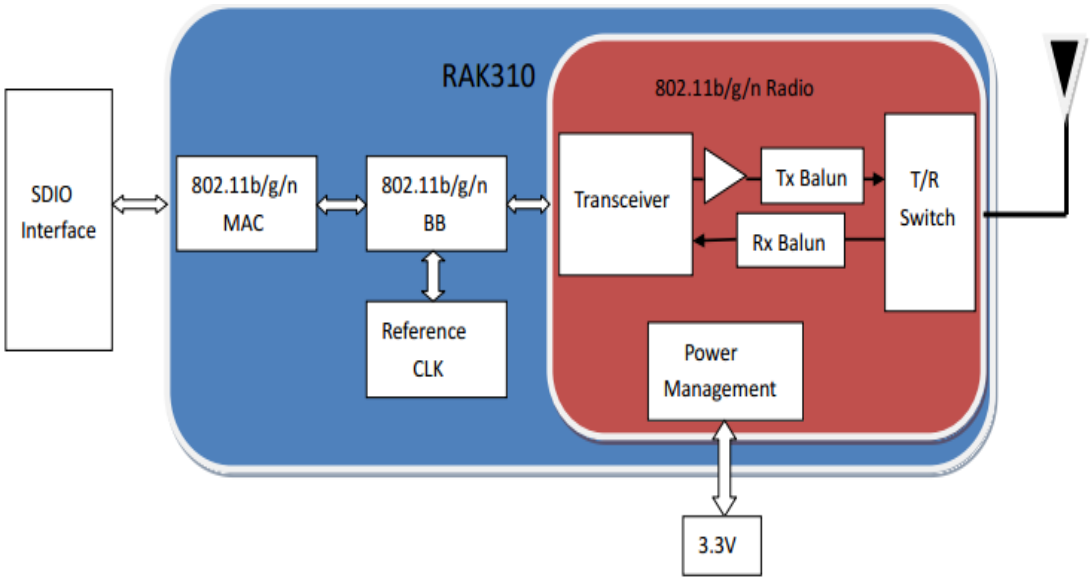
Devices Features

- Support IEEE 802.11b/g/n wireless standards, IEEE 802.11n uniflow, enabling high throughput rate
- Support SDIO 1.0 & 2.0 interfaces
- Reservation for Bluetooth coexist
- Support WEP, WPA/WPA2-PSK,TKIP encryptions
- Infrastructure mode, Ad-Hoc mode
- Support WIFI Direct
- Support WAPI
- Completely WLAN drive under different OS, such as Linux and Android
- Power supply: 3.14~3.46V
- Working temperature: -40~+85℃
- Moisture sensitive level (MSL) Level 3
- Package size: 21.34mmx19.05mmx2.5mm

Key Applications

- Tablet PC
- Medical Device
- Industrial Handset
- Industrial automation and measurement
- WIFI Camera
- Internet-based Consumer electronics, like playing station

RAK 310 System Diagram



1. Functional Description

1.1 Host Interface

- SDIO Interface
  - SDIO 1.0 & 2.0 compatible
  - Support SDIO 1bit, 4bit mode
  - Maximum clock frequency: 50MHz

1.2 WLAN

1.2.1 MAC

- Comply with IEEE802.11b/g/n standards
- Support WEP, WPA/WPA2-PSK, TKIP, AES encryptions
- Support WPS-PBC

1.2.2 Baseband Processor

- Support DSSS (1, 2Mbps), CCK(1, 2, 5.5, 11Mbps), OFDM (6, 9, 12, 18, 24, 36, 48, 54Mbps), HT20 (MCS0 - MCS7)
- Adopt Orthogonal Frequency Division Multiplexing (OFDM) technology, combining with BPSK, QPSK, 16-QAM and 64-QAM; 820.11b with CCK and DSSSmodulation technology

1.2.3 Internal Frequency

- Internally integrate26MHzhigh-accuracy reference clock, simplifying clock circuit design

1.2.4 Power Management

- Internally integrate power management module, supporting 5 power working states: OFF state, HOST-OFF state, SLEEP state, WAKE-UP state, ON state
- Internally power supply switch: with external 3.3V main power supply only, switching to internal power management module to supply, and performing management

1.2.5 RF Circuit

- Internally integrate power amplifier, transceiver, transceivingbalun and RF switch
- Externally connect RF part to antenna through u.FL interface
- Highly integrated RF circuit greatly simplifies RF design, without need to concern the RF circuit of Wi-Fi part

2. Electrical Characteristics

2.1 Absolute Maximum

The Table 2-1 shows the absolute maximum, the Table 2-2 shows the working conditions that RAK310 recommends. The absolute maximum is a value, exceeding which any operation would cause damage to the devices, thus it is not recommended to perform any operation above this maximum value or other values indicated in this document.

Table 2-1 absolute maximum

Symbols	Parameters	Max Value	Unit
VDD3V3	External 3.3V supply voltage	-0.3 ~ 4.0	V
3.3V IO VIH Max	When IO voltage is 3.3V, IO Max voltage	VDD+0.3	V
VIH Min	When IO voltage is 3.3V, IO Min voltage	-0.3	V
RFin	Max RF input (based on 50Ω input)	+10	dBm
Tstore	Storage ambient temperature	-45~+135	℃
ESD	ESD resistance	2000	V

2.2 Recommended Operating Parameters

Table 2-2 Recommended Operating Parameters

Symbols	Parameters	Min Value	Typical Value	Max Value	Unit
VDD3V3	External 3.3v voltage	3.14	3.3	3.46	V
$T_{ambient}$	Ambient temperature	-40		85	℃

2.3 DC Electrical Characteristics

Table 2-3 and Table 2-4 illustrate the general DC electrical characteristics under the recommended operating conditions (except special statement)

Table 2-3 general DC electrical characteristics (3.3V I/O Operating)

Symbols	Parameters		Conditions	Min Value	Typical Value	Max Value	Unit
V_{IH}	High level input			0.7xVDD			V
V_{IL}	Low level input					0.3xVDD	V
I_{IL}	Input leakage current	No pull-up, pull-down resistance	0<VIN<VDD 0<VOUT<VDD	0		-3	nA
		Pull-up	0<VIN<VDD 0<VOUT<VDD	16		48	μA
		Pull-down	0<VIN<VDD 0<VOUT<VDD	-14		-47	μA
V_{OH}	High level output		IOH=-4mA	0.9xVDD			V
			IOH=-12mA	0.9xVDD			V
V_{OL}	Low level output		IOH=4mA			0.1xVDD	V
			IOH=12mA			0.1xVDD	V

2.4 RF Electrical Characteristics

Table 2-4 illustrates RF electrical characteristics of receiverspecifications, and Table 2-5 illustrates RFtransmit specifications.

Table 2-4 RF Receiver Specifications

Parameters		Test Conditions	Typical Value	Unit
Receiver sensitivity	11b, 1Mbps		-97	dBm
	11b, 2 Mbps		-92	dBm
	11b, 5.5 Mbps		-90	dBm
	11b, 11 Mbps		-88	dBm
	11g, 9Mbps		-91	dBm
	11g, 18Mbps		-87	dBm
	11g, 36Mbps		-81	dBm
	11g, 54Mbps		-75	dBm
	11n, MCS1, 13Mbps		-89	dBm

	11n, MCS3, 26Mbps		-82	dBm
	11n, MCS5, 52Mbps		-75	dBm
	11n, MCS7, 65Mbps		-72	dBm
Maximum input signal	CH7	11g, 54Mbps	10	dBm
Adjacent channel suppression	6Mbps		37	dBc
	54Mbps		21	dBc
	MCS0		38	dBc
	MCS7		20	dBc

Table 2-5 Transmit Specifications

Symbols	Parameters	Requirements	Typical Value	Unit
$\mathbf{F}_{tx}$	Frequency range		2.4	GHz
$\mathbf{P}_{out}$	Output power			
	802.11b	1Mbps	17	dBm
	802.11g	6Mbps	17	
	802.11n,HT20	MCS0	17	
	802.11g EVM	54Mbps	14	
	802.11n,HT20 EVM	MCS7	10	
$\mathbf{A}_{pl}$	Power balance loop accuracy		±1.5	dB

3. AC Specification

3.1 SDIO Interface Timing Diagram

Figure 3-1 shows the SDIO interface time sequence.

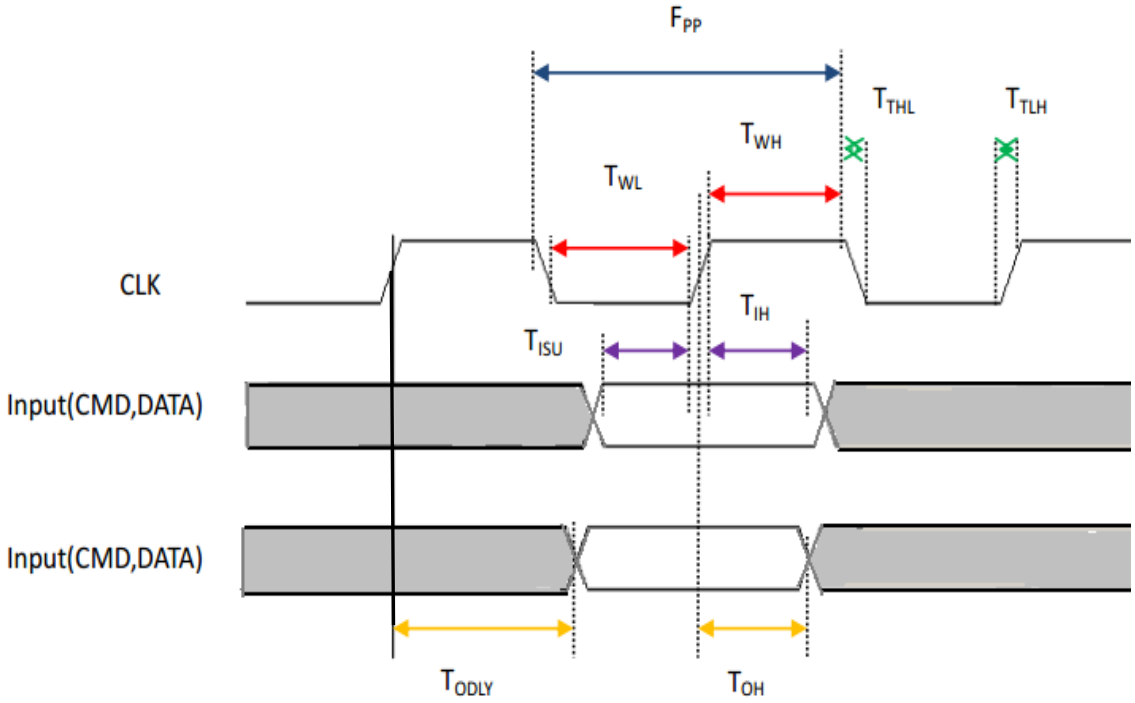


Figure 3-1 SDIOInterface Time Sequence Diagram

3.2 SDIO Interface Timing Requirement

Table 3-2 illustrates the parameter requirement under SDIO interface time sequence.

Table 3-2 SDIO Interface Timing Parameter Requirement

Symbols	Parameters	Min Value	Max Value	Unit	Note
F_{PP}	Clock frequency of data transfer	0	50	MHz	40pF≥CL
T_{WL}	Clock time in low level	7		ns	40pF≥CL
T_{WH}	Clock time in high level	7		ns	40pF≥CL
T_{TLH}	Clock time of rising edge		10	ns	40pF≥CL
T_{THL}	Clock time of falling edge		10	ns	40pF≥CL
T_{ISU}	Time of input set up	6		ns	40pF≥CL
T_{IH}	Time of input hold	2		ns	40pF≥CL
T_{OH}	Time of output maintained	2.5		ns	40pF≥CL
T_{ODLY}	Output delay in data transmission mode	0	14	ns	40pF≥CL

3.3 Reset Timing

Figure 3-2 shows the module timing when power on and power off, and Figure 3-3 shows the reset time sequence， Table 3-3 shows the reset timing requirement range.

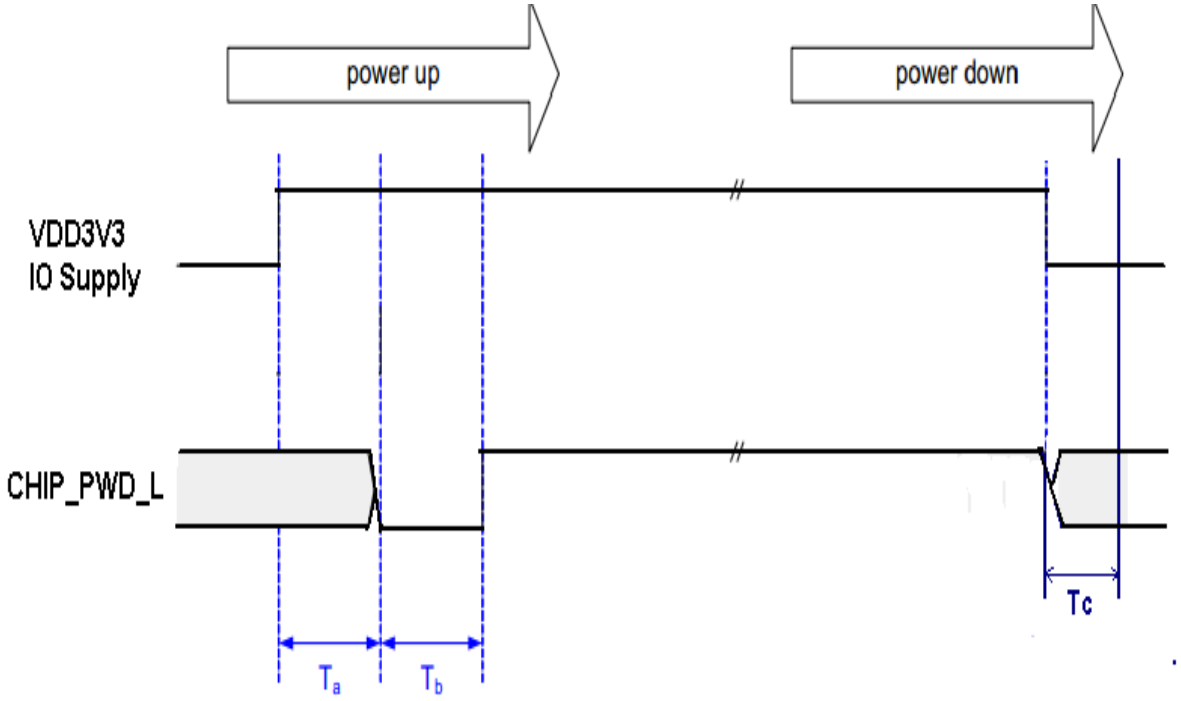


Figure 3-2Power on/Power off Time Sequence Diagram

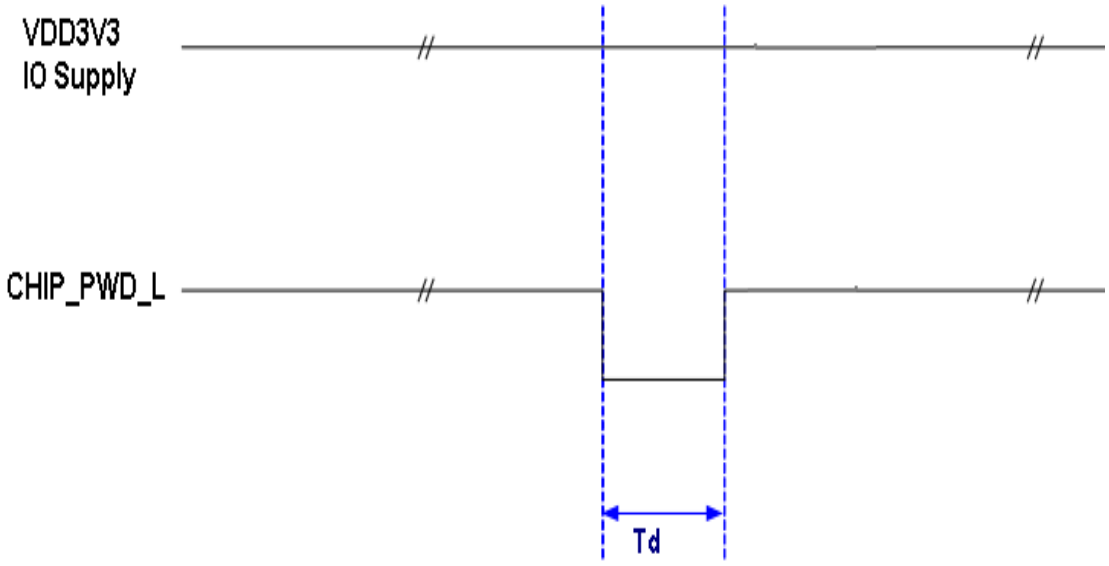


Figure 3-3Reset Time Sequence Diagram

Table 3-3Reset Timing Parameter Requirement

Symbols	Descriptions	Min Value（μS）
Ta	Time period from VDD3V3 power on to IO power effective	0
Tb	Time period from VDD3V3 effective to reset completed	5
Tc	Time period from VDD3V3 power off to reset effective	NA
Td	Reset pulse length	5

4. Pin Definition

4.1 Module Pin Assignment

Figure 4-1 shows module RAK310 pin assignment diagram.

4.2 Module Pin Description

Table 4-1 shows a detailed pin functional description of module RAK310.

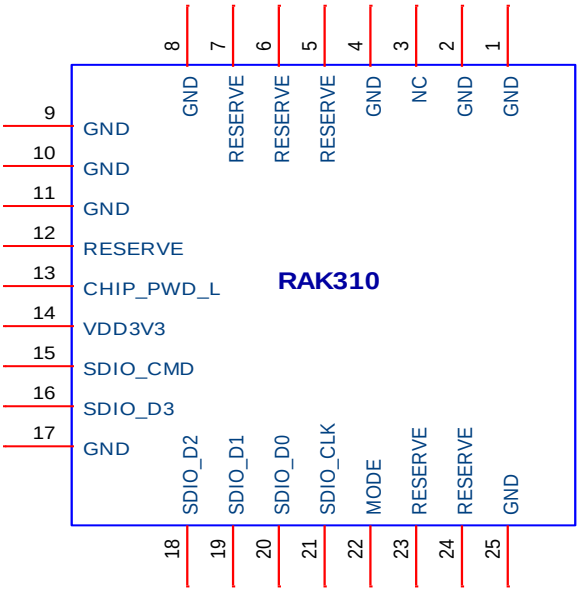


Figure 4-1 RAK310 Pin Assignment Diagram

Table 4-1 RAK310 Pin Description

Pin No.	Name	Description	Type	Pin No.	Name	Description	Type
1	GND	Ground	P	14	VDD3V3	3.3V power	P
2	GND	Ground	P	15	SDIO_CMD	SDIO command	IO
3	NC	No connect	P	16	SDIO_D3	SDIO data position 3	IO
4	GND	Ground	P	17	GND	Ground	P
5	RESERVE	RESERVE	P	18	SDIO_D2	SDIO data position 2	IO
6	RESERVE	RESERVE	O	19	SDIO_D1	SDIO data position 1	IO
7	RESERVE	RESERVE	I	20	SDIO_D0	SDIO data position 0	IO
8	GND	Ground	P	21	SDIO_CLK	SDIO clock line	I
9	GND	Ground	P	22	MODE	Setting chip operation mode , pull-up resistor is needed	I
10	GND	Ground	P	23	RESERVE	RESERVE	P
11	GND	Ground	P	24	RESERVE	RESERVE	P
12	RESERVE	RESERVE	I	25	GND	Ground	P
13	CHIP_PWD_L	Used to reset module	I	26	PAD	Ground	P

Note: Table 4-1 pin type letter explanation，P: Power I: Input O: Output IO: Bidirectional input/output; the 26th pin is the center exposed pad

5. Hardware Introduction

5.1 Top View

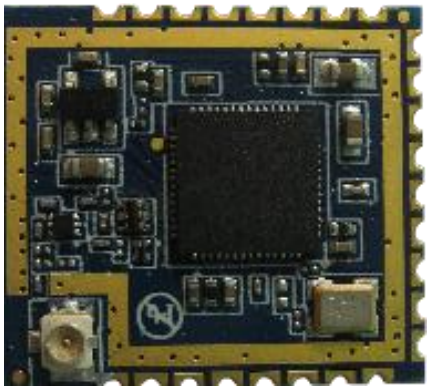


Figure 5-1 RAK310 Top View

5.2 Bottom View

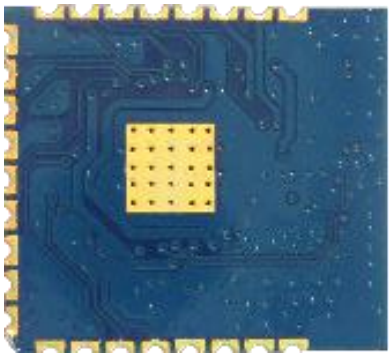


Figure 5-2 RAK310 Bottom View

5.3 RAK310 Recommended PCB Mechanical Size

Figure 5-3 shows the recommended PCB mechanical size (mm).

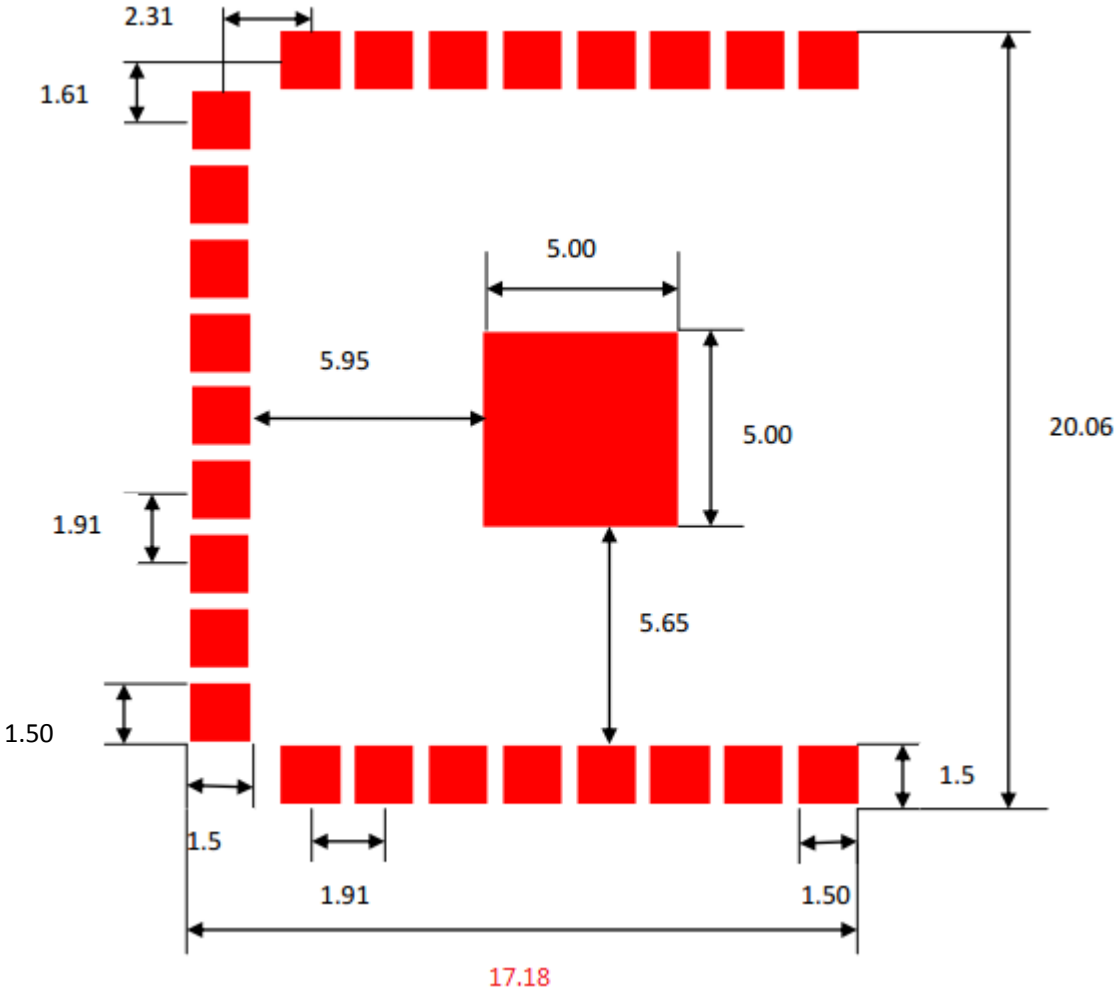


Figure 5-3 PCB Mechanical Size

6. Design Reference

6.1 Design Reference in SDIO Interface Mode

Figure 6-1 illustrates the module RAK310 design reference diagram in SDIO interface working mode.

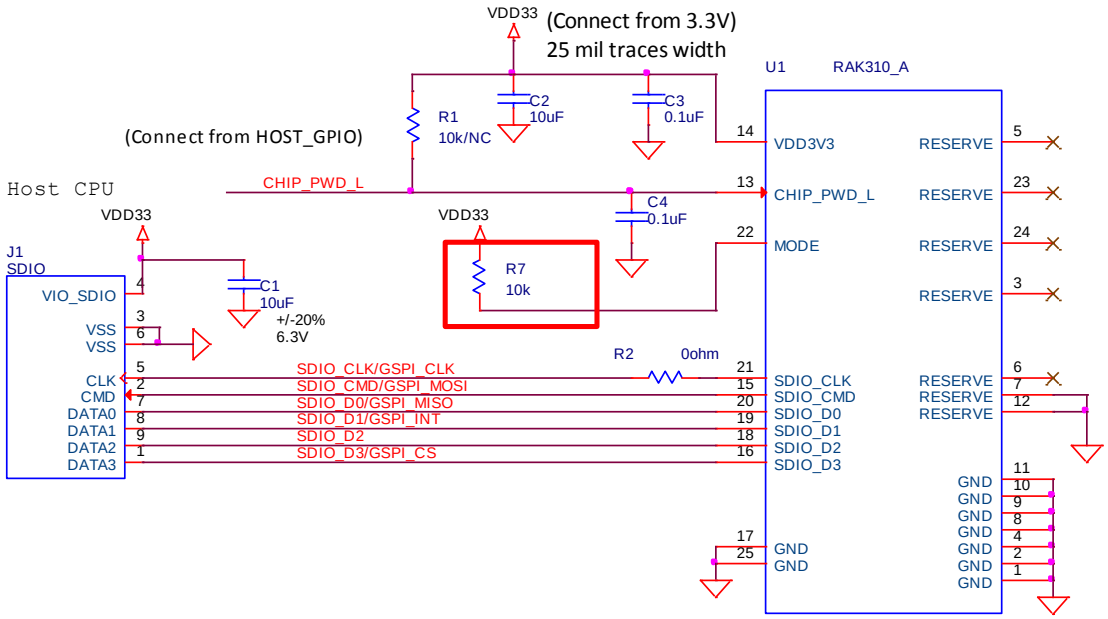


Figure 6-1 SDIO Interface Mode Diagram

7. Power Management

Table 7-1 Power Saving Mode

Working Mode	Working State	Power Consumption
Power saving	OFF	0.004mA
	HOST_OFF	0.048mA
	SLEEP	0.215mA
Continue receive (max)	54Mbps(OFDM)	86mA
Continue transmit (max)	54Mbps(OFDM)	210mA

OFF State: enter this state by directly pulling down CHIP_PWD_L pin;sleep clock is disabled in this state, no state is enabled.
HOST_OFF State: WLAN is disabled，only host interface is live, all the other parts of chip are disabled；Wake up by sending commands to host register.
SLEEP State: Only sleep clock works, Oscillator and crystal are disabled, any waking event will compulsively make a transfer from this state to WAKE-UP state.

8. Manufacturing Guidance

Figure 7-1 shows the temperature graph when manufacture by reflow soldering method.

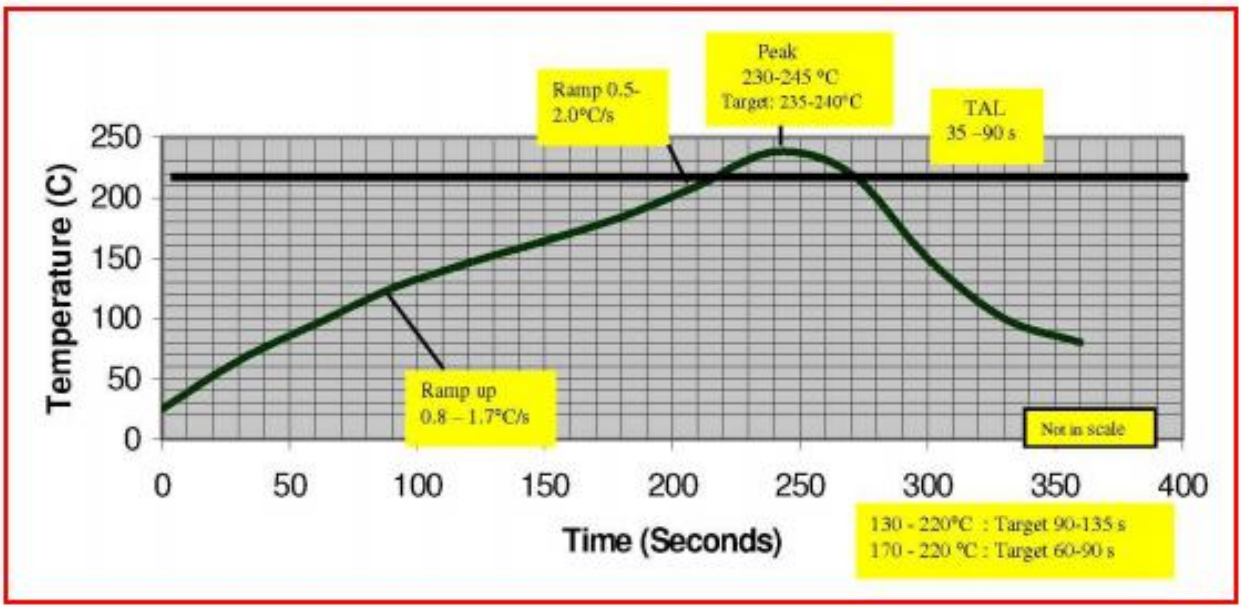


Figure 7-1 Recommended Reflow Soldering Temperature Graph

Note: as shown in the above figure, it is based on the SAC305 lead-free tin paste (3% silver, 0.5% copper). Alpha OM-338 lead-free cleaning-free flux is recommended. This figure is mainly used for guidance. The entire process time is subject to thermal pad number of assembly board and device Intensity.

9. Order Information

9.1 Contact and Address

For more information, please contact the sales of Shenzhen Incel Electronics Co., Ltd.
Add: Room 813, Middle 8F, Building 4, Saige Science and Technology Park
Tel: 0755-83762580
E-mail: szsjl_66q@hotmail.com
Website: www.incel.net.cn

9.2 Product Information

Product Models:
RAK310 (Pb Free)Tray
Weight Information:
RAK310 0.74g/pcs