Computer Architecture. The cache memory

Full name:	Guillermo Facundo Colunga	Spanish ID:	45170929X

A program with a given pattern of memory accesses is executed in a computer. The configuration of the memory system and the sequence of memory accesses are generated by the following command:

```
gencache id
```

where `id` is the 8-digit number of your Spanish ID (DNI without letter). For instance, if your ID is 12345678-Z the command will be

```
gencache 12345678
```

After executing `gencache` program, two text files are generated: `config-id.txt` and `trace-id.prg`. The former describes the memory system and the latter contains the sequence of memory accesses.

Taking into account the content of the above files, you must use the cache simulator to configure the memory system. Save this configuration in a file called `cache-id.memx`. Once saved, you must load the trace file in the cache simulator.

Simulate step-by-step the memory accesses both in the simulator and in paper and write down the necessary information to answer the following questions. Remember that the trace file is a text file that can be edited with a text editor. The first column of this file shows the access type

(0: instruction fetch, 2: data item read, 3: data item write).

1. What memory addresses cause a cache miss? Answer in hexadecimal.

//With the default configuration, those given by the config-45170929, I had no enough memory space to load the trace. To fix that, I'd decided to duplicate the main memory space. That it up to 4Kbytes

6E3 - 0, 0E7 - 2, 6E9 - 0, 0E9 - 3, 36E - 0, 0F0 - 2, 34B - 0, 34C - 0, 111 - 2, 112 - 3, 6EA - 0, 6EC - 0, 114 - 2, 116 - 3, 6EE - 3, 118 -2.

2. What is the cache hit rate? Answer in percentage.

60% - Aciertos | 40% - Fallos

3. What main memory blocks are replaced? Write the **block numbers** in hexadecimal.

74h, 73h, 89h, 89h, 8Ah, 8Ah, 8Bh, 8Ch.

4. What main memory blocks are updated? Write the **block numbers** in hexadecimal.

89h, 8Ah, 8Ch

5. If the memory access pattern were fully random, what would the cache hit rate be? Answer in percentage.

(16 [cache blocks] / 1024 [main memory blocks])*100 = 1’5625%

6. Let’s assume that two cache configurations for the same cache memory, with the same cache size in each configuration, achieve the same hit rate in a simulation process:
    - Configuration A: 2-way set associative placement strategy.
    - Configuration B: fully associative placement strategy.

   Which configuration would you choose for your cache memory and why?

Configuration A. As both configurations achieve the same hit rate then we just have to care about the cost of implementation which actually is the 2-way associative.

Once you have answered the above questions, create a file called

’`Last name, First name.zip`’ with the files `config-id.txt`, `trace-id.txt`, `cache-id.memx` and `cache-id.doc`. The latter is this .doc file with the answers of your exercise. Finally, upload the `.zip` to the Campus Virtual in the appropriate deliverable task.