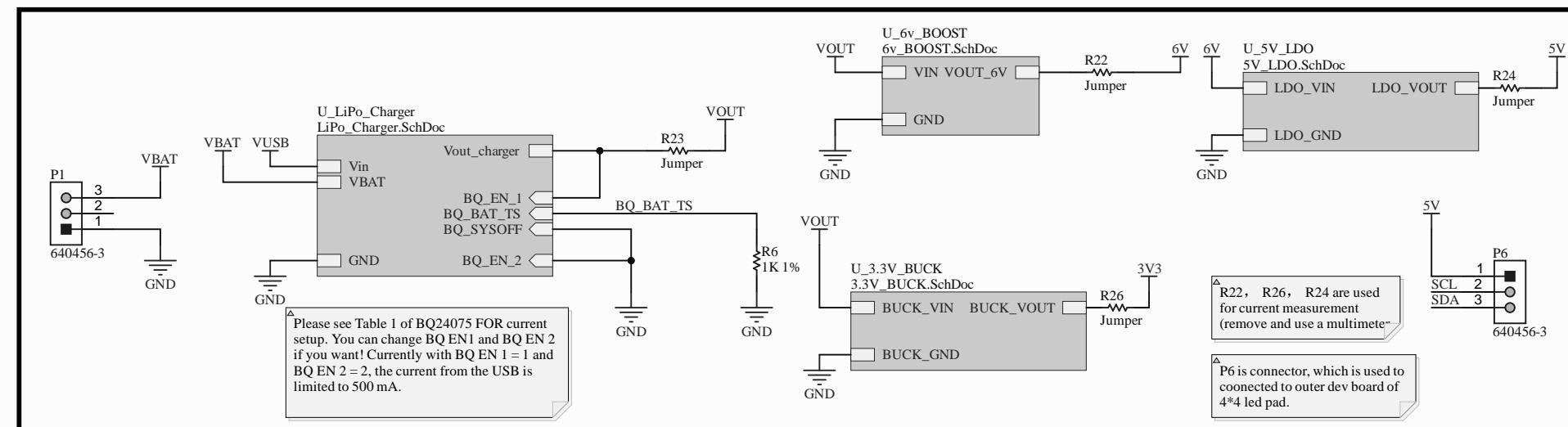


THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO.	REV.	1	2	3	4	5	6	7	8	9	10

POWER SUPPLY - CHANGE ME TO YOUR POWER ARCHITECTURE



NOTES

Section to add version notes or any other general information

NOTE:

This power architecture is just

the

architect

ure

to

match

the

power

arch

ect

you

des

igned

for

your

proj

ect

Note

that

6V

is

conne

cted

to

noth

ing!

▲

3V3 BUCK . If USING for SD CARD,

consid

er

con

nect

the

EN

to

the

MCU

so

you

can

turn

off

the

SD

Car

d

in

sl

eep

mod

us

on

the

SD

Ca

rd

in

the

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO.	REV.	2	1
---------	------	---	---

H

H

G

G

F

F

E

E

D

D

C

C

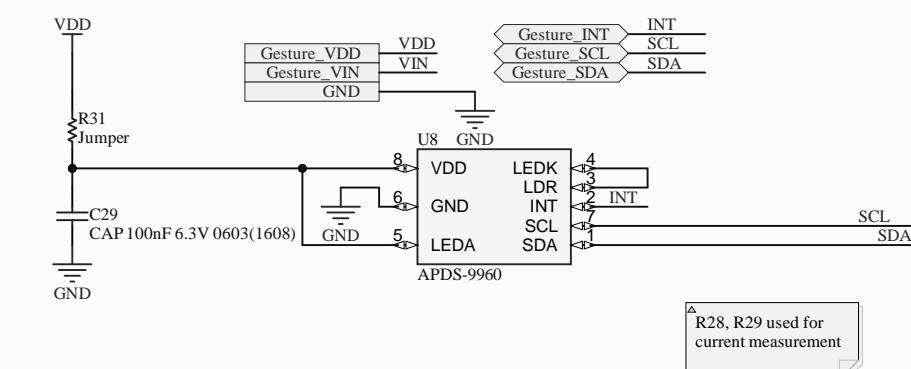
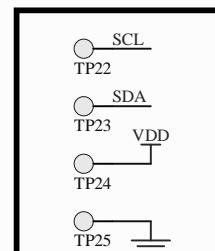
B

B

A

A

TESTPOINTS



APPROVALS		DATE	PROJECT	Penn Engineering
ENG:	.			
DSN:	.		PROJECT REVISION:	DOCUMENT REVISION: DESIGN ITEM:
CHK:	.			
REFERENCE DOCUMENTS				TITLE: APDS9960.SchDoc
BOM:				
ASSY DWG:		SIZE	CAGE CODE	DWG NO.
FAB DWG:		C		*
PCB DWG:		SCALE:	FILE NAME:	APDS9960.SchDoc SHEET 2 OF 10

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO.	REV.	3	2	1
---------	------	---	---	---

H

H

G

G

F

F

E

E

D

D

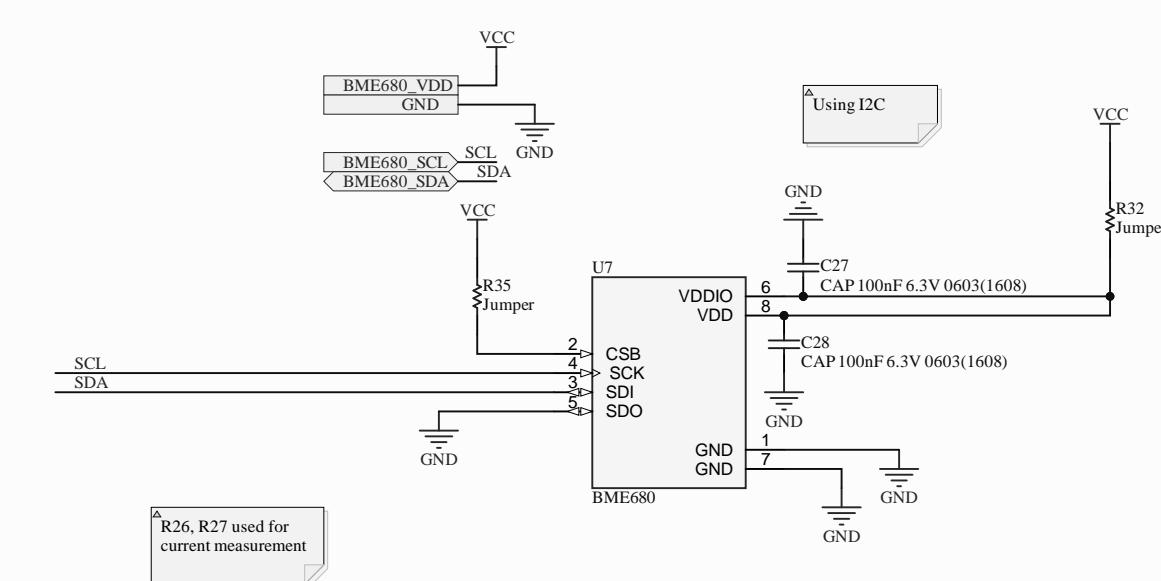
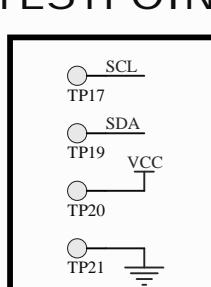
C

C

B

B

TESTPOINTS



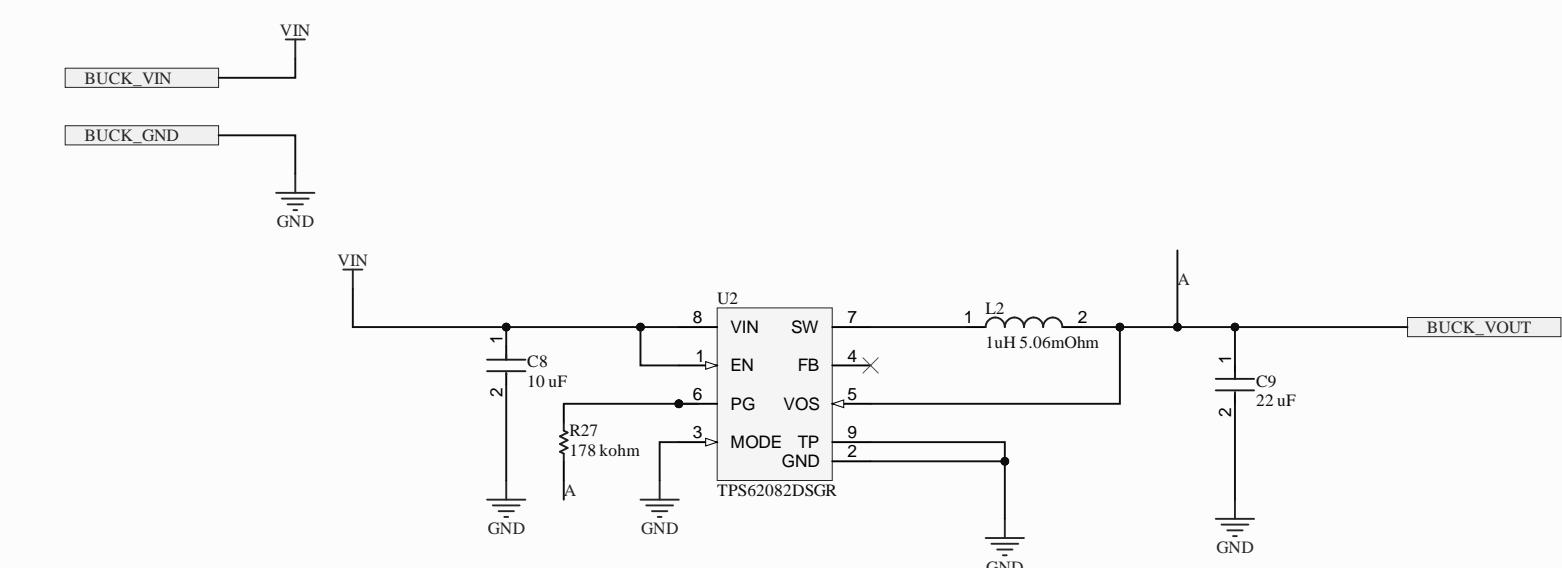
APPROVALS		DATE	PROJECT	Penn Engineering
ENG:	.			
DSN:	.		PROJECT REVISION:	DOCUMENT REVISION: DESIGN ITEM:
CHK:	.		TITLE	BME680.SchDoc
REFERENCE DOCUMENTS				
BOM:			ASSY DWG:	SIZE CAGE CODE DWG NO.
FAB DWG:			FAB DWG:	
PCB DWG:			PCB DWG:	SCALE: FILE NAME: BME680.SchDoc SHEET 3 OF 10

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO.	REV	4	1
REVISION	DESCRIPTION	DATE	APPROVED

H
G
F
E
D
C
B
A

H
G
F
E
D
C
B
A



APPROVALS		DATE	PROJECT	Penn Engineering
ENG:				
DSN:			PROJECT REVISION:	DOCUMENT REVISION: DESIGN ITEM:
CHK:			TITLE	
REFERENCE DOCUMENTS				3.3v_Buck.SchDoc
BOM:				
ASSY DWG:		SIZE	CAGE CODE	DWG NO.
FAB DWG:		C		*
PCB DWG:		SCALE:	FILE NAME:	3.3V_BUCK.SchDoc

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO.	REV	5	1
REVISION	DESCRIPTION	DATE	APPROVED

H

H

G

G

F

F

E

E

D

D

C

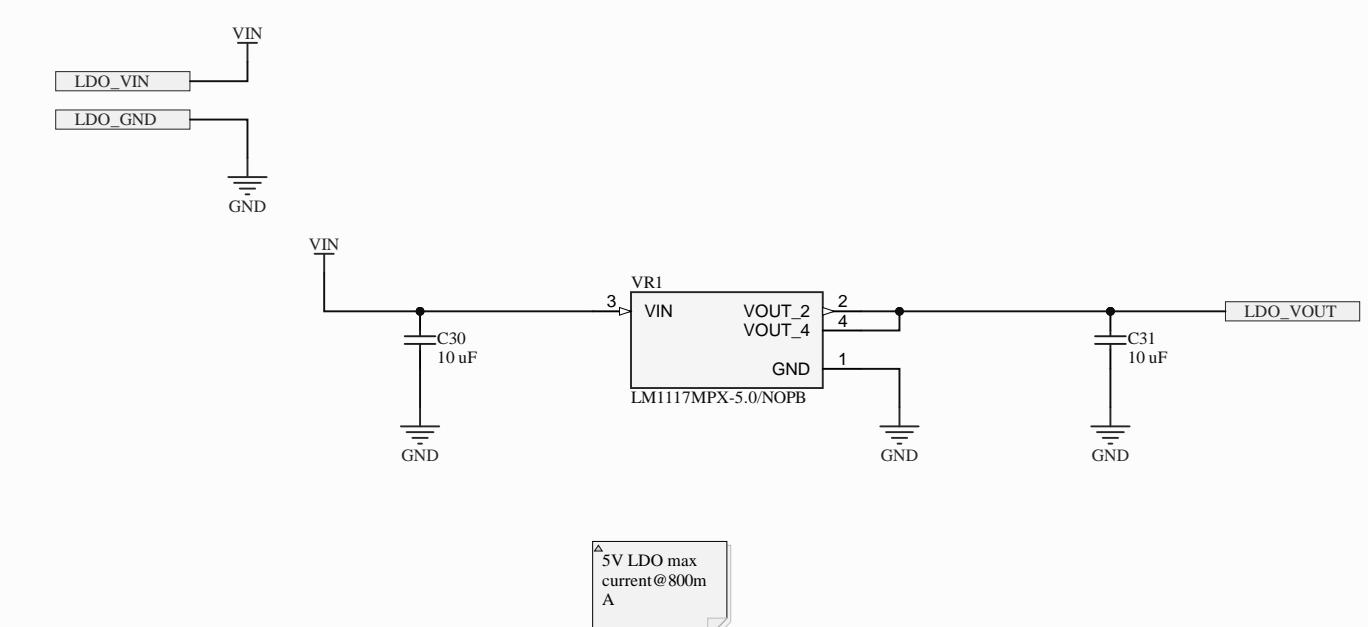
C

B

B

A

A



APPROVALS		DATE	PROJECT	Penn Engineering
ENG:	.			
DSN:	.		PROJECT REVISION:	DOCUMENT REVISION: DESIGN ITEM:
CHK:	.			
REFERENCE DOCUMENTS				TITLE: 5V_LDO.SchDoc
BOM:			ASSY DWG:	SIZE CAGE CODE DWG NO. REV *
FAB DWG:			FAB DWG:	
PCB DWG:			PCB DWG:	SCALE: FILE NAME: 5V_LDO.SchDoc SHEET 5 OF 10

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO.	REV	6	2	1
REVISION	DESCRIPTION	DATE	APPROVED	

H

H

G

G

F

F

E

E

D

D

C

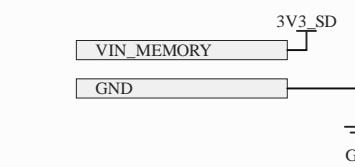
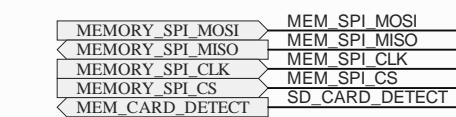
C

B

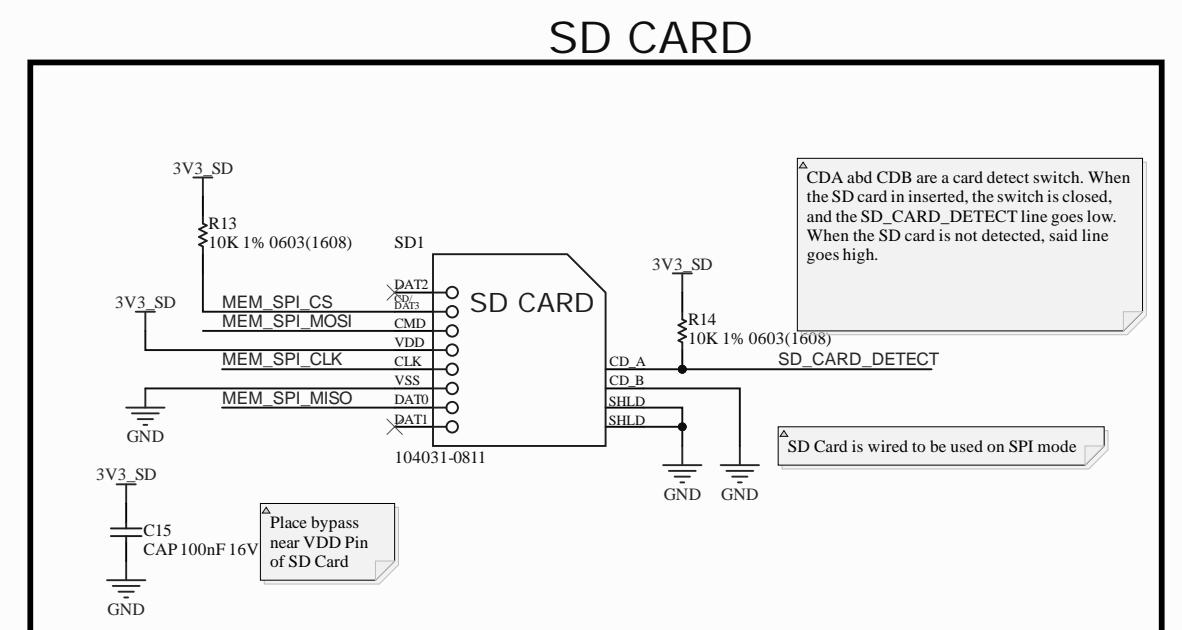
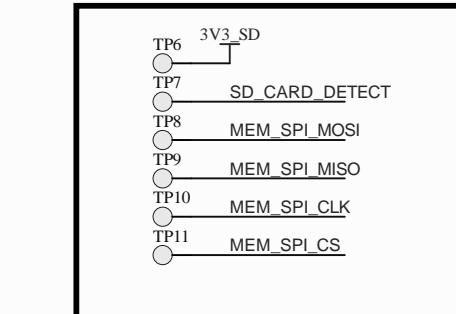
B

A

A



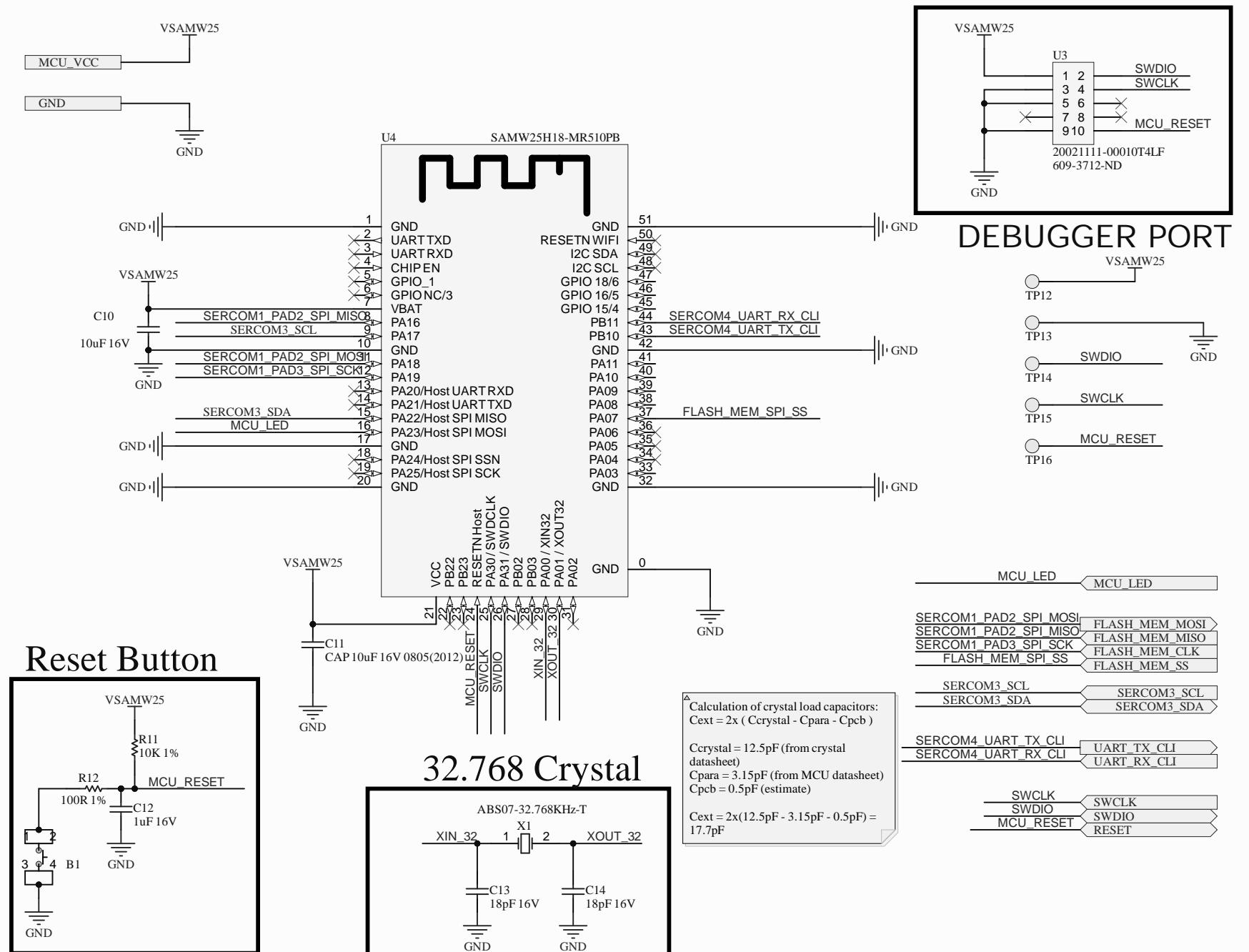
TESTPOINTS



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:		PROJECT REVISION:	DOCUMENT REVISION:
DSN:		DESIGN ITEM:	
CHK:		TITLE: Memory.SchDoc	
REFERENCE DOCUMENTS		ASSY DWG: SIZE CAGE CODE DWG NO. * FAB DWG: PCB DWG: SCALE: FILE NAME: Memory.SchDoc SHEET 6 OF 10	

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

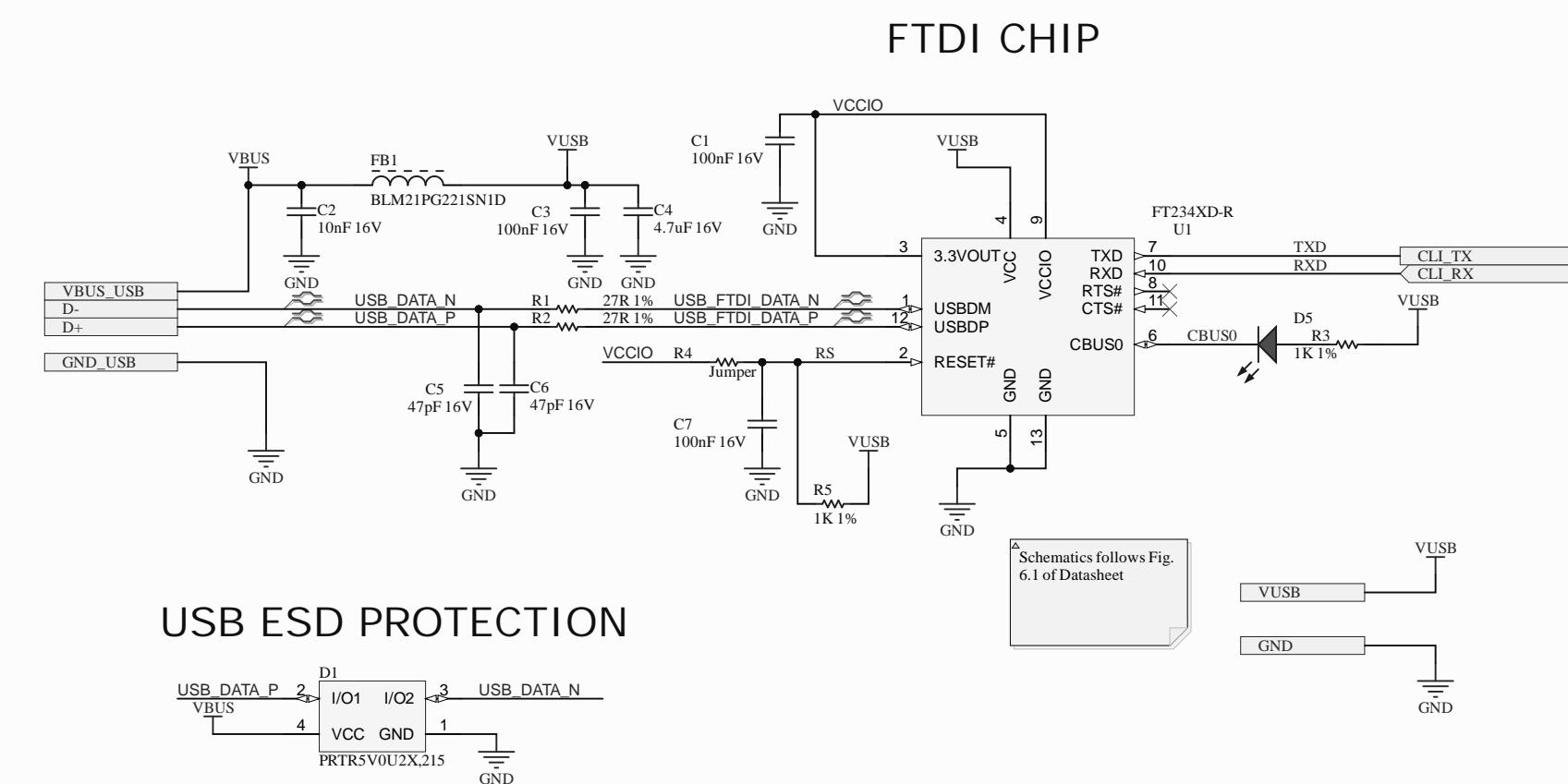
DWG NO.	REV.	7	2	1
---------	------	---	---	---



APPROVALS	DATE	PROJECT	Penn Engineering
ENG: .		DOCUMENT REVISION:	
DSN: .		DESIGN ITEM:	
CHK: .		TITLE	MCU.SchDoc
REFERENCE DOCUMENTS			
ASSY DWG:	SIZE	CAGE CODE	DWG NO.
FAB DWG:	C		*
PCB DWG:	SCALE:	FILE NAME	MCU.SchDoc
			SHEET 7 OF 10

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

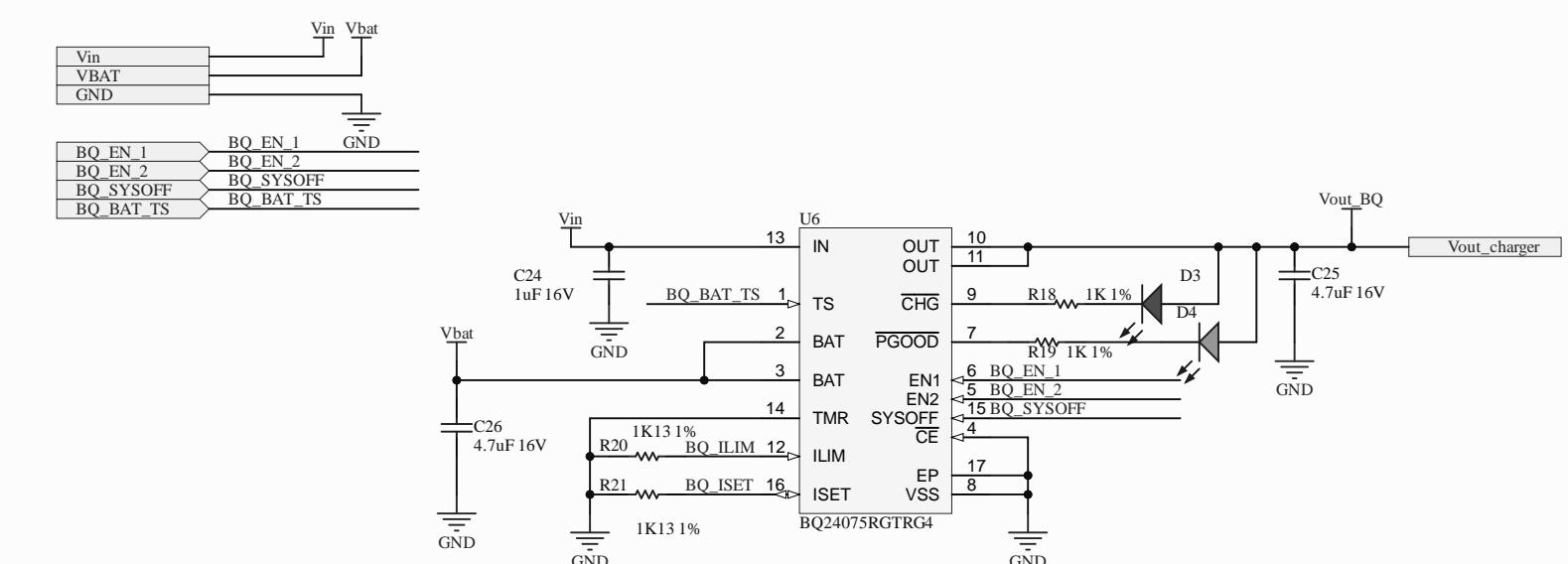
DWG NO.	REV	SHEET	REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:			
DSN:		PROJECT REVISION:	DOCUMENT REVISION:
CHK:		DESIGN ITEM:	
REFERENCE DOCUMENTS			
BOM:	TITLE: FTDI.SchDoc		
ASSY DWG:	SIZE	CAGE CODE	DWG NO.
FAB DWG:	C		
PCB DWG:	SCALE:	FILE NAME	FTDI.SchDoc
			Sheet 8 of 10

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

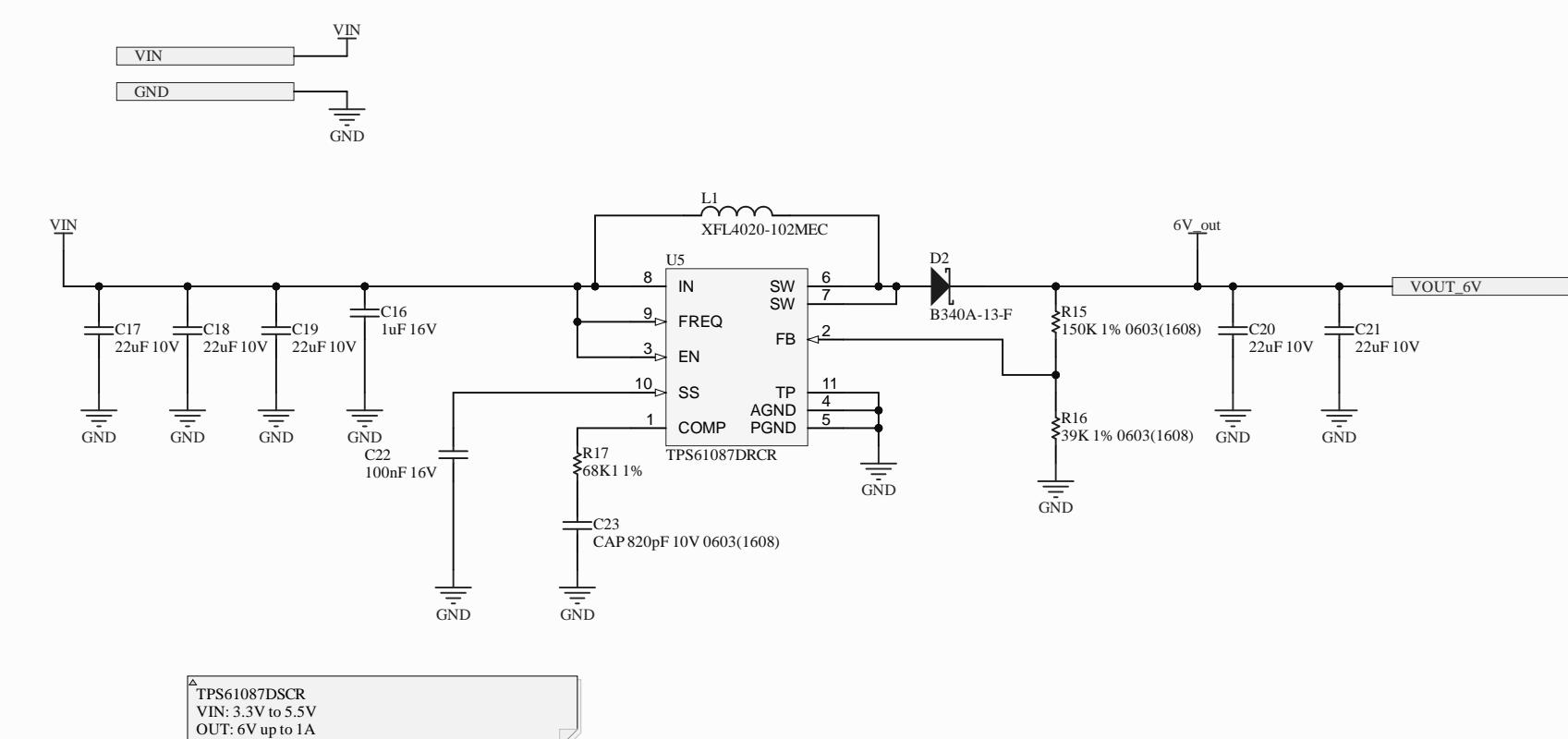
DWG NO.	REV	9	1
REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:			
DSN:		PROJECT REVISION:	DOCUMENT REVISION:
CHK:		TITLE	DESIGN ITEM:
REFERENCE DOCUMENTS			
BOM:		ASSY DWG:	SIZE
FAB DWG:		CAGE CODE	DWG NO.
PCB DWG:		REV	*
		SCALE:	FILE NAME LiPo_Charger.SchDoc
		SHEET	9 OF 10

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO.	REV	10	SHT	REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:			
DSN:		PROJECT REVISION:	DOCUMENT REVISION:
CHK:		DESIGN ITEM:	
REFERENCE DOCUMENTS		TITLE: 6v_BOOST.SchDoc	
BOM:		ASSY DWG:	SIZE
FAB DWG:		CAGE CODE	DWG NO.
PCB DWG:		REV	*
		SCALE:	FILE NAME: 6v_BOOST.SchDoc
			SHEET 10 OF 10

A

B

C

D

E

F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

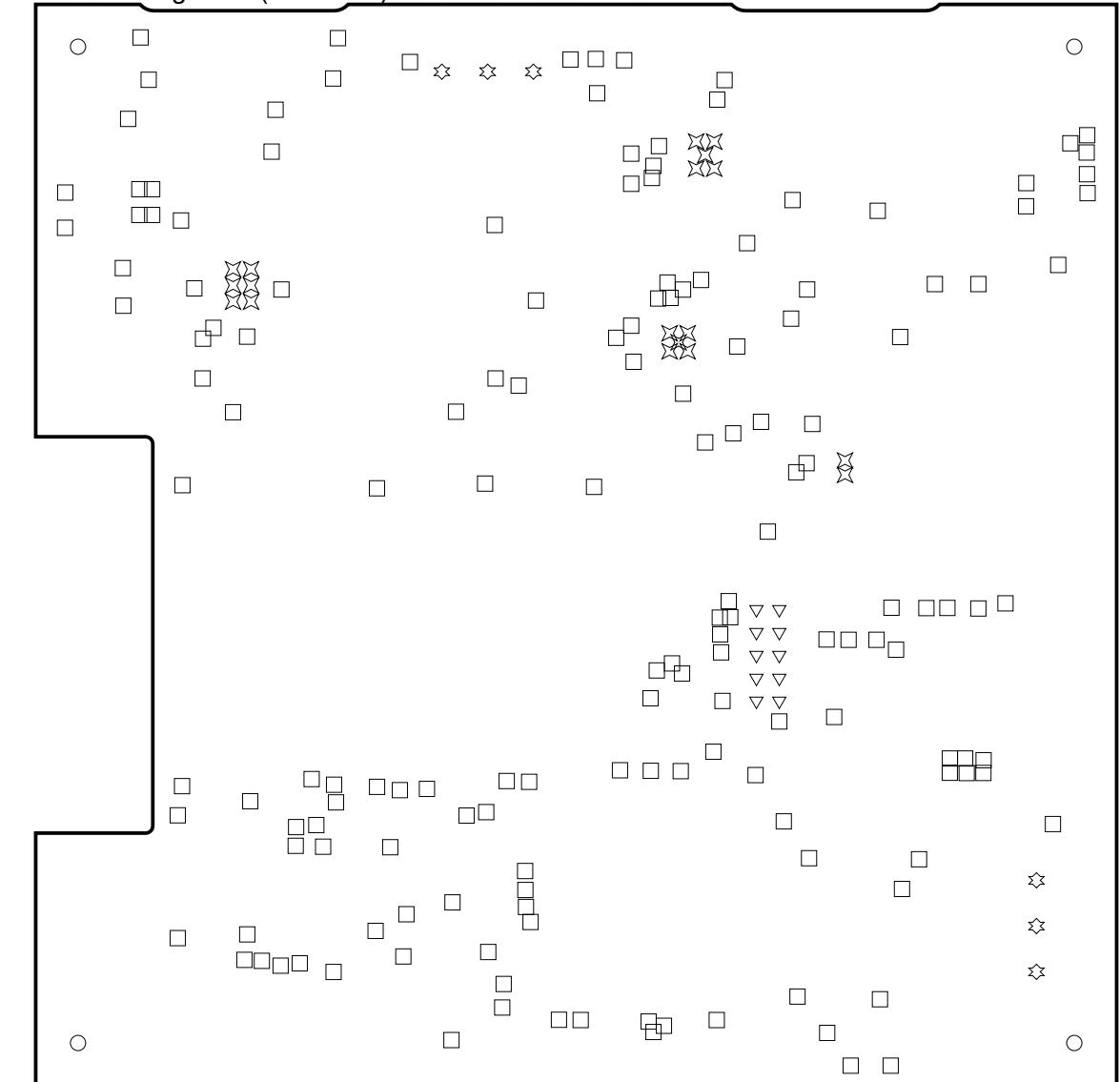
REV STATUS OF SHEETS		REV						DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET									

REVISIONS		DESCRIPTION	DATE	APPROVED

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
☒	18	0.20mm	Plated	
□	162	0.20mm	Plated	
▽	10	0.65mm	Plated	
☒	6	1.27mm	Plated	
○	4	2.70mm	Plated	
	200 Total			

Drill Drawing View (Scale 5:2)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Xitong Zheng Xitong Zheng

DESIGNER: Chenhong Liang Chenhong

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY USED ON

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

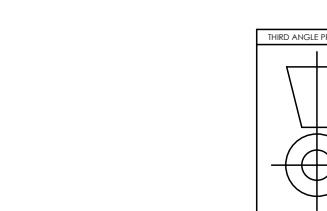
TITLE: Thinking team project

=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO REV:

SCALE: FILE NAME: StarterBoardFabrication.PCDBdwf SHEET: 2 OF 12



A

B

C

D

E

F

DWG NO:
=DOC_NO_ASSY_.lfe

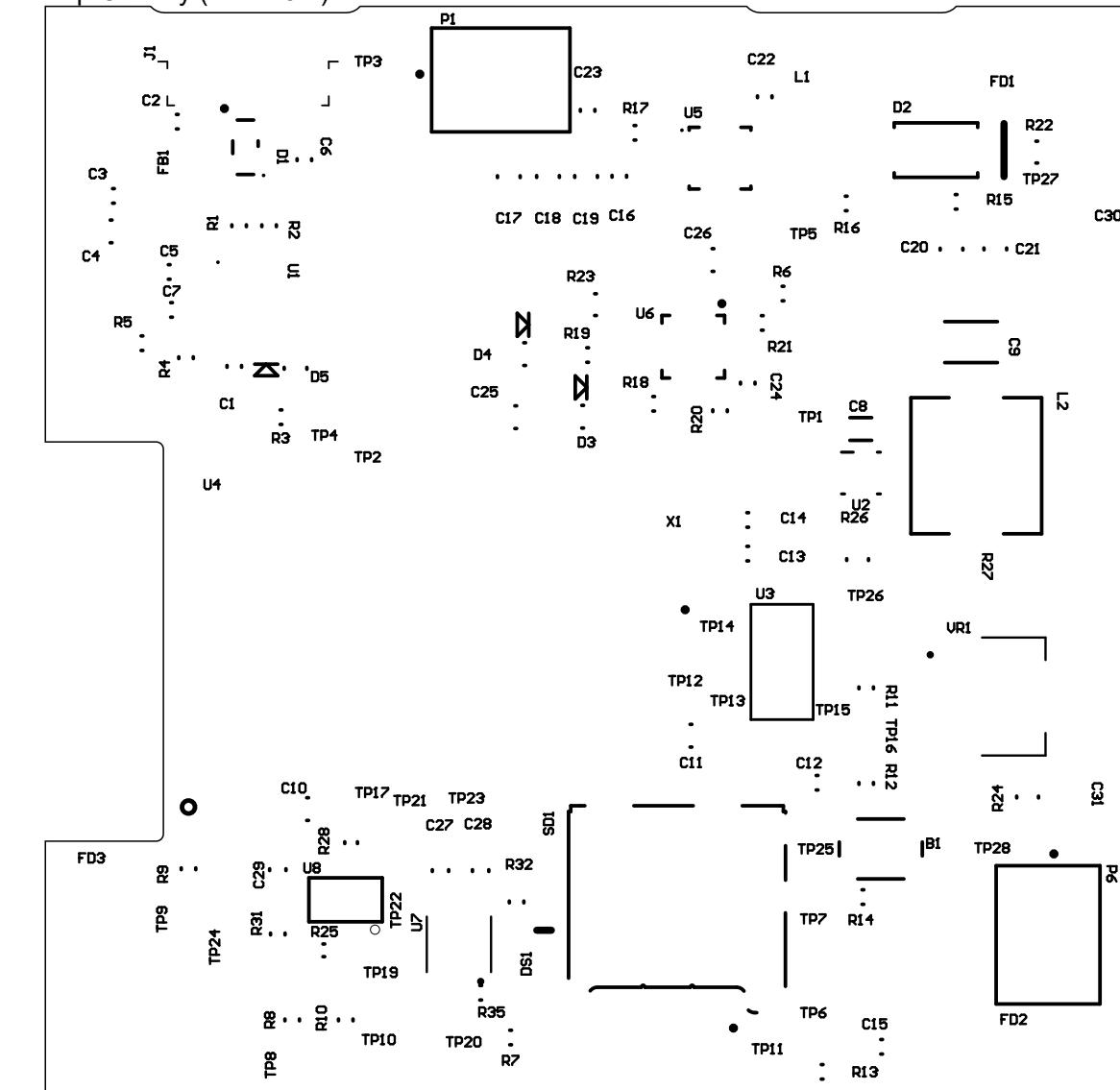
REV:

.lfe

DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		ZONE	REV	DESCRIPTION	DATE	APPROVED

Top Overlay (Scale 5:2)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Xitong Zheng Xitong Zheng

DESIGNER: Chenhong Liang Chenhong

CHECKER: =PCB_CHECKER =PCB_CHECKE

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

PCB DOC: =PCB_DWG_NO

APPLICATION

=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: Thinking team project =PCB_TITLE_2

SIZE: CAGE CODE: DWG NO: REV:
B =CAGE_CO

SCALE: FILE NAME: StarterBoardFabrication.PCDBdwf SHEET: 3 OF 12

Altium™

A

B

C

D

E

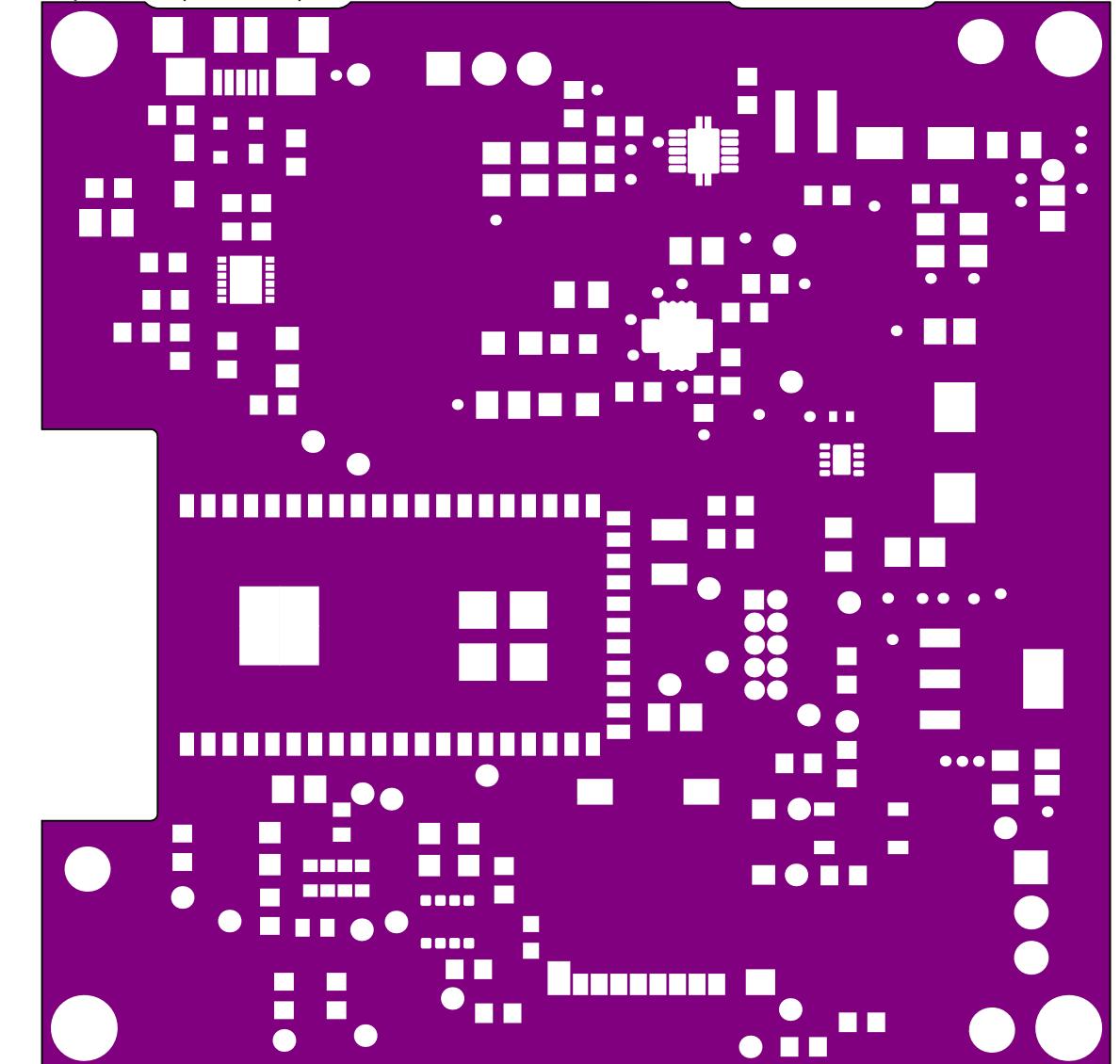
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

Top Solder (Scale 5:2)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Xitong Zheng Xitong Zheng

DESIGNER: Chenhong Liang Chenhong

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
Thinking team project
=PCB_TITLE_2

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: .Item

SIZE: CAGE CODE: DWG NO: REV:

B =CAGE_CO

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 4 OF 12



A

B

C

D

E

F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

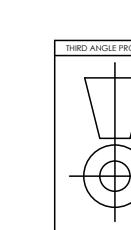
REV STATUS OF SHEETS		REV					DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET								

REVISIONS		DESCRIPTION	DATE	APPROVED

Top Paste (Scale 5:2)



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE
ENGINEER: Xitong Zheng	Xitong Zheng	
DESIGNER: Chenhong Liang	Chenhong	
CHECKER: =PCB_CHECKER	=PCB_CHECKER	
BOM DOC:	Reference Documents	
ASSY DOC:	=DOC_NO_BOM	
SCH DOC:	=DOC_NO_FAB_DWG	
PCB DOC:	=PCB_DWG_NO	
APPLICATION		



=Address1	
=Address2	
=Address3	
=Address4	
DESIGN ITEM: .Item	
DESIGN ITEM REVISION: .ItemRevision	
TITLE: Thinking team project	
=PCB_TITLE_2	
SIZE: B	CAGE CODE: =CAGE_CO
DWG NO:	
REV: .lfe	
FILE NAME: StarterBoardFabrication.PCDBdwf	SCALE: 5 OF 12

Altium™=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE: Thinking team project

=PCB_TITLE_2

SIZE: B

CAGE CODE: =CAGE_CO

DWG NO: .lfe

REV: .lfe

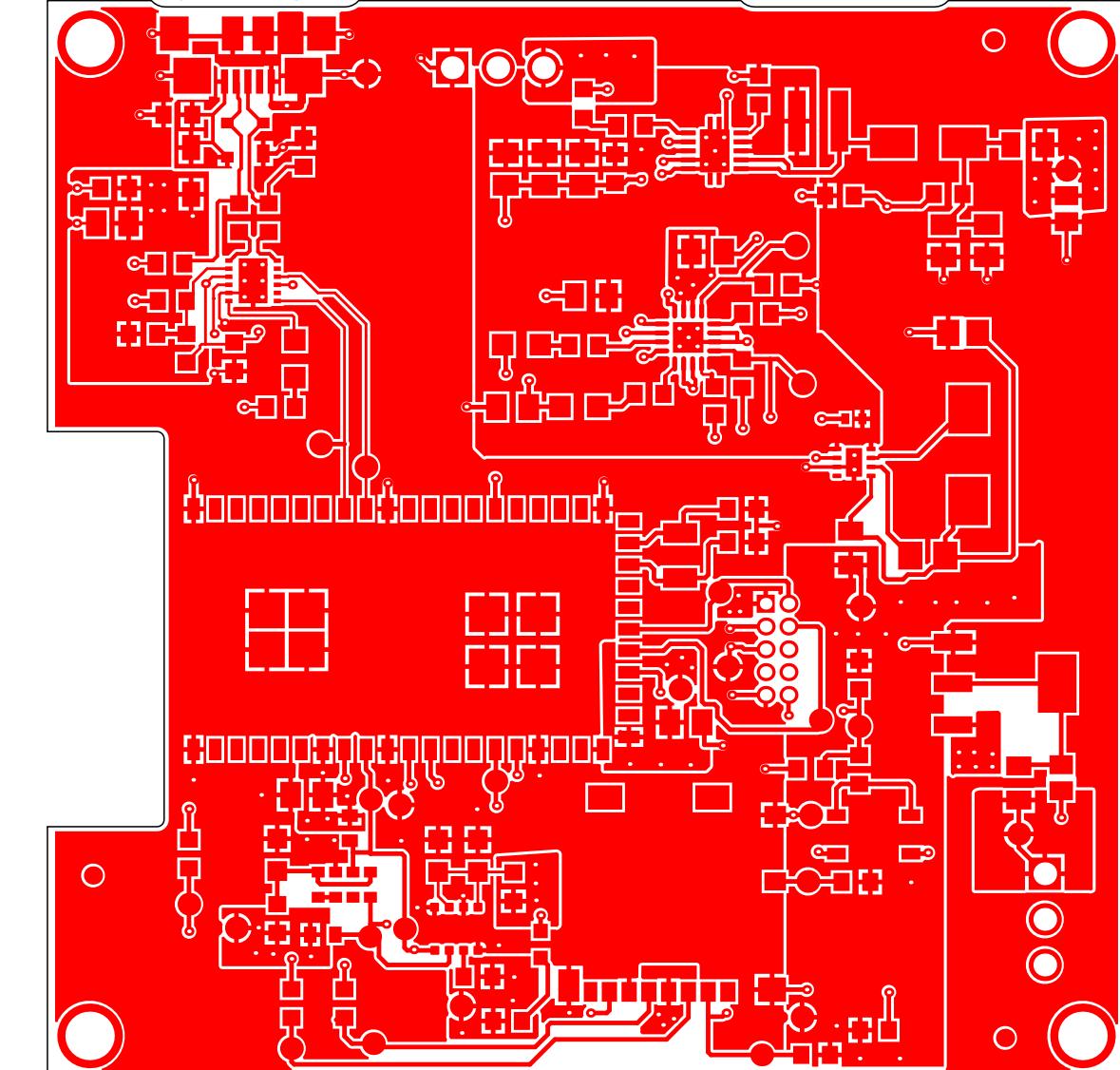
FILE NAME: StarterBoardFabrication.PCDBdwf

SCALE: 5 OF 12

DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		
DESCRIPTION	DATE	APPROVED

Top Layer (Scale 5:2)



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium Thinking team project =PCB_TITLE_2
ENGINEER: Xitong Zheng	Xitong Zheng		
DESIGNER: Chenhong Liang	Chenhong		
CHECKER: =PCB_CHECKER	=PCB_CHECKER	Reference Documents	
BOM DOC: =DOC_NO_BOM			
ASSY DOC: =DOC_NO_FAB_DWG			
SCH DOC: =DOC_NO_SCH_DWG			
NEXT ASSY	USED ON	PCB DOC: =PCB_DWG_NO	
APPLICATION			
		SCALE: 6 OF 12	
		FILE NAME: StarterBoardFabrication.PCBDwf	
		DWG NO: .lfe	
		CAGE CODE: B =CAGE_CO	
		REV: 6	

A

B

C

D

E

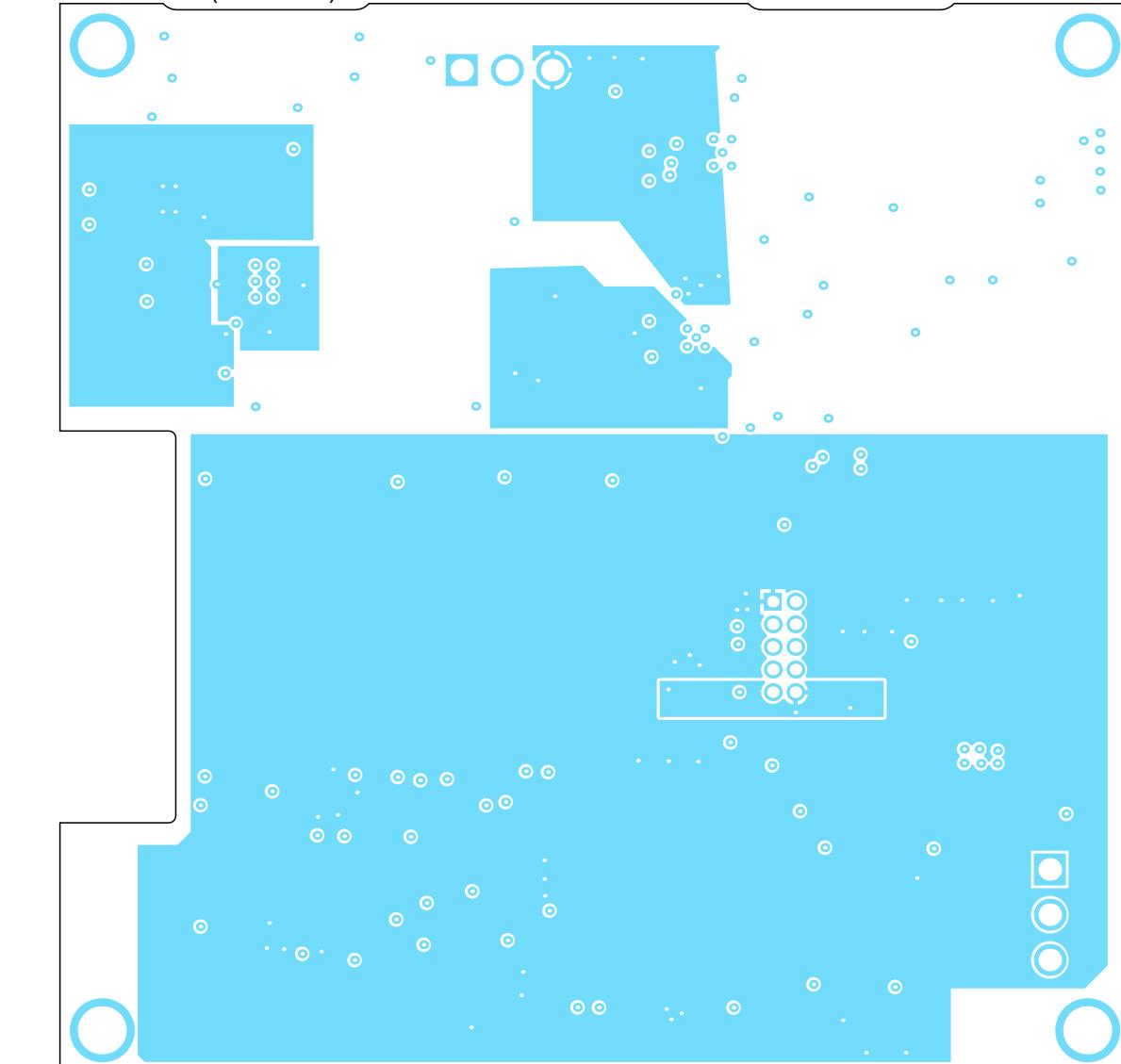
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

PowerPlane (Scale 5:2)



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium Thinking team project =PCB_TITLE_2
ENGINEER: Xitong Zheng	Xitong Zheng		
DESIGNER: Chenhong Liang	Chenhong		
CHECKER: =PCB_CHECKER	=PCB_CHECKER		
BOM DOC: =DOC_NO_BOM	Reference Documents		
ASSY DOC: =DOC_NO_FAB_DWG			
SCH DOC: =DOC_NO_SCH_DWG			
PCB DOC: =PCB_DWG_NO			
APPLICATION			
SIZE: B	CAGE CODE: =CAGE_CO	DWG NO: .lfe	REV: .ItemRevision
FILE NAME: StarterBoardFabrication.PCBDwf			
SCALE: 7 OF 12			

A

B

C

D

E

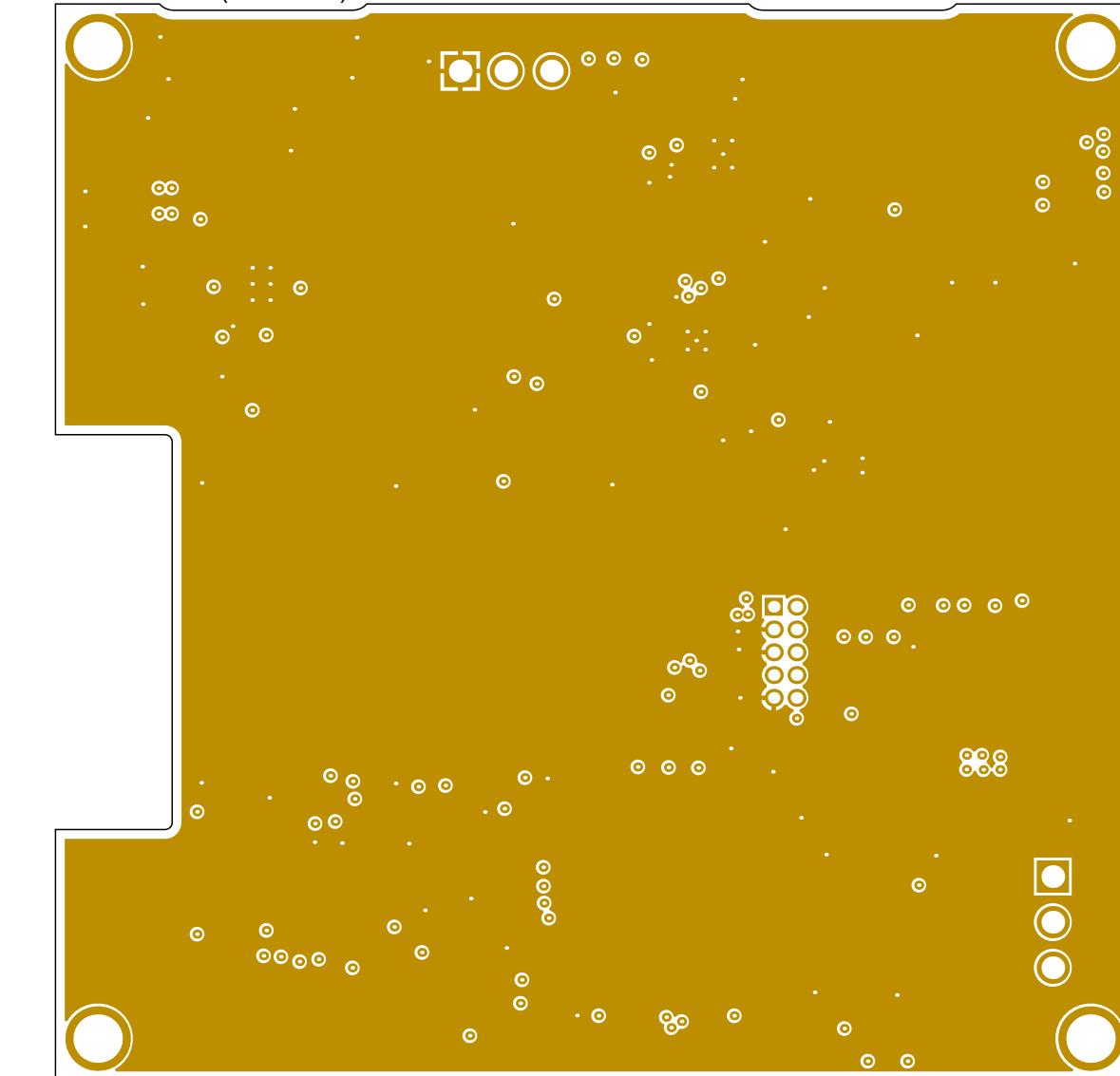
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

GroundPlane (Scale 5:2)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Xitong Zheng Xitong Zheng

DESIGNER: Chenhong Liang Chenhong

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY USED ON PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
 TM
 =Address1
 =Address2
 =Address3
 =Address4

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: Thinking team project

=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO: REV:

B =CAGE_CO

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 8 OF 12



A

B

C

D

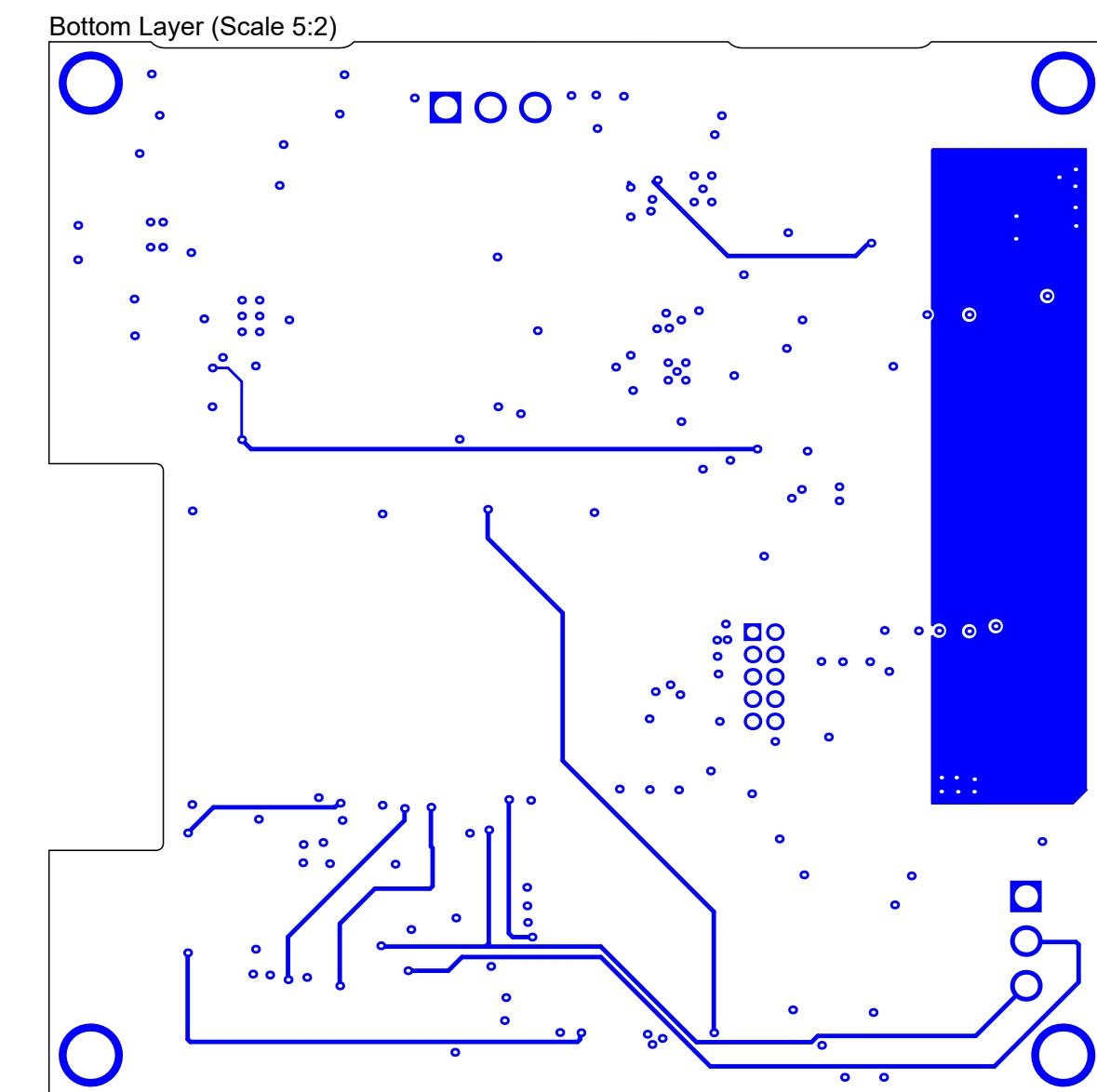
E

F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS		REV					DWG NO.: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET								

REVISIONS		DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER		APPROVALS	DATE	Altium Thinking team project =PCB_TITLE_2
ENGINEER:	Xitong Zheng	Xitong Zheng	=Address1 =Address2 =Address3 =Address4	
DESIGNER:	Chenhong Liang	Chenhong	DESIGN ITEM: .Item	
CHECKER:	=PCB_CHECKER	=PCB_CHECKER	DESIGN ITEM REVISION: .ItemRevision	
Reference Documents		BOM DOC: =DOC_NO_BOM		
		ASSY DOC: =DOC_NO_FAB_DWG		
		SCH DOC: =DOC_NO_SCH_DWG		
NEXT ASSY	USED ON	PCB DOC: =PCB_DWG_NO		
APPLICATION		SCALE: 1:1	FILE NAME: StarterBoardFabrication.PCBDwf	
		DWG NO: B =CAGE_CO	REV: 9 OF 12	

A

B

C

D

E

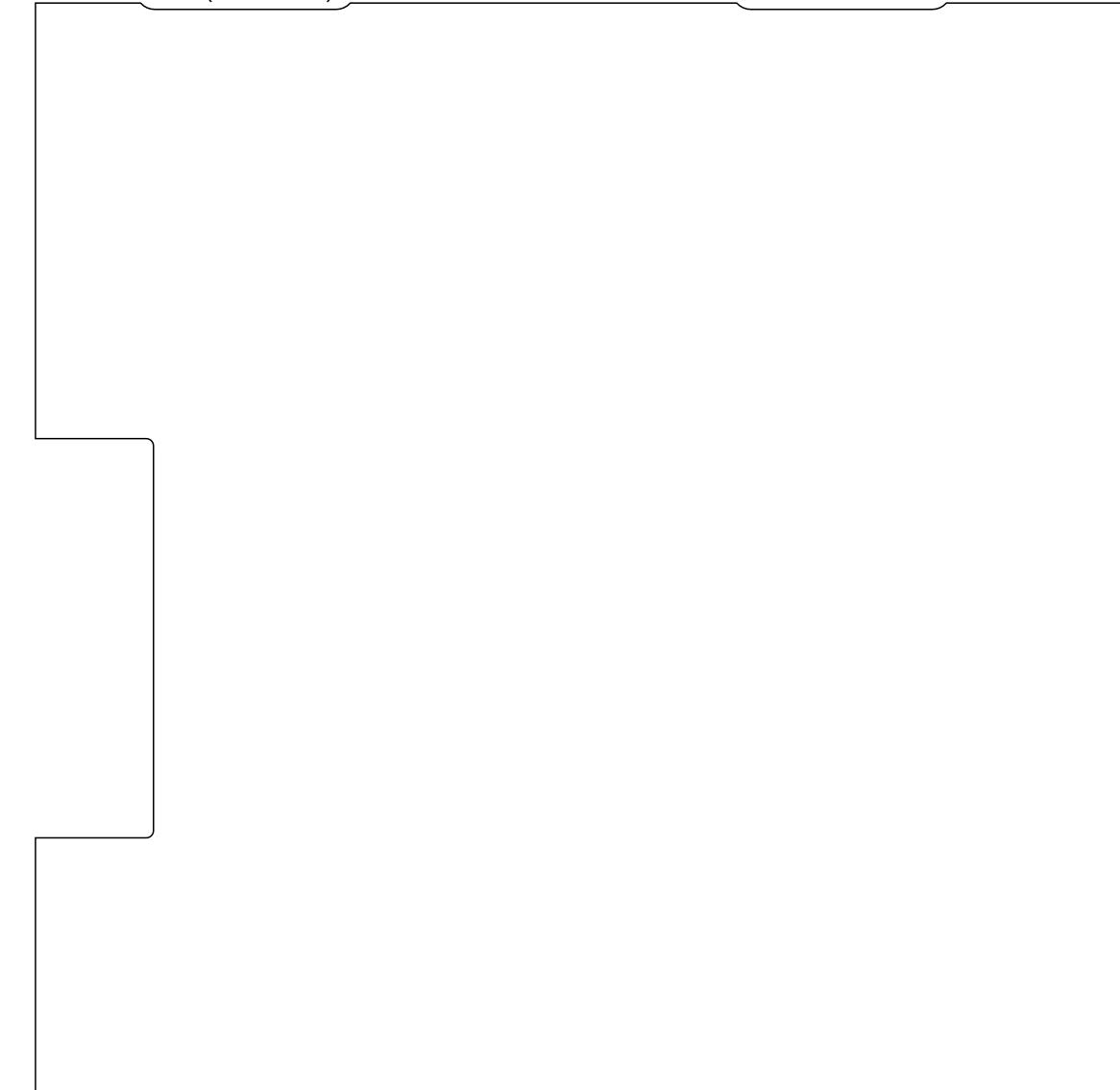
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

Bottom Paste (Scale 5:2)



.lt

DWG NO:
=DOC_NO_ASSY_

.lfe

4

PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Xitong Zheng Xitong Zheng

DESIGNER: Chenhong Liang Chenhong

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY USED ON PCB DOC: =PCB_DWG_NO

APPLICATION

Altium™=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: Thinking team project

=PCB_TITLE_2

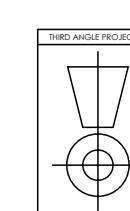
SIZE: CAGE CODE: DWG NO: REV:

B =CAGE_CO

10

OF

12



A

B

C

D

E

F

A

B

C

D

E

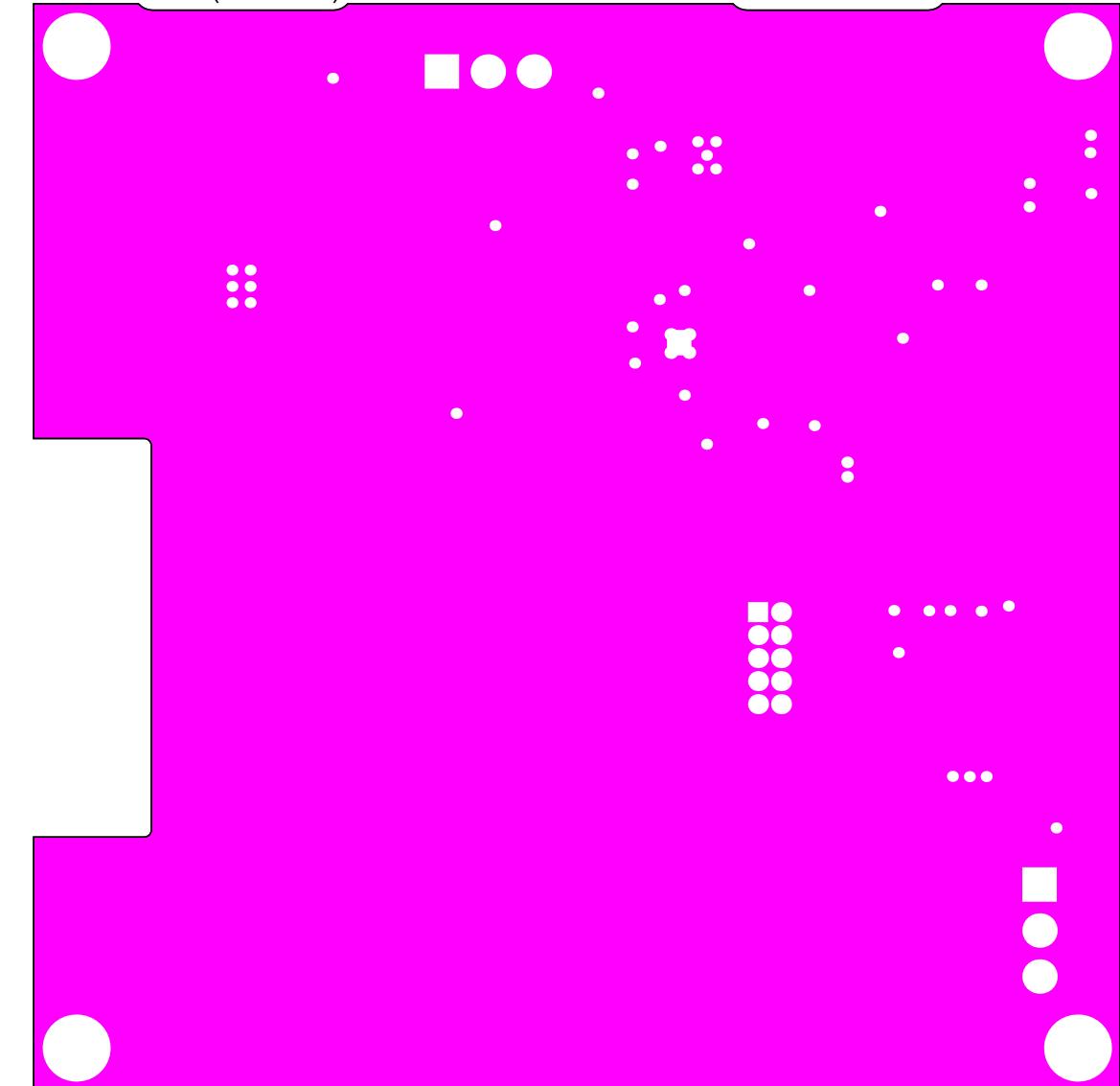
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

Bottom Solder (Scale 5:2)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Xitong Zheng Xitong Zheng

DESIGNER: Chenhong Liang Chenhong

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY USED ON PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
 TM
 =Address1
 =Address2
 =Address3
 =Address4

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

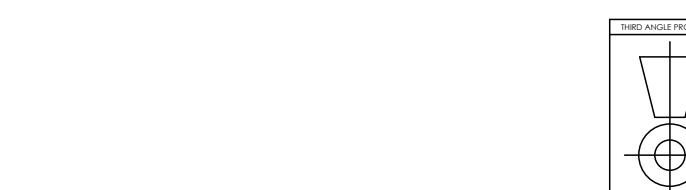
TITLE: Thinking team project

=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO: REV:

B =CAGE_CO

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 11 OF 12



A

B

C

D

E

F

.lt

DWG NO: =DOC_NO_ASSY_.lfe

4

A

B

C

D

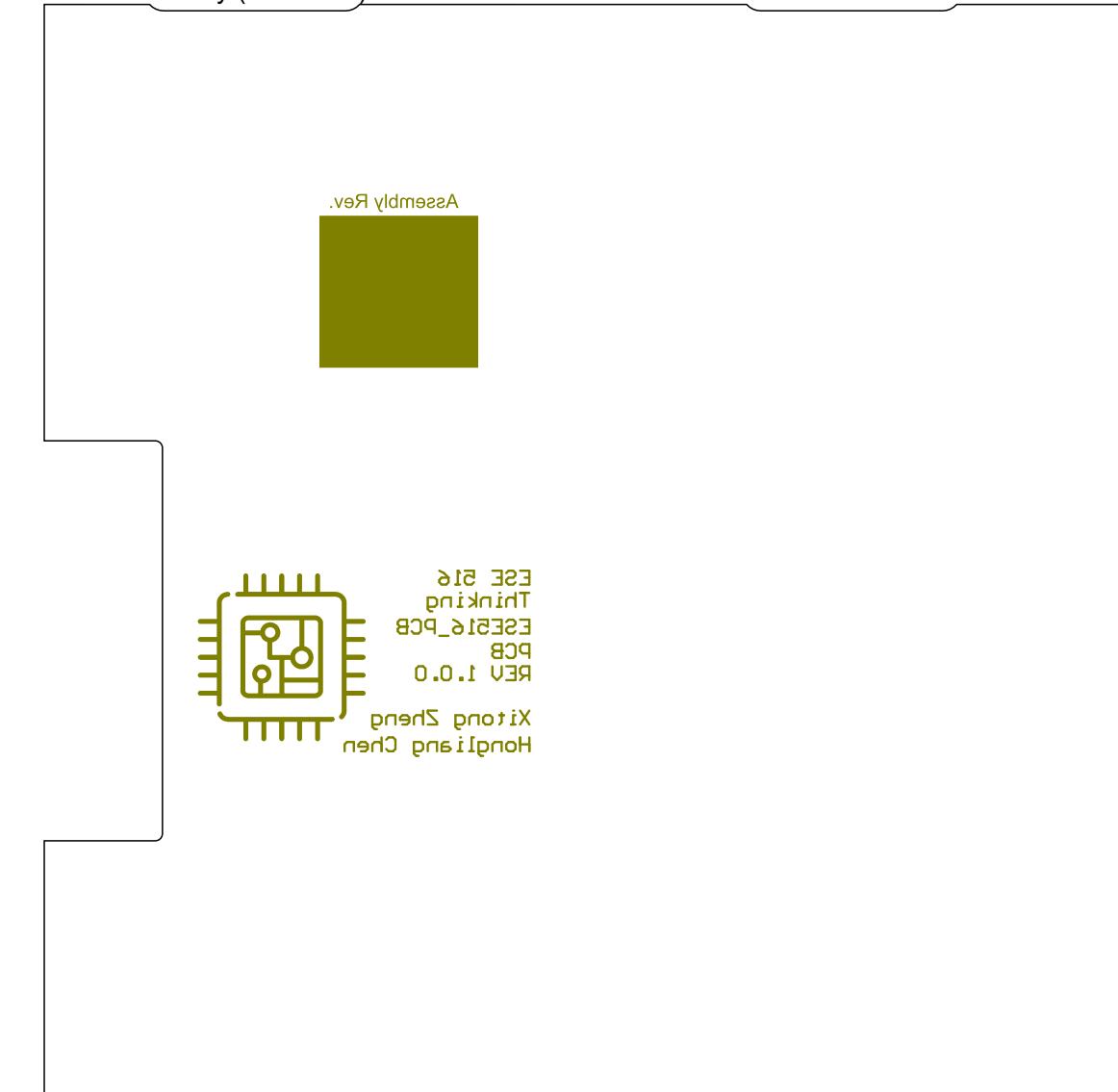
E

F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS		REV												DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET															
ZONE															
REV															
DESCRIPTION															
DATE															
APPROVED															

Bottom Overlay (Scale 5:2)



PART NO: =PCB_PART_NUMBER

APPROVALS

DATE

ENGINEER:

Xitong Zheng

DESIGNER:

Chenhong Liang

CHECKER:

=PCB_CHECKER

=PCB_CHECKER

Reference Documents

Altium
TM

=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE: Thinking team project

=PCB_TITLE_2

SIZE: CAGE CODE:

DWG NO:

B

REV:

=CAGE_CO

SCALE:

FILE NAME:

StarterBoardFabrication.PCBDwf

SHEET: 12 OF 12

A

B

C

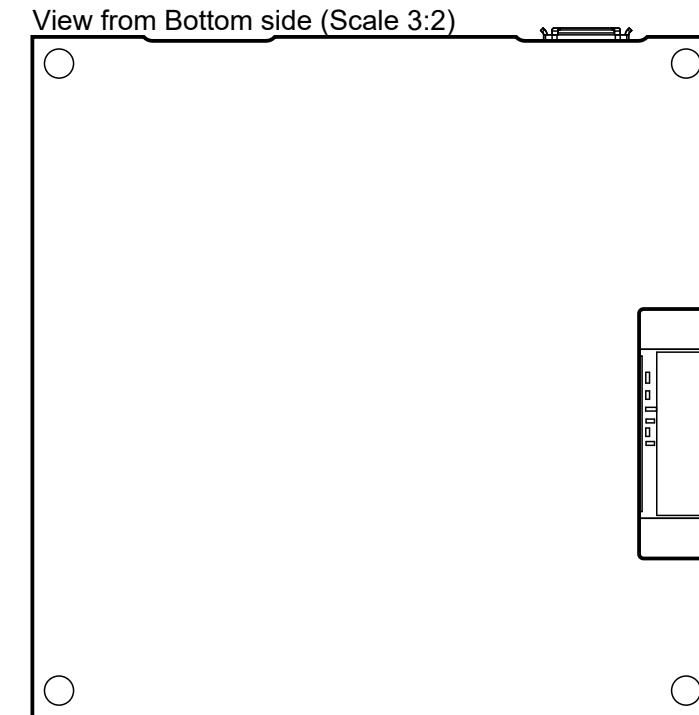
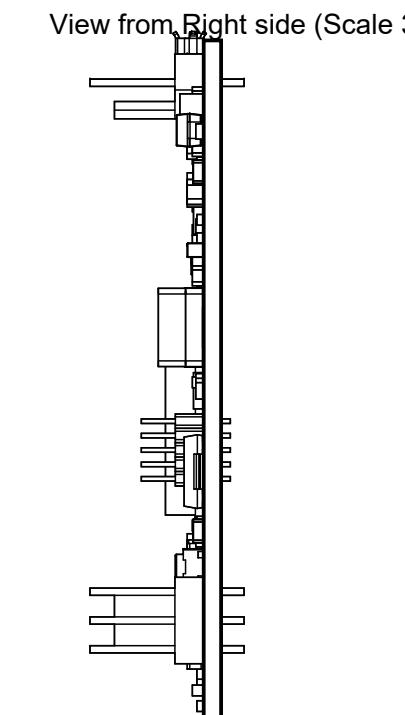
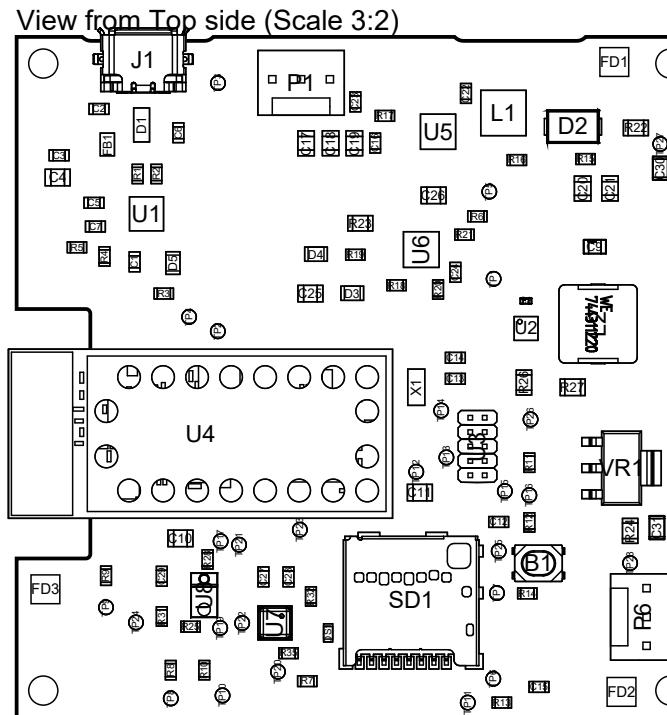
D

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

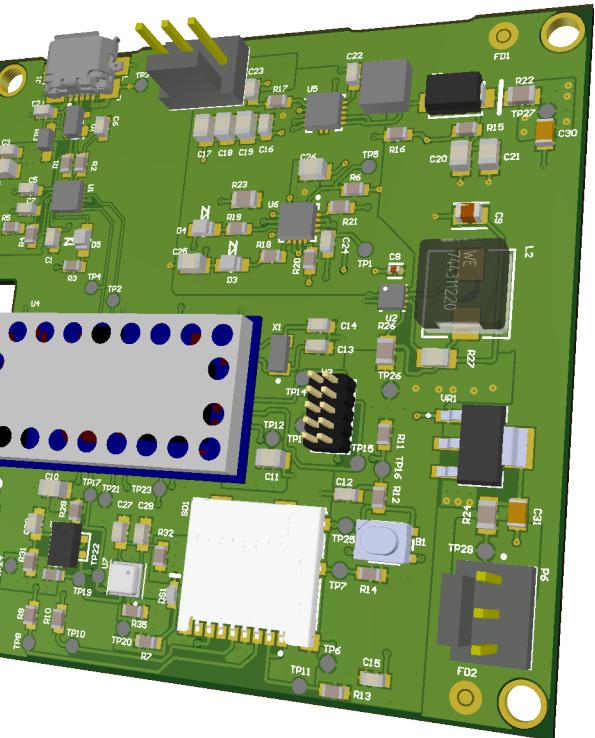
Notes (Unless otherwise specified):

NOTES:

1. THIS ITEM IS ELECTROSTATIC SENSITIVE AND SHALL BE HANDLED ACCORDINGLY
2. WORKMANSHIP WILL CONFORM TO IPC-610 CLASS 2, IPC-7711 WILL APPLY TO ALL REQUIRED REWORK OR MODIFICATION
3. ASSEMBLY IS TO BE IDENTIFIED BY A LABEL INDICATING- SERIAL NUMBER PART NUMBER and REVISION VENDOR DATE CODE
4. THE SUPPLIED INSERTION DATA FOR THIS PCBA IS PROVIDED TO ASSIST PROGRAMMING, COMPONENT OFFSET AND ROTATION ARE RELATIVE TO THE ENGINEERING DESIGN ENVIRONMENT AND MAY NOT MATCH REEL PACKAGING OR FEED ORIENTATION, COMPONENTS, ESPECIALLY POLARIZED PARTS, MUST BE VERIFIED AGAINST THE ACTUAL PCBA DRAWING TO INSURE PROPER INSTALLATION



Realistic View

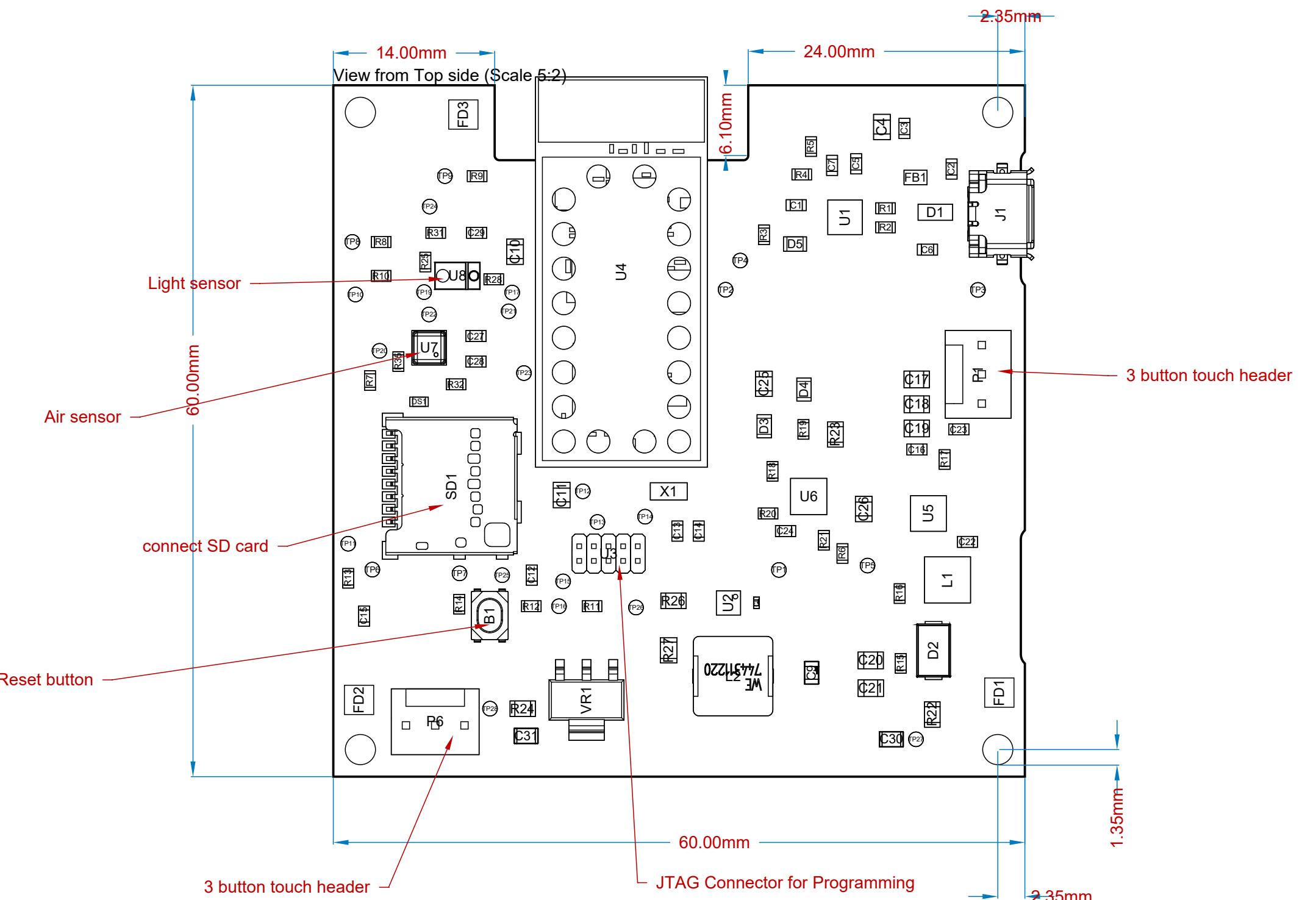


APPROVALS		DATE	=Address1			
ENGINEER:	Xitong Zheng	Xitong	=Address2			
DESIGNER:	Chenhong Liang	Chenhong	=Address3			
CHECKER:	=PCB_CHECKER	=PCB_CHECKER	=Address4			
Reference Documents						
BOM DOC:	=DOC_NO_BOM					
ASSY DOC:	=DOC_NO_FAB_DWG					
SCH DOC:	=DOC_NO_SCH_DWG					
PCB DOC:	=PCB_DWG_NO					
APPLICATION						
THIRD ANGLE PROJECTION						
SIZE: B	CAGE CODE: =CAGE_CO	DWG NO:				
SCALE: 1	FILE NAME: StarterBoardAssembly.PCBDwf	REV: 1	OF	3		

Altium
Thinking Team Project

=PCB_TITLE_2

REV STATUS OF SHEETS				REV				DWG NO.: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET				ZONE	REV	DESCRIPTION	DATE	APPROVED	



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Xitong Zheng Xitong

DESIGNER: Chenhong Liang Chenhong

CHECKER: =PCB_CHECKER =PCB_CHECKE

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

PCB DOC: =PCB_DWG_NO

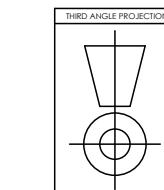
APPLICATION

=Address1
=Address2
=Address3
=Address4

Altium™
DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision
TITLE: Thinking Team Project
=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO REV:



APPLICATION

FILE NAME: StarterBoardAssembly.PCBDwf

A

B

C

D

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe	ZONE	REV	REVISIONS
REV STATUS OF SHEETS	SHEET			DESCRIPTION
				DATE APPROVED

Bill Of Materials

Line #	Designator	Name	Quantity
1	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28	0.1" Pad	27
2	R20, R21	1K13 1%	2
3	R3, R5, R6, R7, R18, R19	1K 1%	6
4	C12, C16, C24	1uF 16V	3
5	C4, C25, C26	4.7uF 16V	3
6	R11, R13, R14	10K 1%, 10K 1% 0603(1608)	3
7	C2	10nF 16V	1
8	C10, C11	10uF 16V, CAP 10uF 16V 0805(2012)	2
9	C13, C14	18pF 16V	2
10	C17, C18, C19, C20, C21	22uF 10V	5
11	R1, R2, R8, R9, R10	27R 1%	5
12	R16	39K 1% 0603(1608)	1
13	FD1, FD2, FD3	40x100mm	3
14	C5, C6	47pF 16V	2
15	R17	68K1 1%	1
16	C1, C3, C7, C15, C22	100nF 16V, CAP 100nF 16V 0603(1608)	5
17	R12	100R 1%	1
18	R15	150K 1% 0603(1608)	1
19	SD1	104031-0811	1
20	P1, P6	640456-3	2
21	U3	20021111-00010T4LF	1
22	X1	ABS07-32.768KHz-T	1
23	D2	B340A-13-F	1
24	FB1	BLM21PG221SN1D	1
25	U6	BQ24075RGTRG4	1
26	C23	CAP 820pF 10V 0603(1608)	1
27	U1	FT234XD-R	1
28	R4, R31, R32, R35	Jumper	4
29	R22, R23, R24, R26	Jumper	4
30	D3, D5	LTST-C170CKT	2
31	D4	LTST-C170GKT	1
32	DS1	LTST-C191KGKT	1
33	U8	APDS-9960	1
34	D1	PRTR5V0U2X,215	1
35	B1	PTS810 SJK 250 SMTR LFS	1
36	U4	SAMW25H18-MR510PB	1
37	U5	TPS61087DRCR	1
38	L1	XFL4020-102MEC	1
39	J1	ZX62R-B-5P	1
40	U7	BME680	1
41	C27, C28, C29	CAP 100nF 6.3V 0603(1608)	3
42	VR1	LM1117MPX-5.0/NOPB	1
43	C8	10 uF	1
44	R25, R28	4K22 1% 0603(1608)	2
45	R27	178 kohm	1
46	C30, C31	10 uF	2
47	C9	22 uF	1
48	U2	TPS62082DSGR	1
49	L2	1uH 5.06mOhm	1

THIRD ANGLE PROJECTION	APPROVALS	DATE	Altium Thinking Team Project =PCB_TITLE_2
	ENGINEER:	Xitong Zheng	
	DESIGNER:	Chenhong Liang	
	CHECKER:	=PCB_CHECKER	
	Reference Documents		
	BOM DOC:	=DOC_NO_BOM	
	ASSY DOC:	=DOC_NO_FAB_DWG	
	SCH DOC:	=DOC_NO_SCH_DWG	
NEXT ASSY	USED ON	PCB DOC:	=PCB_DWG_NO
	APPLICATION	SCALE:	FILE NAME: StarterBoardAssembly.PCBDwf
		REV:	3 OF 3