DLP6500FYE 数字微镜器件 (DMD)

1 特性

- 高分辨率 WQXGA (1920x1080) 阵列，微镜数超过 2 百万
  - 0.65 英寸微镜阵列对角线
  - 7.56µm 微镜间距
  - ±12° 微镜倾斜角（相对于平面）
  - 2.5µs 微镜交叉时间
  - 设计用于边缘照明
- 设计用于宽频带可见光 (420nm – 700nm)
  - 窗口传输 97%（单通、通过双窗面）
  - 微镜反射率 88%
  - 阵列衍射效率 86%
  - 阵列填充因子 92%
- 两条 16 位低压差分信令 (LVDS)、双倍数据速率 (DDR) 输入数据总线
- 专用 DLPC900 控制器，支持 9500Hz（1 位二进制）和 250Hz（8 位灰度）高速模式速率
- 高达 400MHz 的输入数据时钟速率
- 集成微镜驱动器电路

2 应用

- 工业
  - 针对机器视觉和质量控制的 3D 扫描仪
  - 3D 打印
  - 直接成像平版印刷术
  - 激光打标和修复
- 医疗
  - 眼科
  - 针对四肢和皮肤测量的 3D 扫描仪
  - 高光谱成像
  - 高光谱扫描
- 显示屏
  - 3D 成像显微镜
  - 智能和自适应照明

3 说明

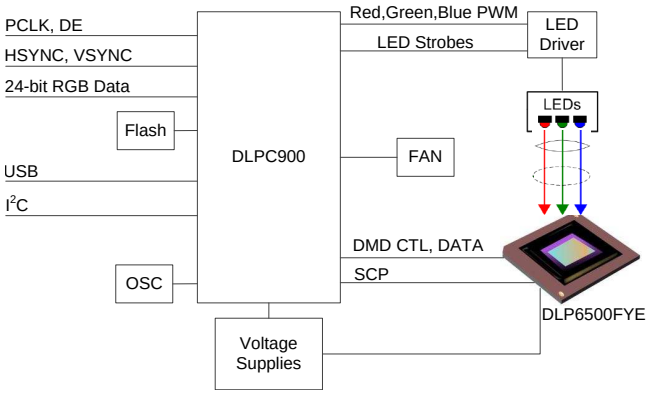
高分辨率 0.65 1080p 数字微镜器件 (DMD) 是一款可调制入射光幅度、方向和/或位相的空间照明调制器 (SLM)，微镜数达 2 百万以上。 DLP6500FYE 具有独特的功能，非常适用于广泛的工业、医疗和高级成像应用。 DLP6500FYE 需要与 DLPC900 数字控制器结合使用才能实现可靠功能和操作。 此专用芯片组可在高速条件下提供全高清 (HD) 分辨率，并且能够轻松集成到多种终端设备解决方案中。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLP6500	FYE (350)	40.6mm × 31.8mm × 6mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化图表



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4 修订历史记录

日期	修订版本	注释
2014 年 10 月	*	最初发布。

5 Pin Configuration and Functions

Package Connector Terminals
(Bottom View) for FYE (350)

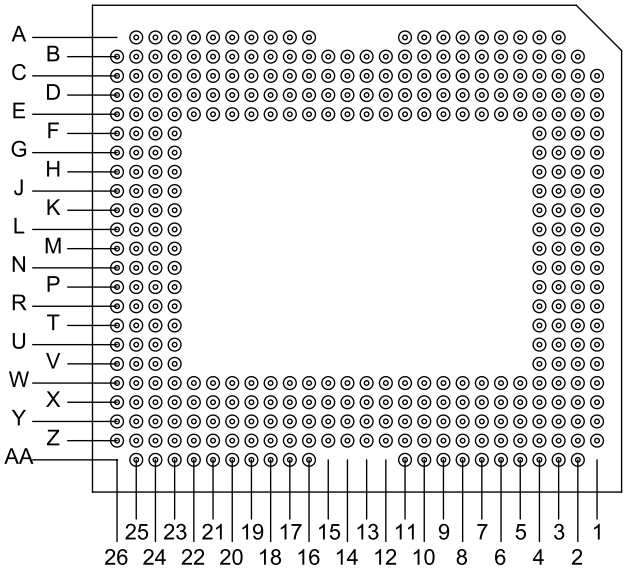


Table 1. Pin Functions

PIN(1)		TYPE (I/O/P)	SIGNAL	DATA RATE(2)	INTERNAL TERM(3)	DESCRIPTION	TRACE (mils)(4)
NAME	NO.						
DATA BUS A							
D_AN(0)	B14	Input	LVDS	DDR	Differential	Data, Negative	494.88
D_AN(1)	B15	Input	LVDS	DDR	Differential	Data, Negative	486.18
D_AN(2)	C16	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_AN(3)	K24	Input	LVDS	DDR	Differential	Data, Negative	485.67
D_AN(4)	B18	Input	LVDS	DDR	Differential	Data, Negative	494.76
D_AN(5)	L24	Input	LVDS	DDR	Differential	Data, Negative	490.63
D_AN(6)	C19	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_AN(7)	H24	Input	LVDS	DDR	Differential	Data, Negative	485.55
D_AN(8)	H23	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_AN(9)	B25	Input	LVDS	DDR	Differential	Data, Negative	485.59
D_AN(10)	D24	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_AN(11)	E25	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_AN(12)	F25	Input	LVDS	DDR	Differential	Data, Negative	490.04
D_AN(13)	H25	Input	LVDS	DDR	Differential	Data, Negative	485.91
D_AN(14)	L25	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_AN(15)	G24	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_AP(0)	C14	Input	LVDS	DDR	Differential	Data, Positive	494.84
D_AP(1)	B16	Input	LVDS	DDR	Differential	Data, Positive	486.22
D_AP(2)	C17	Input	LVDS	DDR	Differential	Data, Positive	494.65
D_AP(3)	K23	Input	LVDS	DDR	Differential	Data, Positive	488.42
D_AP(4)	B19	Input	LVDS	DDR	Differential	Data, Positive	495.16
D_AP(5)	L23	Input	LVDS	DDR	Differential	Data, Positive	490.67
D_AP(6)	C20	Input	LVDS	DDR	Differential	Data, Positive	498.11
D_AP(7)	J24	Input	LVDS	DDR	Differential	Data, Positive	486.22
D_AP(8)	J23	Input	LVDS	DDR	Differential	Data, Positive	495.47
D_AP(9)	C25	Input	LVDS	DDR	Differential	Data, Positive	485.94
D_AP(10)	E24	Input	LVDS	DDR	Differential	Data, Positive	495.16
D_AP(11)	D25	Input	LVDS	DDR	Differential	Data, Positive	494.13
D_AP(12)	G25	Input	LVDS	DDR	Differential	Data, Positive	488.98
D_AP(13)	J25	Input	LVDS	DDR	Differential	Data, Positive	492.56
D_AP(14)	K25	Input	LVDS	DDR	Differential	Data, Positive	495.16
D_AP(15)	F24	Input	LVDS	DDR	Differential	Data, Positive	495.16
DATA BUS B							
D_BN(0)	Z14	Input	LVDS	DDR	Differential	Data, Negative	494.92
D_BN(1)	Z15	Input	LVDS	DDR	Differential	Data, Negative	486.18
D_BN(2)	Y16	Input	LVDS	DDR	Differential	Data, Negative	496.46
D_BN(3)	P24	Input	LVDS	DDR	Differential	Data, Negative	493.74
D_BN(4)	Z18	Input	LVDS	DDR	Differential	Data, Negative	494.76
D_BN(5)	N24	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_BN(6)	Y19	Input	LVDS	DDR	Differential	Data, Negative	492.16
D_BN(7)	T24	Input	LVDS	DDR	Differential	Data, Negative	492.68

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.
(2) DDR = Double Data Rate.
SDR = Single Data Rate.
Refer to the *Timing Requirements* for specifications and relationships.
(3) Internal term = CMOS level internal termination. Refer to *Recommended Operating Conditions* for differential termination specification.
(4) Dielectric Constant for the DMD Type A ceramic package is approximately 9.6.
For the package trace lengths shown:
Propagation Speed = 11.8 / sqrt(9.6) = 3.808 in/ns.
Propagation Delay = 0.262 ns/in = 262 ps/in = 10.315 ps/mm.

Table 1. Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	DESCRIPTION	TRACE (mils)[4]
NAME	NO.						
D_BN(8)	T23	Input	LVDS	DDR	Differential	Data, Negative	484.45
D_BN(9)	Z25	Input	LVDS	DDR	Differential	Data, Negative	492.09
D_BN(10)	X24	Input	LVDS	DDR	Differential	Data, Negative	497.72
D_BN(11)	W25	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_BN(12)	V25	Input	LVDS	DDR	Differential	Data, Negative	484.17
D_BN(13)	T25	Input	LVDS	DDR	Differential	Data, Negative	481.42
D_BN(14)	N25	Input	LVDS	DDR	Differential	Data, Negative	495.16
D_BN(15)	U24	Input	LVDS	DDR	Differential	Data, Negative	489.8
D_BP(0)	Y14	Input	LVDS	DDR	Differential	Data, Positive	494.88
D_BP(1)	Z16	Input	LVDS	DDR	Differential	Data, Positive	486.26
D_BP(2)	Y17	Input	LVDS	DDR	Differential	Data, Positive	495.16
D_BP(3)	P23	Input	LVDS	DDR	Differential	Data, Positive	492.48
D_BP(4)	Z19	Input	LVDS	DDR	Differential	Data, Positive	495.16
D_BP(5)	N23	Input	LVDS	DDR	Differential	Data, Positive	497.99
D_BP(6)	Y20	Input	LVDS	DDR	Differential	Data, Positive	495.16
D_BP(7)	R24	Input	LVDS	DDR	Differential	Data, Positive	492.05
D_BP(8)	R23	Input	LVDS	DDR	Differential	Data, Positive	484.45
D_BP(9)	Y25	Input	LVDS	DDR	Differential	Data, Positive	492.24
D_BP(10)	W24	Input	LVDS	DDR	Differential	Data, Positive	495.16
D_BP(11)	X25	Input	LVDS	DDR	Differential	Data, Positive	494.72
D_BP(12)	U25	Input	LVDS	DDR	Differential	Data, Positive	483.78
D_BP(13)	R25	Input	LVDS	DDR	Differential	Data, Positive	489.13
D_BP(14)	P25	Input	LVDS	DDR	Differential	Data, Positive	499.53
D_BP(15)	V24	Input	LVDS	DDR	Differential	Data, Positive	488.66
SERIAL CONTROL							
SCTRL_AN	C23	Input	LVDS	DDR	Differential	Serial Control, Negative	492.95
SCTRL_BN	Y23	Input	LVDS	DDR	Differential	Serial Control, Negative	493.78
SCTRL_AP	C24	Input	LVDS	DDR	Differential	Serial Control, Positive	493.78
SCTRL_BP	Y24	Input	LVDS	DDR	Differential	Serial Control, Positive	493.11
CLOCKS							
DCLK_AN	B23	Input	LVDS		Differential	Clock, Negative	480.35
DCLK_BN	Z23	Input	LVDS		Differential	Clock, Negative	486.22
DCLK_AP	B22	Input	LVDS		Differential	Clock, Positive	485.83
DCLK_BP	Z22	Input	LVDS		Differential	Clock, Positive	491.93
SERIAL COMMUNICATIONS PORT (SCP)							
SCP_DO	B8	Output	LVCMOS	SDR		Serial Communications Port Output	
SCP_DI	B7	Input	LVCMOS	SDR	Pull-Down	Serial Communications Port Data Input	
SCP_CLK	B6	Input	LVCMOS		Pull-Down	Serial Communications Port Clock	
SCP_ENZ	C8	Input	LVCMOS		Pull-Down	Active-low Serial Communications Port Enable	
MICROMIRROR RESET CONTROL							
RESET_ADDR(0)	X9	Input	LVCMOS		Pull-Down	Reset Driver Address Select	
RESET_ADDR(1)	X8	Input	LVCMOS		Pull-Down	Reset Driver Address Select	
RESET_ADDR(2)	Z8	Input	LVCMOS		Pull-Down	Reset Driver Address Select	
RESET_ADDR(3)	Z7	Input	LVCMOS		Pull-Down	Reset Driver Address Select	
RESET_MODE(0)	W11	Input	LVCMOS		Pull-Down	Reset Driver Mode Select	
RESET_MODE(1)	Z10	Input	LVCMOS		Pull-Down	Reset Driver Mode Select	
RESET_SEL(0)	Y10	Input	LVCMOS		Pull-Down	Reset Driver Level Select	
RESET_SEL(1)	Y9	Input	LVCMOS		Pull-Down	Reset Driver Level Select	

Table 1. Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	DESCRIPTION	TRACE (mils)[4]
NAME	NO.						
RESET_STROBE	Y7	Input	LVCMOS		Pull-Down	Reset Address, Mode, & Level latched on rising-edge	
ENABLES and INTERRUPTS							
PWRDNZ	D2	Input	LVCMOS		Pull-Down	Active-low Device Reset	
RESET_OEZ	W7	Input	LVCMOS		Pull-Down	Active-low output enable for DMD reset driver circuits	
RESETZ	Z6	Input	LVCMOS		Pull-Down	Active-low sets Reset circuits in known VOFFSET state	
RESET_IRQZ	Z5	Output	LVCMOS			Active-low, output interrupt to ASIC	
VOLTAGE REGULATOR MONITORING							
PG_BIAS	E11	Input	LVCMOS		Pull-Up	Active-low fault from external VBIAS regulator	
PG_OFFSET	B10	Input	LVCMOS		Pull-Up	Active-low fault from external VOFFSET regulator	
PG_RESET	D11	Input	LVCMOS		Pull-Up	Active-low fault from external VRESET regulator	
EN_BIAS	D9	Output	LVCMOS			Active-high enable for external VBIAS regulator	
EN_OFFSET	C9	Output	LVCMOS			Active-high enable for external VOFFSET regulator	
EN_RESET	E9	Output	LVCMOS			Active-high enable for external VRESET regulator	
LEAVE PIN UNCONNECTED							
MBRST(0)	C2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(1)	C3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(2)	C5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(3)	C4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(4)	E5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(5)	E4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(6)	E3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(7)	G4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(8)	G3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(9)	G2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(10)	J4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(11)	J3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(12)	J2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(13)	L4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(14)	L3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(15)	L2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	

Table 1. Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	DESCRIPTION	TRACE (mils)[4]
NAME	NO.						
LEAVE PIN UNCONNECTED							
RESERVED_PFE	E7	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_TM	D13	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_XI1	E13	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_TP0	W12	Input	Analog			For proper DMD operation, do not connect	
RESERVED_TP1	Y11	Input	Analog			For proper DMD operation, do not connect	
RESERVED_TP2	X11	Input	Analog			For proper DMD operation, do not connect	
LEAVE PIN UNCONNECTED							
RESERVED_BA	Y12	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_BB	C12	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_TS	D5	Output	LVCMOS			For proper DMD operation, do not connect	
LEAVE PIN UNCONNECTED							
NO CONNECT	B11					For proper DMD operation, do not connect	
NO CONNECT	C11					For proper DMD operation, do not connect	
NO CONNECT	C13					For proper DMD operation, do not connect	
NO CONNECT	E12					For proper DMD operation, do not connect	
NO CONNECT	E14					For proper DMD operation, do not connect	
NO CONNECT	E23					For proper DMD operation, do not connect	
NO CONNECT	H4					For proper DMD operation, do not connect	
NO CONNECT	N2					For proper DMD operation, do not connect	
NO CONNECT	N3					For proper DMD operation, do not connect	
NO CONNECT	N4					For proper DMD operation, do not connect	
NO CONNECT	R2					For proper DMD operation, do not connect	
NO CONNECT	R3					For proper DMD operation, do not connect	
NO CONNECT	R4					For proper DMD operation, do not connect	
NO CONNECT	T4					For proper DMD operation, do not connect	
NO CONNECT	U2					For proper DMD operation, do not connect	
NO CONNECT	U3					For proper DMD operation, do not connect	
NO CONNECT	U4					For proper DMD operation, do not connect	
NO CONNECT	W3					For proper DMD operation, do not connect	
NO CONNECT	W4					For proper DMD operation, do not connect	

Table 1. Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	DESCRIPTION	TRACE (mils)[4]
NAME	NO.						
NO CONNECT	W5					For proper DMD operation, do not connect	
NO CONNECT	W13					For proper DMD operation, do not connect	
NO CONNECT	W14					For proper DMD operation, do not connect	
NO CONNECT	W23					For proper DMD operation, do not connect	
NO CONNECT	X4					For proper DMD operation, do not connect	
NO CONNECT	X5					For proper DMD operation, do not connect	
NO CONNECT	X13					For proper DMD operation, do not connect	
NO CONNECT	Y2					For proper DMD operation, do not connect	
NO CONNECT	Y3					For proper DMD operation, do not connect	
NO CONNECT	Y4					For proper DMD operation, do not connect	
NO CONNECT	Y5					For proper DMD operation, do not connect	
NO CONNECT	Z11					For proper DMD operation, do not connect	

PIN				TYPE (I/O/P)	SIGNAL	DESCRIPTION
NAME[1]	NO.	NO.	NO.			
VBIAS	A6	A7	A8	Power	Analog	Supply voltage for positive Bias level of Micromirror reset signal.
VBIAS	AA6	AA7	AA8	Power	Analog	Supply voltage for positive Bias level of Micromirror reset signal.
VOFFSET	A3	A4	A25	Power	Analog	Supply voltage for HVCMOS logic.
VOFFSET	B26	L26	M26	Power	Analog	Supply voltage for stepped high voltage at Micromirror address electrodes.
VOFFSET	N26	Z26	Z27	Power	Analog	Supply voltage for Offset level of MBRST(31:0).
VOFFSET	AA3	AA4	AA25	Power	Analog	
VRESET	G1	H1	J1	Power	Analog	Supply voltage for negative Reset level of Micromirror reset signal.
VRESET	R1	T1	U1	Power	Analog	Supply voltage for negative Reset level of Micromirror reset signal.
VCC	A9	B3	B5	Power	Analog	
VCC	B12	C1	C6	Power	Analog	
VCC	C10	D4	D6	Power	Analog	
VCC	D8	E1	E2	Power	Analog	Supply voltage for LVCMOS core logic.
VCC	E10	E15	E16	Power	Analog	Supply voltage for normal high level at Micromirror address electrodes.
VCC	E17	F3	H2	Power	Analog	Supply voltage for positive Offset level of Micromirror reset signal during Power Down sequence.
VCC	K1	K3	M4	Power	Analog	
VCC	P1	P3	T2	Power	Analog	
VCC	V3	W1	W2	Power	Analog	
VCC	W6	W9	W10	Power	Analog	
VCC	W15	W16	W17	Power	Analog	
VCC	X3	X6		Power	Analog	
VCC	Y1	Y8	Y13	Power	Analog	
VCC	Z1	Z3	Z12	Power	Analog	
VCC	AA2	AA9	AA10	Power	Analog	
VCCI	A16	A17	A18	Power	Analog	Supply voltage for LVDS receivers.

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.

PIN				TYPE (I/O/P)	SIGNAL	DESCRIPTION
NAME(1)	NO.	NO.	NO.			
VCCI	A20	A21	A23	Power	Analog	Supply voltage for LVDS receivers.
VCCI	AA16	AA17	AA18	Power	Analog	Supply voltage for LVDS receivers.
VCCI	AA20	AA21	AA23	Power	Analog	Supply voltage for LVDS receivers.
VSS	A5	A10	A11	Power	Analog	Device Ground. Common return for all power.
VSS	A19	A22	A24	Power	Analog	Device Ground. Common return for all power.
VSS	B2	B4	B9	Power	Analog	Device Ground. Common return for all power.
VSS	B13	B17	B20	Power	Analog	Device Ground. Common return for all power.
VSS	B21	B24	C7	Power	Analog	Device Ground. Common return for all power.
VSS	C15	C18	C21	Power	Analog	Device Ground. Common return for all power.
VSS	C22	C26	D1	Power	Analog	Device Ground. Common return for all power.
VSS	D3	D7	D10	Power	Analog	Device Ground. Common return for all power.
VSS	D12	D14	D15	Power	Analog	Device Ground. Common return for all power.
VSS	D16	D17	D18	Power	Analog	Device Ground. Common return for all power.
VSS	D19	D20	D21	Power	Analog	Device Ground. Common return for all power.
VSS	D22	D23	D26	Power	Analog	Device Ground. Common return for all power.
VSS	E6	E8	E18	Power	Analog	Device Ground. Common return for all power.
VSS	E19	E20	E21	Power	Analog	Device Ground. Common return for all power.
VSS	E22	E26	F1	Power	Analog	Device Ground. Common return for all power.
VSS	F2	F4	F23	Power	Analog	Device Ground. Common return for all power.
VSS	F26	G23	G26	Power	Analog	Device Ground. Common return for all power.
VSS	H3	H26	J26	Power	Analog	Device Ground. Common return for all power.
VSS	K2	K4	K26	Power	Analog	Device Ground. Common return for all power.
VSS	L1	M1	M2	Power	Analog	Device Ground. Common return for all power.
VSS	M3	M23	M24	Power	Analog	Device Ground. Common return for all power.
VSS	M25	N1	P2	Power	Analog	Device Ground. Common return for all power.
VSS	P4	P26	R26	Power	Analog	Device Ground. Common return for all power.
VSS	T3	T26	U23	Power	Analog	Device Ground. Common return for all power.
VSS	U26	V1	V2	Power	Analog	Device Ground. Common return for all power.
VSS	V4	V23	V26	Power	Analog	Device Ground. Common return for all power.
VSS	W8	W18	W19	Power	Analog	Device Ground. Common return for all power.
VSS	W20	W21	W22	Power	Analog	Device Ground. Common return for all power.
VSS	W26	X1	X2	Power	Analog	Device Ground. Common return for all power.
VSS	X7	X10	X12	Power	Analog	Device Ground. Common return for all power.
VSS	X14	X15	X16	Power	Analog	Device Ground. Common return for all power.
VSS	X17	X18	X19	Power	Analog	Device Ground. Common return for all power.
VSS	X20	X21	X22	Power	Analog	Device Ground. Common return for all power.
VSS	X23	X26	Y6	Power	Analog	Device Ground. Common return for all power.
VSS	Y15	Y18	Y21	Power	Analog	Device Ground. Common return for all power.
VSS	Y22	Y26	Z2	Power	Analog	Device Ground. Common return for all power.
VSS	Z4	Z9	Z13	Power	Analog	Device Ground. Common return for all power.
VSS	Z17	Z20	Z21	Power	Analog	Device Ground. Common return for all power.
VSS	Z24	AA5	AA11	Power	Analog	Device Ground. Common return for all power.
VSS	AA19	AA22	AA24	Power	Analog	Device Ground. Common return for all power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

SUPPLY VOLTAGES		MIN	MAX	UNIT
VCC	Supply voltage for LVCMOS core logic (2)	–0.5	4	V
VCCI	Supply voltage for LVDS receivers (2)	–0.5	4	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode (2) (3)	–0.5	9	V
VBIAS	Supply voltage for micromirror electrode (2)	–0.5	17	V
VRESET	Supply voltage for micromirror electrode (2)	–11	0.5	V
| VCC – VCCI |	Supply voltage delta (absolute value) (4)		0.3	V
| VBIAS – VOFFSET |	Supply voltage delta (absolute value) (5)		8.75	V
INPUT VOLTAGES				
	Input voltage for all other LVCMOS input pins (2)	–0.5	VCC + 0.15	V
	Input voltage for all other LVDS input pins (2) (6)	–0.5	VCCI + 0.15	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value) (7)		700	mV
I_{ID}	Input differential current (7)		7	mA
CLOCKS				
f_{clock}	Clock frequency for LVDS interface, DCLK_A		460	MHz
	Clock frequency for LVDS interface, DCLK_B		460	MHz
ENVIRONMENTAL				
T_{CASE}	Case temperature: operational (8) (9)	–20	90	ºC
	Case temperature: non–operational (9)	–40	90	ºC
	Dew Point (Operating and non-Operating)		81	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure above *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected
(3) VOFFSET supply transients must fall within specified voltages.
(4) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. Refer to *Power Supply Recommendations* for additional information.
(6) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential. .
(7) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors
(8) Exposure of the DMD simultaneously to any combination of the maximum operating conditions for case temperature, differential temperature, or illumination power density (see *Handling Ratings*).
(9) DMD Temperature is the worst-case of any test point shown in Figure 15, or the active array as calculated by the *Micromirror Array Temperature Calculation* .

6.2 Handling Ratings

PARAMETER(1) (2) (3)			MIN	MAX	UNIT
T_{stg}	DMD Storage Temperature		–40	85	°C
	Long-Term Storage Dew Point (4)			24	°C
	Short-Term Storage Dew Point(5)			28	°C
$V_{(ESD)}$	Electrostatic discharge	All pins, human body model (HBM), per ANSI/ESDA/JEDEC JS-001(6)		2000	V

(1) Handling Ratings are applicable before the DMD is installed in the final product.
(2) All CMOS devices require proper Electrostatic Discharge (ESD) handling procedures.
(3) As a best practice, TI recommends storing the DMD in a temperature and humidity controlled environment.
(4) Long-term is defined as the average over the usable life.
(5) Short-term is defined as less than the cumulative days over the usable life of the device.
(6) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES(1) (2)					
VCC	Supply voltage for LVCMOS core logic	3.15	3.3	3.45	V
VCCI	Supply voltage for LVDS receivers	3.15	3.3	3.45	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrodes(2)	8.25	8.5	8.75	V
VBIAS	Supply voltage for micromirror electrodes	15.5	16	16.5	V
VRESET	Supply voltage for micromirror electrodes	–9.5	–10	–10.5	V
|VCCI–VCC|	Supply voltage delta (absolute value) (3)			0.3	V
|VBIAS–VOFFSET|	Supply voltage delta (absolute value)(4)			8.75	V
LVCMOS PINS					
V_{IH}	High level Input voltage (5)	1.7	2.5	VCC + 0.15	V
V_{IL}	Low level Input voltage(5)	– 0.3		0.7	V
I_{OH}	High level output current at V_{OH} = 2.4 V			–20	mA
I_{OL}	Low level output current at V_{OL} = 0.4 V			15	mA
T_{PWRDNZ}	PWRDNZ pulse width(6)	10			ns
SCP INTERFACE					
f_{clock}	SCP clock frequency(7)			500	kHz
t_{SCP_SKEW}	Time between valid SCPDI and rising edge of SCPCLK(8)	–800		800	ns
t_{SCP_DELAY}	Time between valid SCPDO and rising edge of SCPCLK(8)			700	ns
$t_{SCP\_BYTE\_INTERVAL}$	Time between consecutive bytes	1			µs
$t_{SCP\_NEG\_ENZ}$	Time between falling edge of SCPENZ and the first rising edge of SCPCLK	30			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	1			µs
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state)			1.5	ns
f_{clock}	SCP circuit clock oscillator frequency (9)	9.6		11.1	MHz

(1) Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) VOFFSET supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(4) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. Refer to Power Supply Recommendations for additional information.
(5) Tester Conditions for V_{IH} and V_{IL}:
Frequency = 60MHz. Maximum Rise Time = 2.5 ns at (20% to 80%)
Frequency = 60MHz. Maximum Fall Time = 2.5 ns at (80% to 20%)
(6) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
(7) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(8) Refer to Figure 3.
(9) SCP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
LVDS INTERFACE					
f_{clock}	Clock frequency for LVDS interface, DCLK (all channels)			400	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value) (10)	100	400	600	mV
V_{CM}	Common mode (10)		1200		mV
V_{LVDS}	LVDS voltage (10)	0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL (11)					
T_{DMD}	DMD temperature–operational, long-term (12) (13) (14)	0		40 to 70 (13)	°C
	DMD temperature – operational, short-term	–20		75	°C
T_{WINDOW}	Window temperature – operational (15)			90	°C
$T_{CERAMIC\text{-}WINDOW\text{-}DELTA}$	Delta ceramic-to-window temperature -operational (15) (16)			30	°C
	Long-term dew point (operational, non-operational, long-term)			24	°C
	Short-term dew point (14) (17) (operational, non-operational, short-term)			28	°C
ILL_{UV}	Illumination, wavelength < 420 nm			0.68	mW/cm^2
ILL_{VIS}	Illumination, wavelengths between 420 and 700 nm			Thermally Limited (18)	mW/cm^2
ILL_{IR}	Illumination, wavelength > 700 nm			10	mW/cm^2

(10) Refer to Figure 4, Figure 5, and Figure 6.
(11) Optimal, long-term performance and optical efficiency of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(12) DMD Temperature is the worst-case of any thermal test point in Figure 10, or the active array as calculated by the Figure 15.
(13) Per Figure 1, the maximum operational case temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-on/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(14) Long-term is defined as the average over the usable life.
(15) Window temperature as measured at thermal test points TP2, TP3, TP4 and TP5 in Figure 15.The locations of thermal test points TP2, TP3, TP4 and TP5 in Figure 15 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, a test point should be added to that location.
(16) Ceramic package temperature as measured at test point 1 (TP 1) in Figure 10.
(17) Dew points beyond the specified long-term dew point (operating, non-operating, or storage) are for short-term conditions only, where short-term is defined as< 60 cumulative days over the usable life of the device .
(18) Refer to *Thermal Information* and *Micromirror Array Temperature Calculation* .

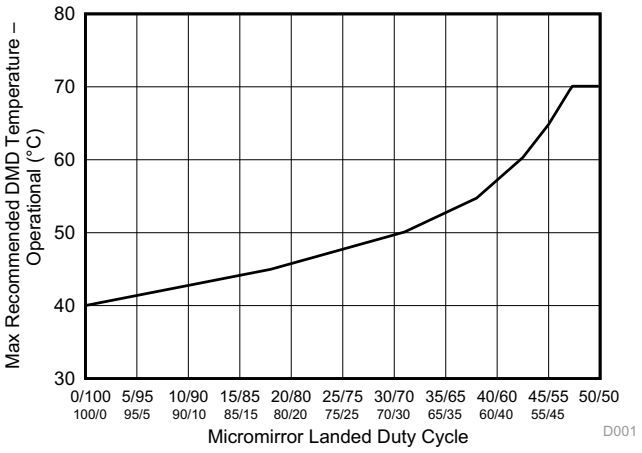


Figure 1. Max Recommended DMD Temperature – Derating Curve

6.4 Thermal Information

THERMAL METRIC(1)	MIN	DLP6500FYE FYE (350)	MAX	UNIT
Active Area-to-Case Ceramic Thermal resistance (1)			0.6	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions* . The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device. .

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	VCC = 3.3 V, I_{OH} = –20 mA	2.4			V
V_{OL}	Low level output voltage	VCC = 3.45 V, I_{OL} = 15 mA			0.4	V
I_{IH}	High–level input current(2) (3)	VCC = 3.45 V , V_I = VCC			250	µA
IIL	Low level input current	VCC = 3.45 V, V_I = 0	–250			µA
I_{OZ}	High–impedance output current	VCC = 3.45 V			10	µA
CURRENT						
I_{CC}	Supply current (4)	VCC = 3.6 V			1076	mA
I_{CCI}		VCCI = 3.6 V			518	
I_{OFFSET}	Supply current (5)	VOFFSET = 8.75 V			4	mA
I_{BIAS}		VBIAS = 16.5 V			14	
I_{RESET}	Supply current	VRESET = –10.5 V			11	mA
I_{TOTAL}		Total Sum			1623	
POWER						
P_{CC}	Supply power dissipation	VCC = 3.6 V			3874	mW
P_{CCI}		VCCI = 3.6 V			1865	
P_{OFFSET}		VOFFSET = 8.75 V			35	
P_{BIAS}		VBIAS = 16.5 V			231	
P_{RESET}		VRESET = –10.5 V			116	
P_{TOTAL}	Supply power dissipation(6)	Total Sum			6300	
CAPACITANCE						
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Output capacitance	f = 1 MHz			10	pF
C_M	Reset group capacitance MBRST(14:0)	f = 1 MHz 1920 × 72 micromirrors	330		390	pF

(1) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) Applies to LVCMOS input pins only. Does not apply to LVDS pins and MBRST pins.
(3) LVCMOS input pins utilize an internal 18000 Ω passive resistor for pull-up and pull-down configurations. Refer to *Pin Configuration and Functions* to determine pull-up or pull-down configuration used.
(4) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(6) Total power on the active micromirror array is the sum of the electrical power dissipation and the absorbed power from the illumination source. See the *Micromirror Array Temperature Calculation* .

6.6 Timing Requirements

Over *Recommended Operating Conditions* unless otherwise noted.

DESCRIPTION[1]				MIN	TYP	MAX	UNIT
SCP INTERFACE[2]							
t_r	Rise time	20% to 80%				200	ns
t_f	Fall time	80% to 20%				200	ns
LVDS INTERFACE[2]							
t_r	Rise time	20% to 80%		100		400	ps
t_f	Fall time	80% to 20%		100		400	ps
LVDS CLOCKS[3]							
t_c	Cycle time	DCLK_A, 50% to 50%		2.5			ns
		DCLK_B, 50% to 50%		2.5			
t_w	Pulse duration	DCLK_A, 50% to 50%		1.19	1.25		ns
		DCLK_B, 50% to 50%		1.19	1.25		
LVDS INTERFACE[3]							
t_{su}	Setup time	D_A(15:0) before rising or falling edge of DCLK_A		0.1			ns
		D_B(15:0) before rising or falling edge of DCLK_B		0.1			
t_{su}	Setup time	SCTRL_A before rising or falling edge of DCLK_A		0.1			ns
		SCTRL_B before rising or falling edge of DCLK_B		0.1			
t_h	Hold time	D_A(15:0) after rising or falling edge of DCLK_A		0.4			ns
		D_B(15:0) after rising or falling edge of DCLK_B		0.4			
t_h	Hold time	SCTRL_A after rising or falling edge of DCLK_A		0.3			ns
		SCTRL_B after rising or falling edge of DCLK_B		0.3			
LVDS INTERFACE[4]							
t_{skew}	Skew time	Channel B relative to Channel A [4]	Channel A includes the following LVDS pairs: DCLK_AP and DCLK_AN SCTRL_AP and SCTRL_AN D_AP(15:0) and D_AN(15:0)	–1.25		1.25	ns
			Channel B includes the following LVDS pairs: DCLK_BP and DCLK_BN SCTRL_BP and SCTRL_BN D_BP(15:0) and D_BN(15:0)				

(1) Refer to *Pin Configuration and Functions* for pin details.
(2) Refer to Figure 7
(3) Refer to Figure 8
(4) Refer to Figure 9

Timing Requirements

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 2 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Refer to the *Application and Implementation* section.

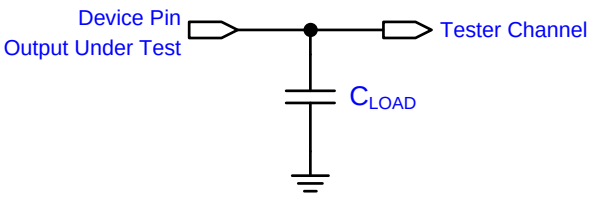
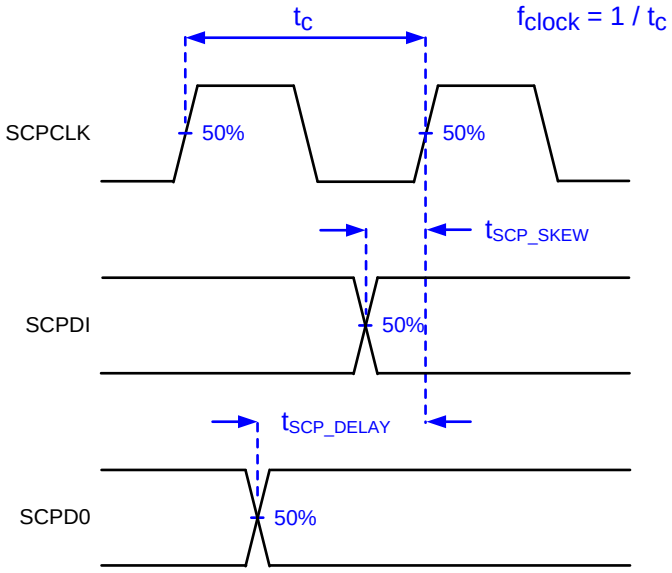


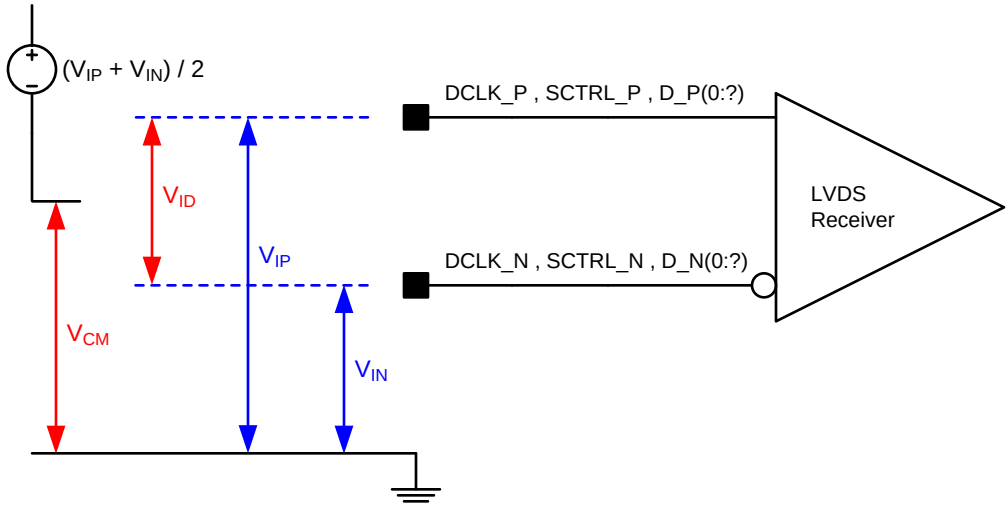
Figure 2. Test Load Circuit



Not to scale.

Refer to SCP Interface section of the Recommended Operating Conditions table.

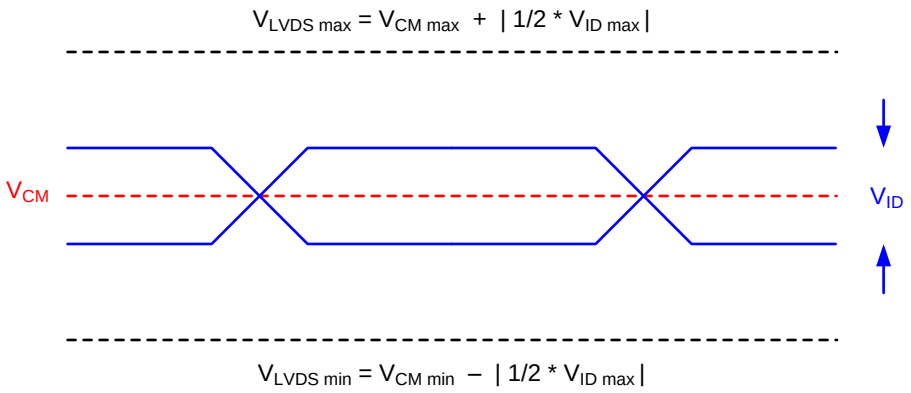
Figure 3. SCP Timing Parameters



Refer to LVDS Interface section of the Recommended Operating Conditions table.

Refer to Pin Configuration and Functions for list of LVDS pins.

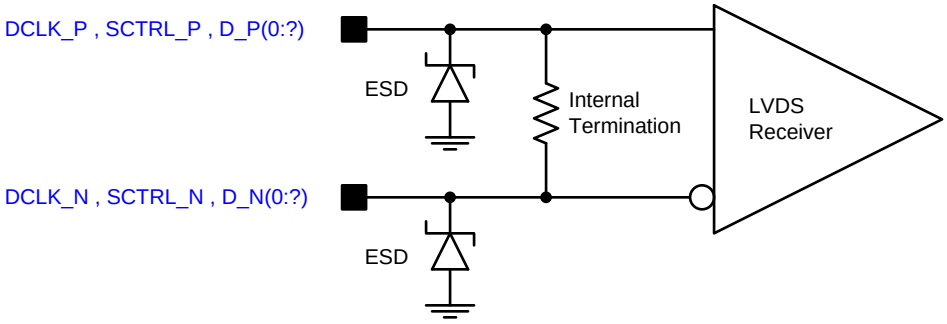
Figure 4. LVDS Voltage Definitions (References)



Not to scale.

Refer to LVDS Interface section of the Recommended Operating Conditions table.

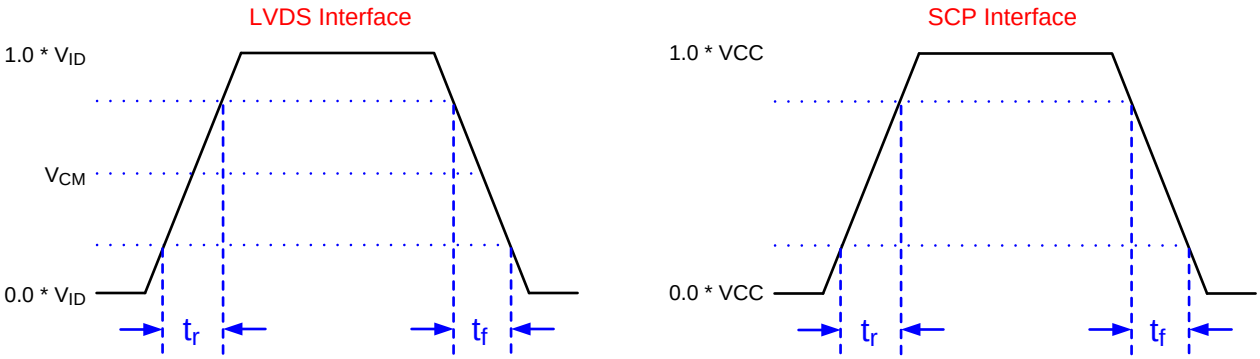
Figure 5. LVDS Voltage Parameters



Refer to LVDS Interface section of the Recommended Operating Conditions table.

Refer to Pin Configuration and Functions for list of LVDS pins.

Figure 6. LVDS Equivalent Input Circuit

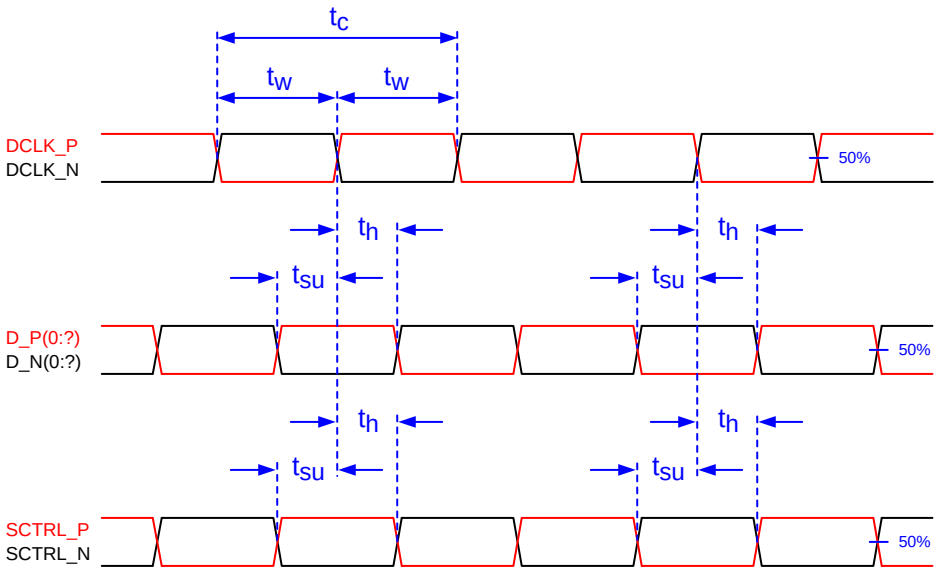


Not to scale.

Refer to the *Timing Requirements*

Refer to Pin Configuration and Functions for list of LVDS pins and SCP pins..

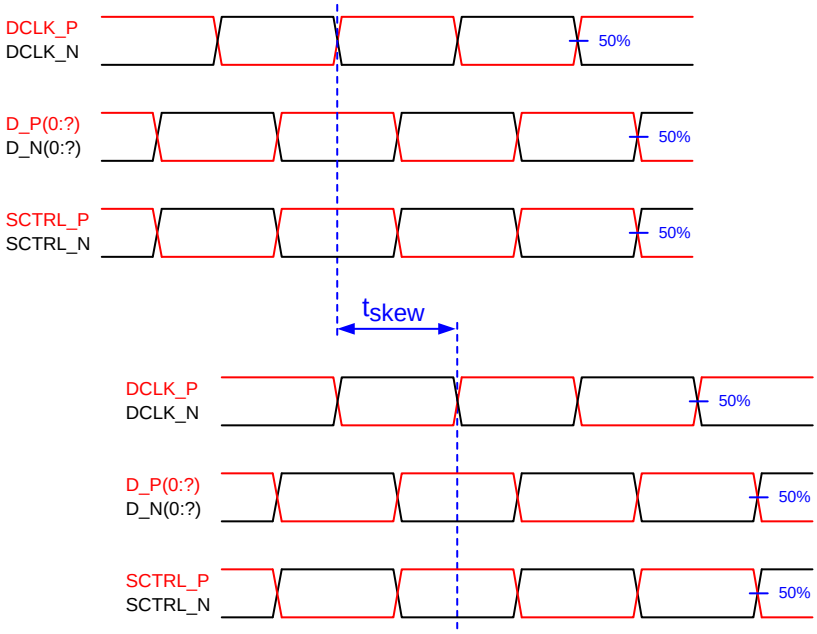
Figure 7. Rise Time and Fall Time



Not to scale.

Refer to LVDS INTERFACE section in the *Timing Requirements* table.

Figure 8. Timing Requirement Parameter Definitions



Not to scale.

Refer to LVDS INTERFACE section in the *Timing Requirements* table.

Figure 9. LVDS Interface Channel Skew Definition

6.7 Typical Characteristics

The DLP6500 DMD is controlled by the DLPC900 controller. The controller has two modes of operation. The first is Video mode where the video source is displayed on the DMD. The second is Pattern mode, where the patterns are pre-stored in flash memory and then streamed to the DMD. The allowed DMD pattern rate depends on which mode and bit-depth is selected.

Table 2. Bit Depth versus Pattern Rate

BIT DEPTH	VIDEO MODE RATE (Hz)	PATTERN MODE RATE (Hz)
1	2880	9523
2	1440	3289
3	960	2638
4	720	1364
5	480	823
6	480	672
7	360	500
8	247	247

6.8 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the: • Thermal Interface area • Electrical Interface areas	(See Figure 10)			11.30	Kg
Maximum Load 22.64 Applied per condition 2					Kg
• Thermal Interface area • Electrical Interface areas	(See Figure 10)			0 22.60	Kg

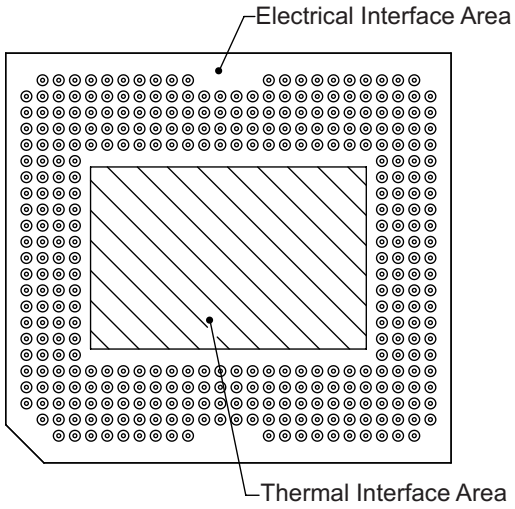
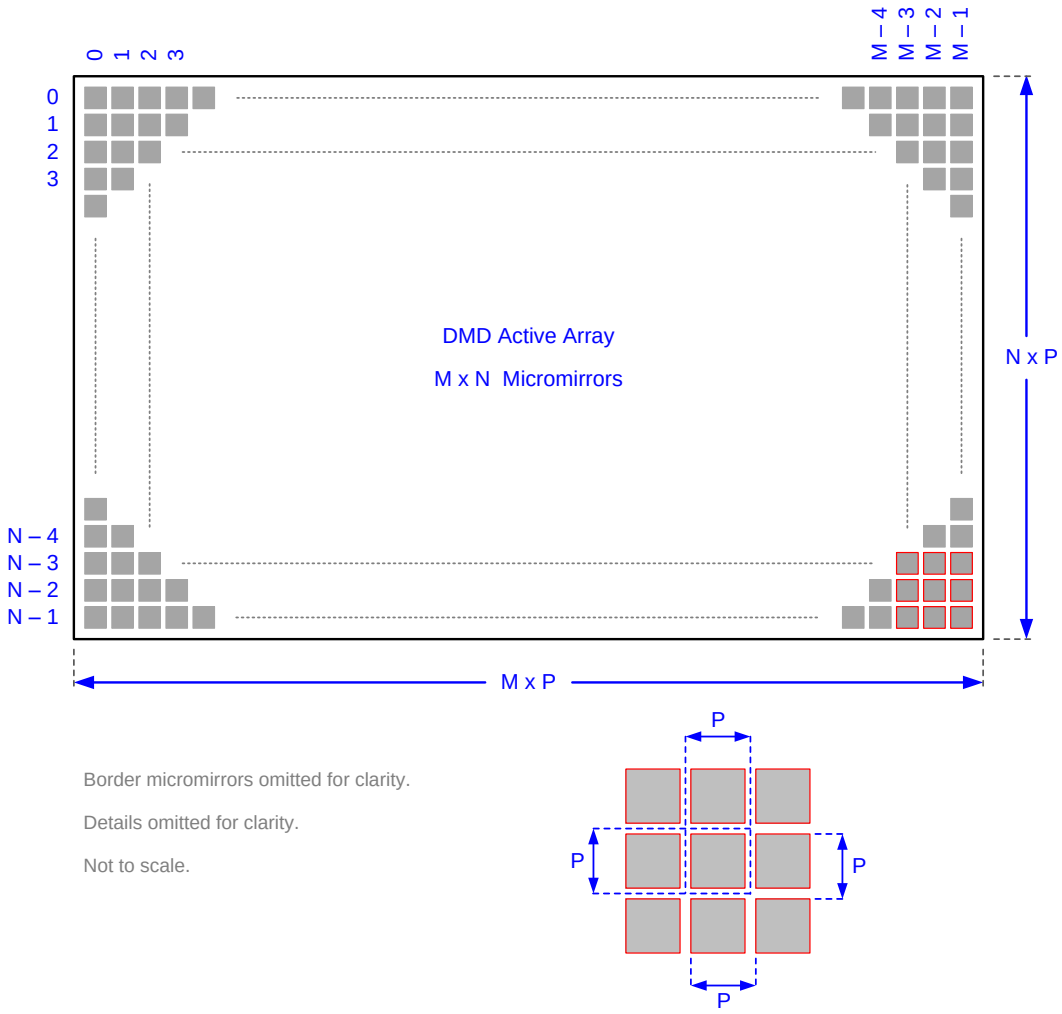


Figure 10. System Mounting Interface Loads

6.9 Micromirror Array Physical Characteristics

				VALUE	UNIT
M	Number of active columns		See Figure 11	1920	micromirrors
N	Number of active rows			1080	micromirrors
P	Micromirror (pixel) pitch			7.56	µm
	Micromirror active array width	M × P		14.5152	mm
	Micromirror active array height	N × P		8.1648	mm
	Micromirror active border	Pond of micromirror (POM)(1)		14	micromirrors /side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

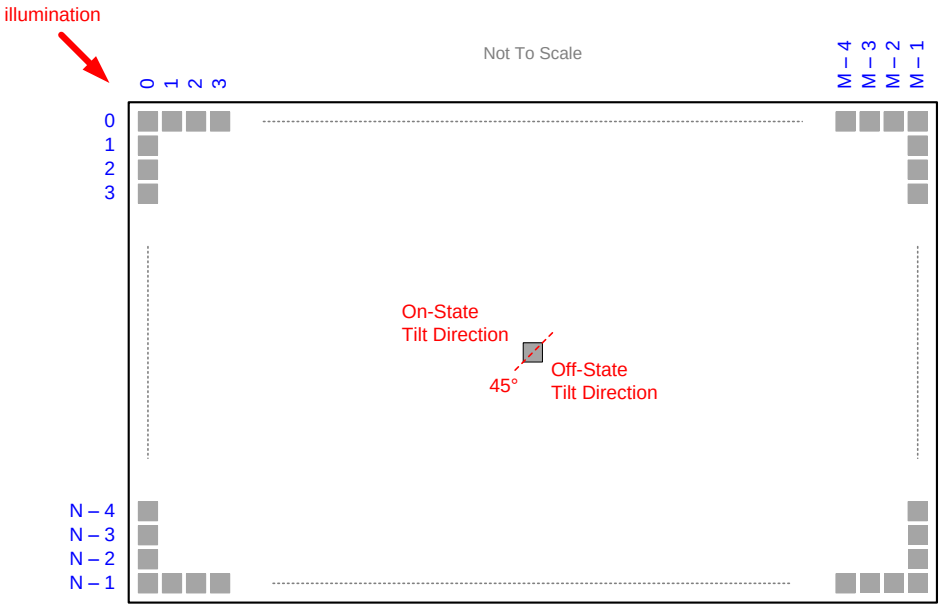
Figure 11. Micromirror Array Physical Characteristics

6.10 Micromirror Array Optical Characteristics

See *Optical Interface and System Image Quality* for important information

	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD landed state (1)		12		°
β	Micromirror tilt angle tolerance (1) (2) (3) (4) (5)		–1		1	°
	Micromirror tilt direction (5) (6) (7)		44	45	46	°
	Number of out-of-specification micromirrors (8)	Adjacent micromirrors			0	micromirrors
		Non-adjacent micromirrors			10	
	Micromirror crossover time (9) (10)	Typical performance		2.5		µs
	Micromirror switching time (10)	Typical performance		5		µs
	DMD photopic efficiency within the wavelength range 420 nm to 700 nm (11)			66%		

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(7) Refer to Figure 12
(8) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.
(9) Micromirror crossover time is primarily a function of the natural response time of the micromirrors.
(10) Performance as measured at the start of life.
(11) Efficiency numbers assume 24-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 12. Micromirror Landed Orientation and Tilt

6.11 Window Characteristics

PARAMETER (1)	CONDITIONS	MIN	TYP	MAX	UNIT
Window material designation S600	Corning 7056				
Window refractive index	at wavelength 589 nm		1.487		
Window aperture	See (2)				
Illumination overfill	Refer to *Illumination Overfill*				
Window transmittance, single–pass through both surfaces and glass (3)	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Window Characteristics and Optics* for more information.
(2) For details regarding the size and location of the window aperture, see the package mechanical characteristics listed in the Mechanical ICD in the Mechanical, Packaging, and Orderable Information section,
(3) See the TI application report DLPA031, *Wavelength Transmittance Considerations for DLP™ DMD Window*.

6.12 Chipset Component Usage Specification

The DLP6500FYE is a component of one or more DLP® chipsets. Reliable function and operation of the DLP6500FYE requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

7 Detailed Description

7.1 Overview

DLP6500FYE is a 0.65 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and square grid pixel arrangement are shown in Figure 11.

The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS), Double Data Rate (DDR).

DLP6500FYE DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of *M* memory cell columns by *N* memory cell rows. Refer to the *Functional Block Diagram* .

The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

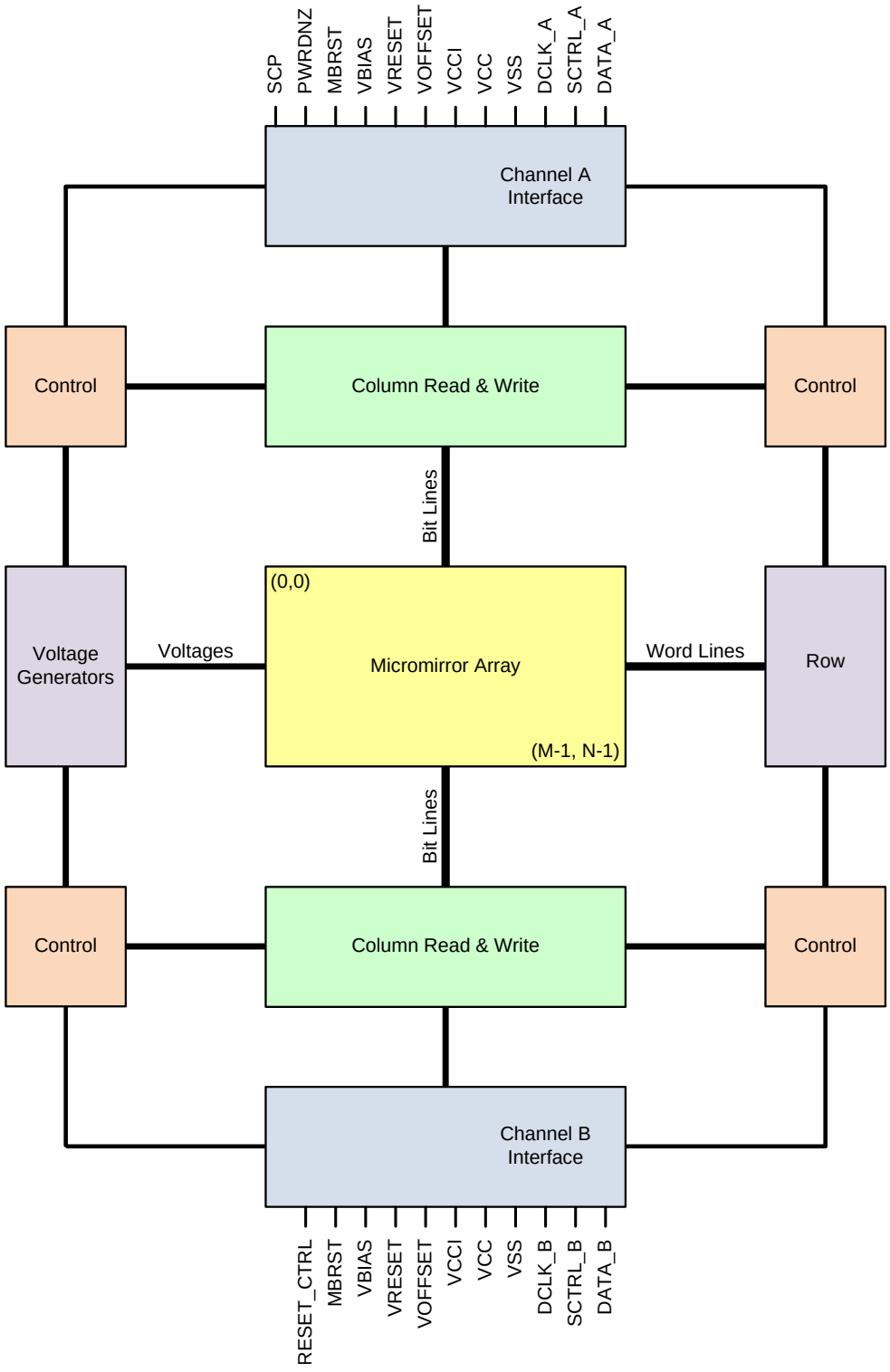
Each cell of the *M* × *N* memory array drives its true and complement ('Q' and 'QB') data to two electrodes underlying one micromirror, one electrode on each side of the diagonal axis of rotation. Refer to *Micromirror Array Optical Characteristics* . The micromirrors are electrically tied to the micromirror reset signals (MBRST) and the micromirror array is divided into reset groups.

Electrostatic potentials between a micromirror and its memory data electrodes cause the micromirror to tilt toward the illumination source in a DLP projection system or away from it, thus reflecting its incident light into or out of an optical collection aperture. The positive (+) tilt angle state corresponds to an 'on' pixel, and the negative (–) tilt angle state corresponds to an 'off' pixel.

Refer to *Micromirror Array Optical Characteristics* for the ± tilt angle specifications. Refer to *Pin Configuration and Functions* for more information on micromirror reset control.

7.2 Functional Block Diagram

Not to Scale. Details Omitted for Clarity. See Accompanying Notes in this Section.



For pin details on Channels A, B, C, and D, refer to *Pin Configuration and Functions* and LVDS Interface section of *Timing Requirements* .

7.3 Feature Description

DLP6500FYE device consists of highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional orthogonal pixel array. Refer to Figure 11 and Figure 13.

Each aluminum micromirror is switchable between two discrete angular positions, –α and +α. The angular positions are measured relative to the micromirror array plane, which is parallel to the silicon substrate. Refer to *Micromirror Array Optical Characteristics* and Figure 14.

The parked position of the micromirror is not a latched position and is therefore not necessarily perfectly parallel to the array plane. Individual micromirror flat state angular positions may vary. Tilt direction of the micromirror is perpendicular to the hinge-axis. The on-state landed position is directed toward the left-top edge of the package, as shown in Figure 13.

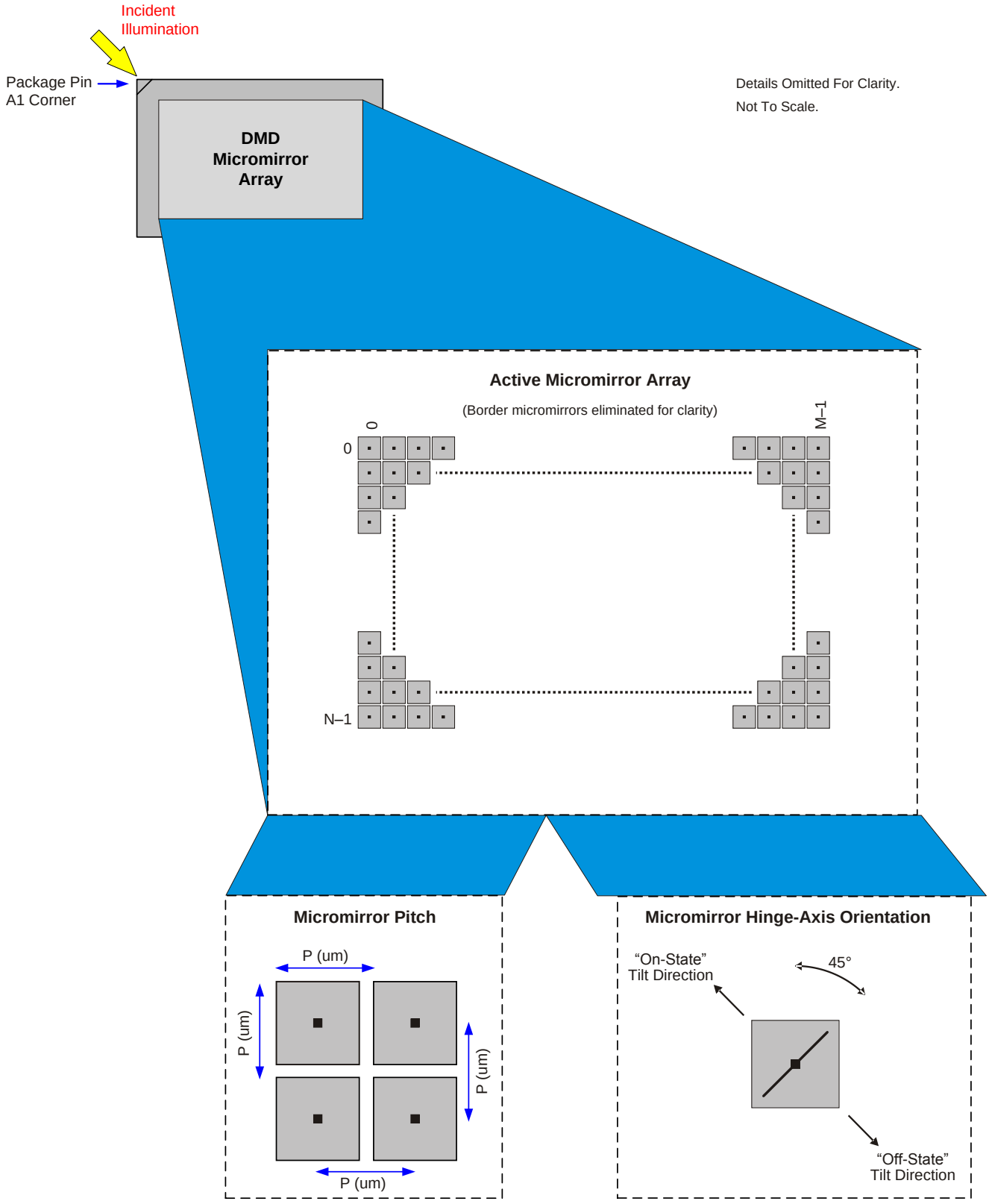
Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror *clocking pulse* is applied. The angular position (–α and +α) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update.

Writing logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a +α position. Writing logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a – α position.

Updating the angular position of the micromirror array consists of two steps. First, update the contents of the CMOS memory. Second, apply a micromirror reset to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror reset pulses are generated internally by the DLP6500FYE DMD , with application of the pulses being coordinated by the DLPC900 display controller.

For more information, see the TI application report DLPA008A, *DMD101: Introduction to Digital Micromirror Device (DMD) Technology*.

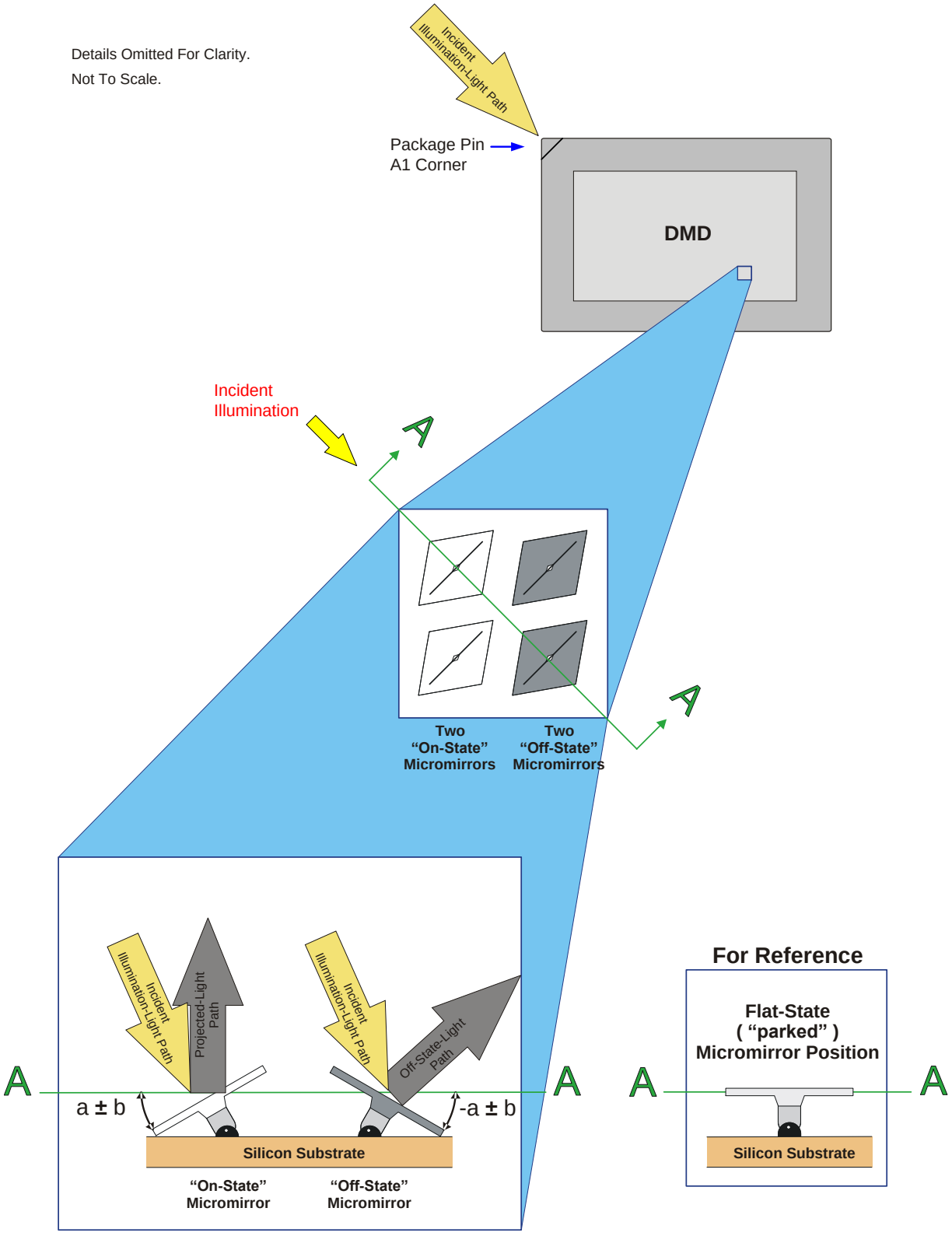
Feature Description (continued)



Refer to Micromirror Array Physical Characteristics, Figure 11, and Micromirror Landed Orientation and Tilt

Figure 13. Micromirror Array, Pitch, Hinge Axis Orientation

Feature Description (continued)



Micromirror States: On, Off, Flat

Figure 14. Micromirror States: On, Off, Flat

7.4 Device Functional Modes

DLP6500FYE is part of the chipset comprising of the DLP6500FYE DMD and DLPC900 display controller. To ensure reliable operation, DLP6500FYE DMD must always be used with a DLPC900 display controller.

DMD functional modes are controlled by the DLPC900 digital display controller. See the DLPC900 data sheet listed in Related Documents. Contact a TI applications engineer for more information.

7.5 Window Characteristics and Optics

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.2 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

7.5.3 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

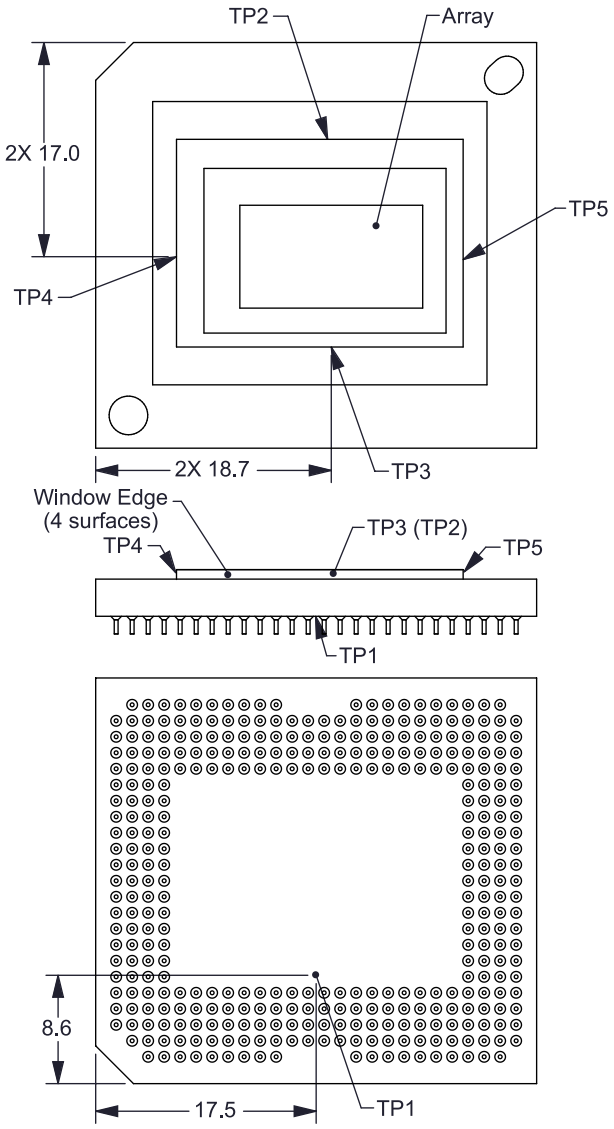


Figure 15. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL)$$

where

- T_{ARRAY} = Computed micromirror array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in Figure 15
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from micromirror array to outside ceramic (°C/W) specified in *Thermal Information*
- Q_{ARRAY} = Total DMD power; electrical, specified in *Electrical Characteristics* , plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W), specified in *Electrical Characteristics*

Micromirror Array Temperature Calculation (continued)

- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm) (3)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The nominal electrical power dissipation to use when calculating array temperature is 2.9 Watts . Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00293 W/lm.

Sample Calculation for typical projection application:

$T_{CERAMIC}$ = 55°C, assumed system measurement; see *Recommended Operating Conditions* for specific limits
SL = 2000 lm
$Q_{ELECTRICAL}$ = 2.9 W (see the maximum power specifications in *Electrical Characteristics*)
C_{L2W} = 0.00293 W/lm
Q_{ARRAY} = 2.9 W + (0.00293 W/lm × 2000 lm) = 8.76 W
T_{ARRAY} = 55°C + (8.76 W × 0.6 × C/W) = 60.26°C

7.7 Micromirror Landed-on/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On–state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On–state 100% of the time (and in the Off–state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off–state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

Micromirror Landed-on/Landed-Off Duty Cycle (continued)

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a give long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 3.

Table 3. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

Where:

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 4.

Table 4. Example Landed Duty Cycle for Full-Color

Red Cycle Percentage 50%	Green Cycle Percentage 20%	Blue Cycle Percentage 30%	Landed Duty Cycle
Red Scale Value	Green Scale Value	Blue Scale Value	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLP6500FYE along with the DLPC900 controller provides a solution for many applications including structured light and video projection. The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC900. Applications of interest include machine vision and 3D printing.

8.2 Typical Application

A typical embedded system application using the DLPC900 controller and a DLP6500FYE is shown in Figure 16. In this configuration, the DLPC900 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. This system configuration supports still and motion video sources plus sequential pattern mode. Refer to Related Documents for the DLPC900 digital controller data sheet.

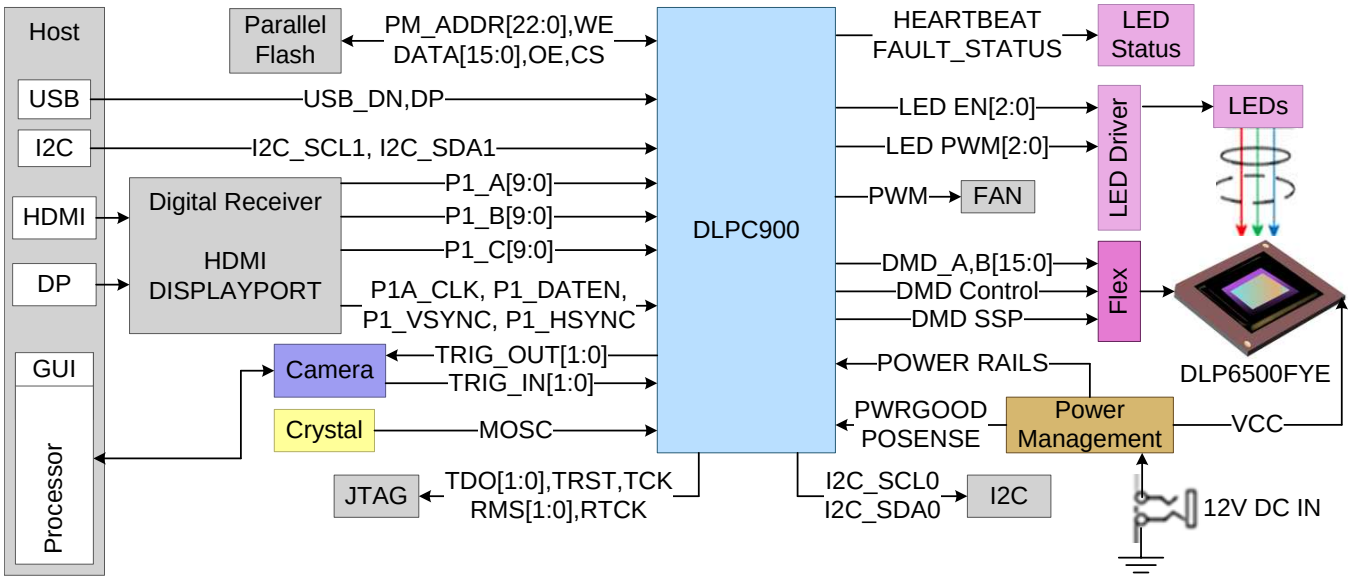


Figure 16. Typical Application Schematic

8.2.1 Design Requirements

Detailed design requirements are located in the DLPC900 digital controller data sheet. Refer to Related Documents.

8.2.2 Detailed Design Procedure

See the reference design schematic for connecting together the DLPC900 display controller and the DLP6500 DMD. An example board layout is included in the reference design data base. Layout guidelines should be followed for reliability.

9 Power Supply Recommendations

9.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC900 device.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VCC, VCCI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. VSS must also be connected. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 17.

9.2 DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions* s. During power-up, VBIAS does not have to start after VOFFSET.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings* , in *Recommended Operating Conditions* , and in *DMD Power Supply Sequencing Requirements* .
- During power-up, LVCMOS input pins shall not be driven high until after VCC and VCCI have settled at operating voltages listed in *Recommended Operating Conditions* .

9.3 DMD Power Supply Power-Down Procedure

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. Refer to Table 5.
- During power-down, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions* . During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings* , in *Recommended Operating Conditions* , and in Figure 17.
- During power-down, LVCMOS input pins must be less than specified in *Recommended Operating Conditions* .

DMD Power Supply Power-Down Procedure (continued)

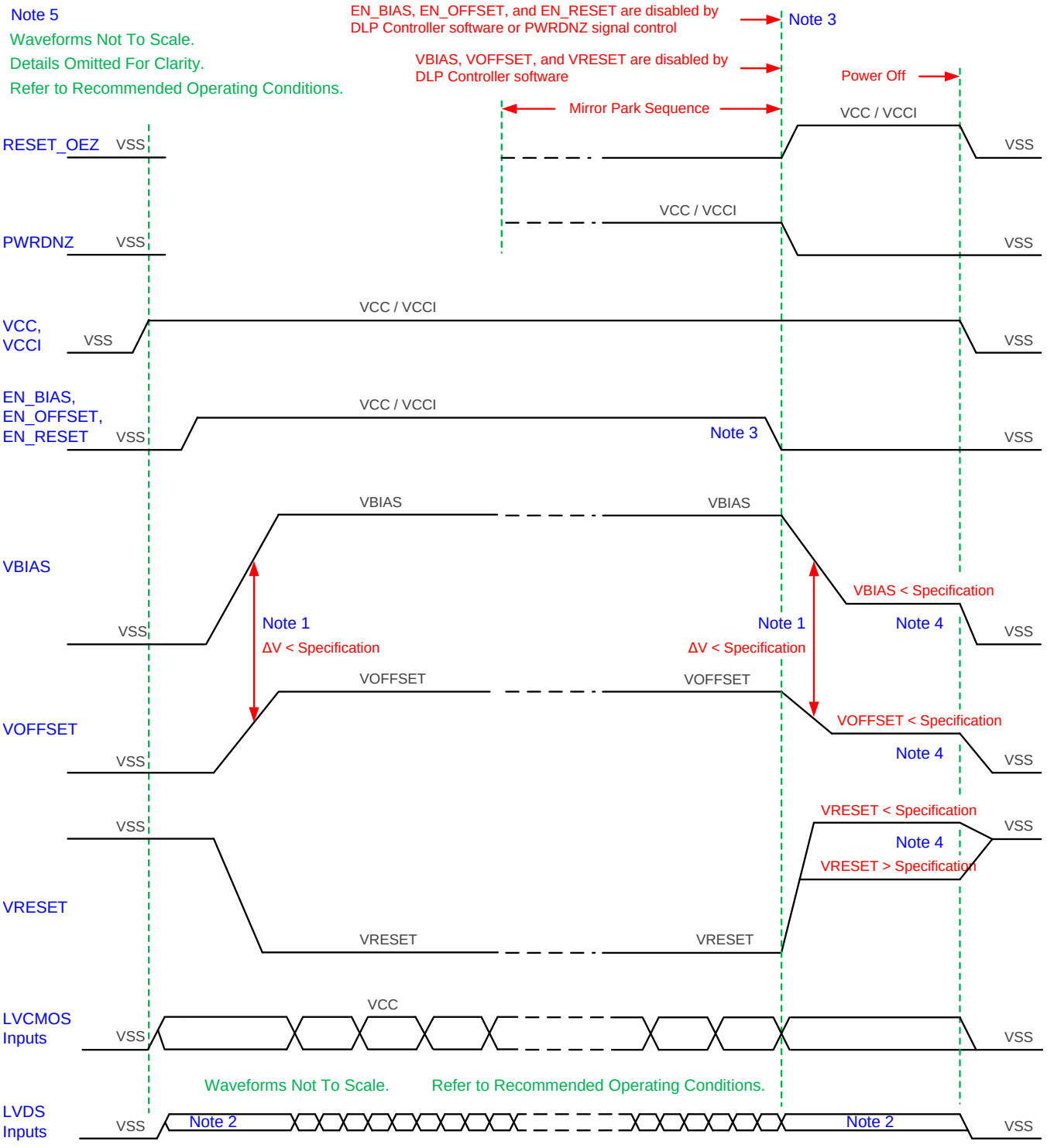


Figure 17. DMD Power Supply Sequencing Requirements

1. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in *Recommended Operating Conditions* . OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down.
2. LVDS signals are less than the input differential voltage (VID) maximum specified in *Recommended*

DMD Power Supply Power-Down Procedure (continued)

Operating Conditions . During power-down, LVDS signals are less than the high level input voltage (VIH) maximum specified in *Recommended Operating Conditions* .

3. When system power is interrupted, the DLP controller (DLPC900) initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET after the micromirror park sequence. Software power-down disables VBIAS, VRESET, and VOFFSET after the micromirror park sequence through software control. For either case, enable signals EN_BIAS, EN_OFFSET, and EN_RESET are used to disable VBIAS, VOFFSET, and VRESET, respectfully.
4. Refer to Table 5.
5. Figure not to scale. Details have been omitted for clarity. Refer to *Recommended Operating Conditions* .

Table 5. DMD Power-Down Sequence Requirements

PARAMETER		MIN	MAX	UNIT
VBIAS	Supply voltage level during power–down sequence		4.0	V
VOFFSET			4.0	V
VRESET		–4.0	0.5	V

10 Layout

10.1 Layout Guidelines

The DLP6500FYE along with one DLPC900 controller provides a solution for many applications including structured light and video projection. This section provides layout guidelines for the DLP6500FYE.

10.1.1 General PCB Recommendations

The PCB shall be designed to IPC2221 and IPC2222, Class 2, Type Z, at level B producibility and built to IPC6011 and IPC6012, class 2. The PCB board thickness to be 0.062 inches +/- 10%, using standard FR-4 material, and applies after all lamination and plating processes, measured from copper to copper.

Two-ounce copper planes are recommended in the PCB design in order to achieve needed thermal connectivity. Refer to Related Documents for the DLPC900 Digital Controller Data Sheet for related information on the DMD Interface Considerations.

High-speed interface waveform quality and timing on the DLPC900 controller (that is, the LVDS DMD interface) is dependent on the following factors:

- Total length of the interconnect system
- Spacing between traces
- Characteristic impedance
- Etch losses
- How well matched the lengths are across the interface

Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

- Setup Margin = (controller output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)
- Hold-time Margin = (controller output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

The PCB SI degradation is the signal integrity degradation due to PCB affects which includes such things as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol-interference (ISI) noise.

DLPC900 I/O timing parameters can be found in DLPC900 Digital Controller Data Sheet. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not as easy to determine.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines provide a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Deviation from these recommendations may work, but should be confirmed with PCB signal integrity analysis or lab measurements.

10.2 Layout Example

10.2.1 Board Stack and Impedance Requirements

Refer to Figure 18 for guidance on the parameters.

PCB design:

Configuration:	Asymmetric dual stripline
Etch thickness (T):	1.0-oz copper (1.2 mil)
Flex etch thickness (T):	0.5-oz copper (0.6 mil)
Single-ended signal impedance:	50 Ω (±10%)
Differential signal impedance:	100 Ω (±10%)

Layout Example (continued)

PCB stack-up:

Reference plane 1 is assumed to be a ground plane for proper return path.

Reference plane 2 is assumed to be the I/O power plane or ground.

Dielectric FR4, (Er):	4.2 (nominal)
Signal trace distance to reference plane 1 (H1):	5.0 mil (nominal)
Signal trace distance to reference plane 2 (H2):	34.2 mil (nominal)

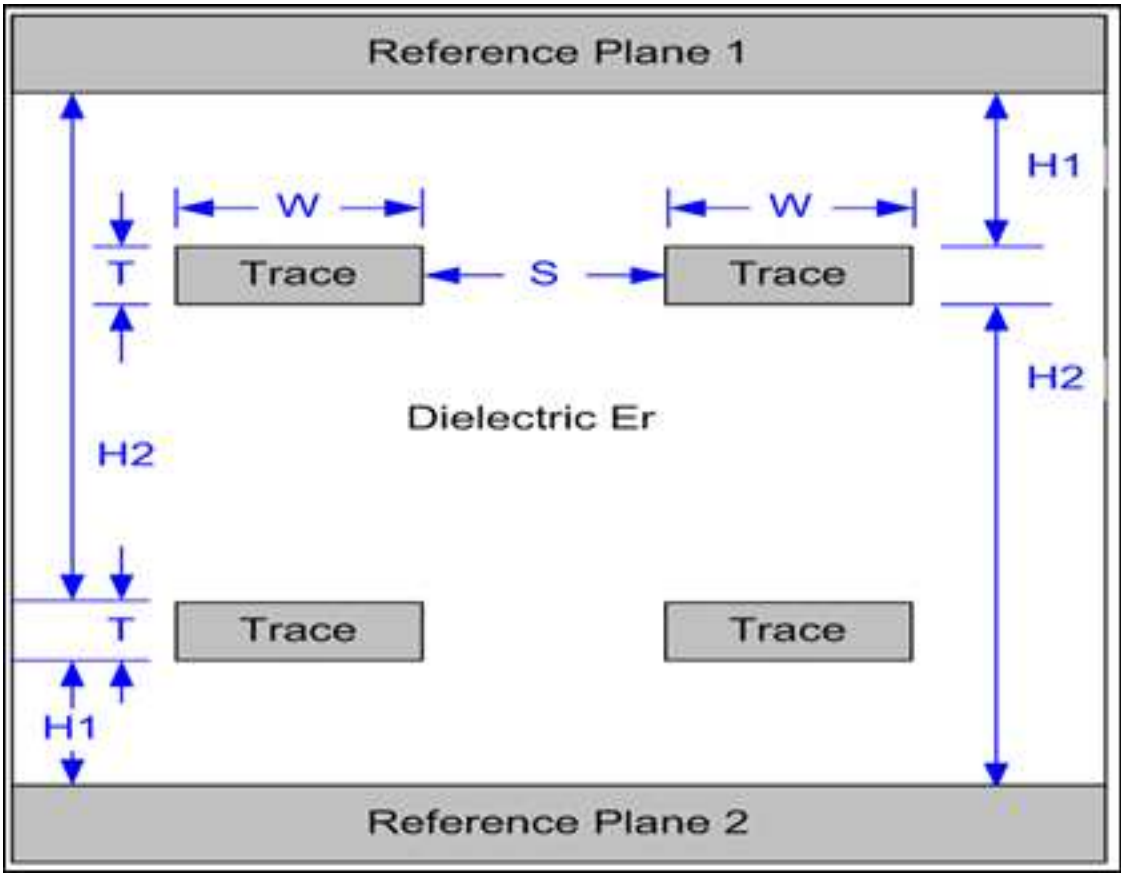


Figure 18. PCB Stack Geometries

Table 6. General PCB Routing (Applies to All Corresponding PCB Signals)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Line width (W)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB etch clocks	7 (0.18)	4.25 (0.11)	mil (mm)

Layout Example (continued)

Table 6. General PCB Routing (Applies to All Corresponding PCB Signals) (continued)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Differential signal pair spacing (S)	PCB etch data or control	N/A	5.75(1) –0.15	mil (mm)
	PCB etch clocks	N/A	5.75(1) –0.15	mil (mm)
Minimum differential pair-to-pair spacing (S)	PCB etch data or control	N/A	20 (0.51)	mil (mm)
	PCB etch clocks	N/A	20 (0.51)	mil (mm)
	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
Minimum line spacing to other signals (S)	PCB etch data or control	10 (0.25)	20 (0.51)	mil (mm)
	PCB etch clocks	20 (0.51)	20 (0.51)	mil (mm)
Maximum differential pair P-to-N length mismatch	Total data	N/A	12 0.3	mil (mm)
	Total data	N/A	12 0.3	mil (mm)

(1) Spacing may vary to maintain differential impedance requirements

Table 7. DMD Interface Specific Routing

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD (LVDS)	SCTRL_AN / SCTRL_AP D_AP(15:0)/ D_AN(15:0)	DCKA_P/ DCKA_N	± 150 (± 3.81)	mil (mm)
DMD (LVDS)	SCTRL_BN/ SCTRL_BP D_BP(15:0)/ D_BN(15:0)	DCKB_P/ DCKB_N	± 150 (± 3.81)	mil (mm)

Number of layer changes:

- Single-ended signals: Minimize
- Differential signals: Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

Table 8. DMD Signal Routing Length(1)

BUS	MIN	MAX	UNIT
DMD (LVDS)	50	375	mm

(1) Max signal routing length includes escape routing.

Stubs: Stubs should be avoided.

Termination Requirements: DMD interface: None – The DMD receiver is differentially terminated to 100 Ω internally.

Connector (DMD-LVDS interface bus only):

High-speed connectors that meet the following requirements should be used:

- Differential crosstalk:< 5%
- Differential impedance: 75 to 125 Ω

Routing requirements for right-angle connectors: When using right-angle connectors, P-N pairs should be routed in the same row to minimize delay mismatch. When using right-angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths. Voltage or low frequency signals should be routed on the outer layers. Signal trace corners shall be no sharper than 45 degrees. Adjacent signal layers shall have the predominant traces routed orthogonal to each other.

These guidelines will produce a maximum PCB routing mismatch of 4.41 mm (0.174 inch) or approximately 30.4 ps, assuming 175 ps/inch FR4 propagation delay.

These PCB routing guidelines will result in approximately 25-ps system setup margin and 25-ps system hold margin for the DMD interface after accounting for signal integrity degradation as well as routing mismatch.

Both the DLPC900 output timing parameters and the DLP6500FYE DMD input timing parameters include timing budget to account for their respective internal package routing skew.

10.2.1.1 Power Planes

Signal routing is NOT allowed on the power and ground planes. All device pin and via connections to this plane shall use a thermal relief with a minimum of four spokes. The power plane shall clear the edge of the PCB by 0.2”.

Prior to routing, vias connecting all digital ground layers (GND) should be placed around the edge of the rigid PWB regions 0.025” from the board edges with a 0.100” spacing. It is also desirable to have all internal digital ground (GND) planes connected together in as many places as possible. If possible, all internal ground planes should be connected together with a minimum distance between connections of 0.5”. Extra vias are not required if there are sufficient ground vias due to normal ground connections of devices. NOTE: All signal routing and signal vias should be inside the perimeter ring of ground vias.

Power and Ground pins of each component shall be connected to the power and ground planes with one via for each pin. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100”). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. Ground plane slots are NOT allowed.

Route VOFFSET, VBIAS, and VRESET as a wide trace >20mils (wider if space allows) with 20 mils spacing.

10.2.1.2 LVDS Signals

The LVDS signals shall be first. Each pair of differential signals must be routed together at a constant separation such that constant differential impedance (as in section *Board Stack and Impedance Requirements*) is maintained throughout the length. Avoid sharp turns and layer switching while keeping lengths to a minimum. The distance from one pair of differential signals to another shall be at least 2 times the distance within the pair.

10.2.1.3 Critical Signals

The critical signals on the board must be hand routed in the order specified below. In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long trace all around the PCB.

Table 9. Timing Critical Signals

GROUP	SIGNAL	CONSTRAINTS	ROUTING LAYERS
1	D_AP(0:15), D_AN(0:15), DCLK_AP, DCLK_AN, SCTRL_AN, SCTRL_AP, D_BP(0:15), D_BN (0:15), DCLK_BP, DCLK_BN, SCTRL_BN, SCTRL_BP	Refer to Table 6 and Table 7	Internal signal layers. Avoid layer switching when routing these signals.
2	RESET_ADDR_(0:3), RESET_MODE_(0:1), RESET_OEZ, RESET_SEL_(0:1) RESET_STROBE, RESET_IRQZ.		Internal signal layers. Top and bottom as required.
3	SCP_CLK, SCP_DO, SCP_DI, SCP_DMD_CSZ.		Any
4	Others	No matching/length requirement	Any

10.2.1.4 Device Placement

Unless otherwise specified, all major components should be placed on top layer. Small components such as ceramic, non-polarized capacitors, resistors and resistor networks can be placed on bottom layer. All high frequency de-coupling capacitors for the ICs shall be placed near the parts. Distribute the capacitors evenly around the IC and locate them as close to the device's power pins as possible (preferably with no vias). In the case where an IC has multiple de-coupling capacitors with different values, alternate the values of those that are side by side as much as possible and place the smaller value capacitor closer to the device.

10.2.1.5 Device Orientation

It is desirable to have all polarized capacitors oriented with their positive terminals in the same direction. If polarized capacitors are oriented both horizontally and vertically, then all horizontal capacitors should be oriented with the "+" terminal the same direction and likewise for the vertically oriented ones.

10.2.1.6 Fiducials

Fiducials for automatic component insertion should be placed on the board according to the following guidelines or on recommendation from manufacturer:

- Fiducials for optical auto insertion alignment shall be placed on three corners of both sides of the PWB.
- Fiducials shall also be placed in the center of the land patterns for fine pitch components (lead spacing <0.05").
- Fiducials should be 0.050 inch copper with 0.100 inch cutout (antipad).

11 器件文档支持

11.1 器件支持

11.1.1 器件命名规则

表 **10.** 封装具体信息

封装类型	引脚	连接器
FYE	350	PGA

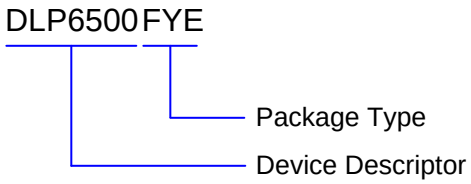


图 **19.** 部件号说明

11.1.2 器件标记

器件标记将包括可读信息和一个二维矩阵码。 图 20 中显示了可读信息。 二维矩阵码是一个字母数字字符串，其中包含 DMD 部件号、序列号的第 1 部分和序列号的第 2 部分。 DMD 序列号（第 1 部分）的首字符为制造年份。 DMD 序列号（第 1 部分）的第二个字符为制造月份。 DMD 序列号（第 2 部分）的最后一个字符为偏置电压二进制字母。

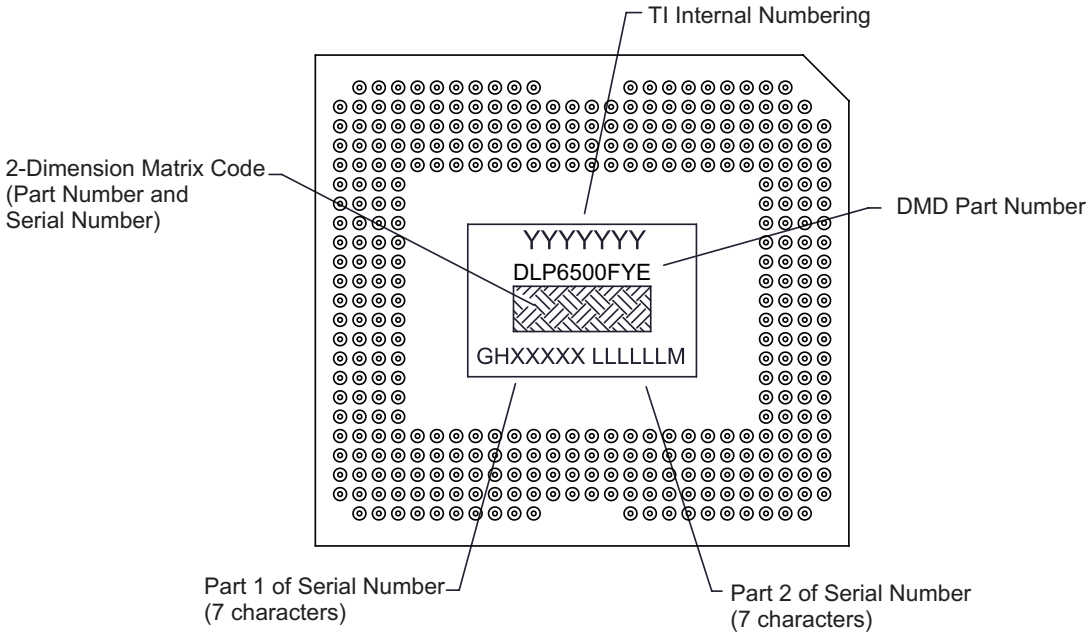


图 **20. DMD** 标记

11.2 文档支持

11.2.1 相关文档

以下文档包含关于使用 DLP6500 器件的更多信息。

表 **11.** 相关文档

文档	
DLPC900 数字控制器数据表	DLPS037
DLPC900 软件编程人员指南	DLPU018

11.3 商标

DLP is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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	产品		应用
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放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP6500FYE	ACTIVE	CPGA	FYE	350	1	Green (RoHS & no Sb/Br)	PD NIPDAU	Level-1-NC-NC			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

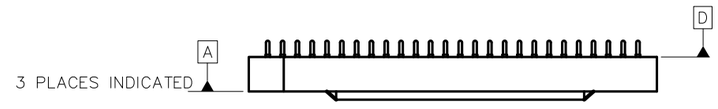
DWG NO 2511543 SH 1

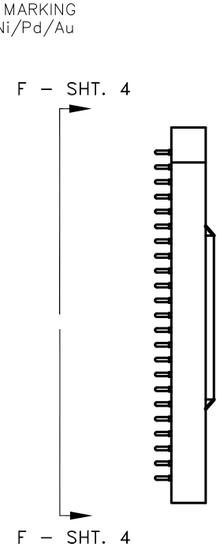
REVISIONS

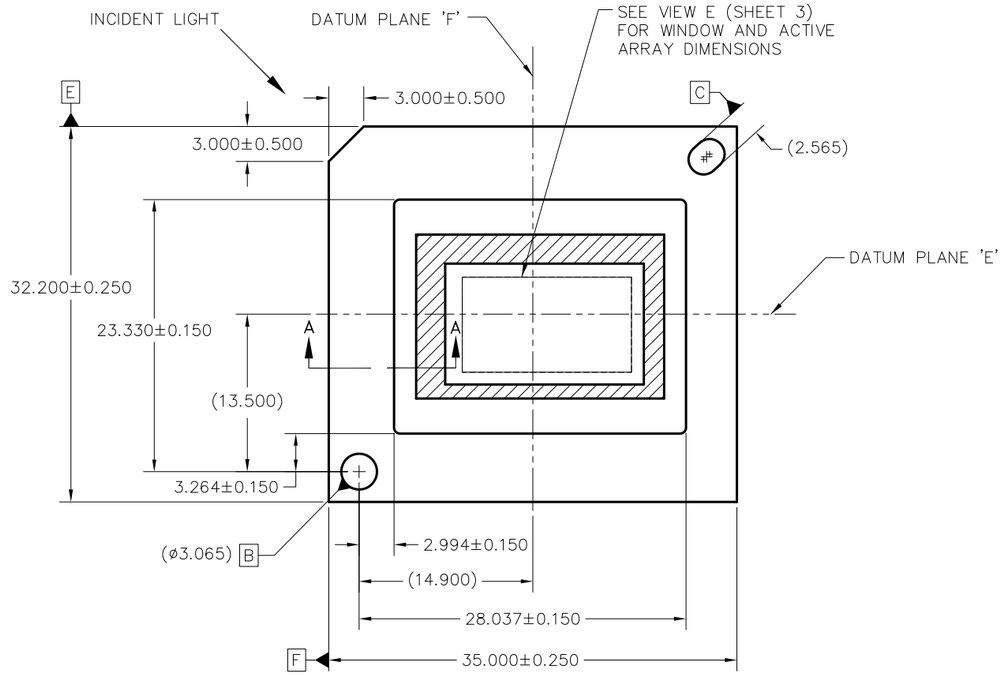
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2111739, INITIAL RELEASE	11/04/2010	F. ARMSTRONG
B	ECO 2112602, CHANGE TOLERANCES ON OUTSIDE DIMENSIONS TO ±0.250; CHANGE DATUM B, BACK SIDE PINS, AND DATUM PLANES 'E' AND 'F' TO REFERENCE CENTERLINE OF PART	12/10/2010	F. ARMSTRONG
C	ECO 2135107, ADD NOTE 8 TO SHEETS 1 & 4	08/02/2013	F. ARMSTRONG
D	ECO 2139887, CHG GLASS SIZE UPPER TOL TO +0.050 TO MATCH PROCESS CAPABILITY	02/14/2014	F. ARMSTRONG

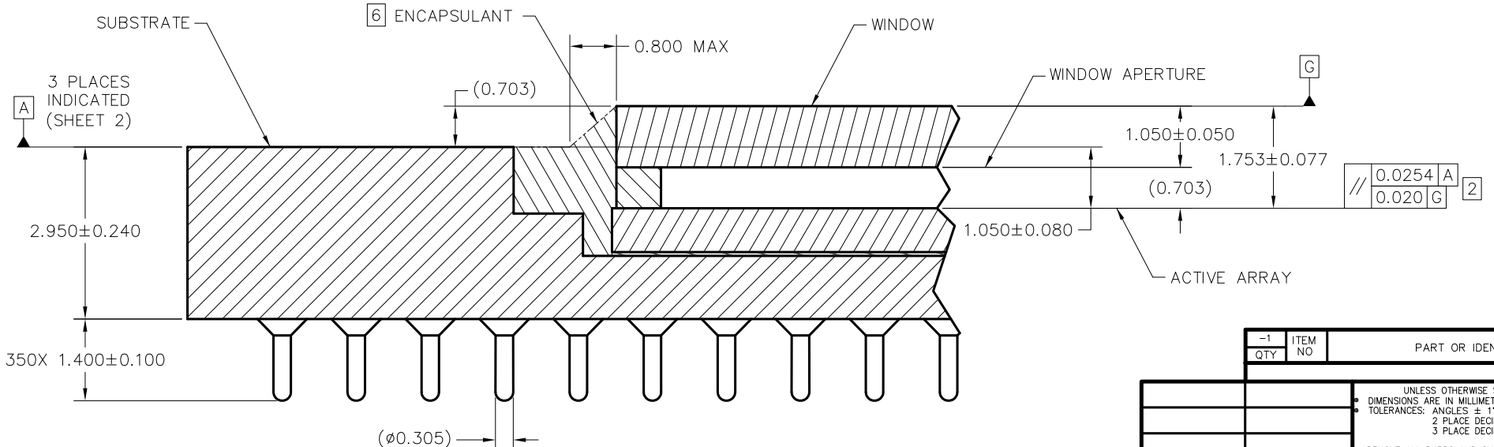
NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES ARE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.









SECTION A–A
SCALE 20/1

QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
–1		PARTS LIST		

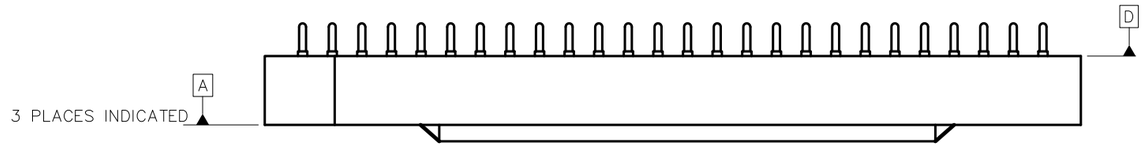
UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5–1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

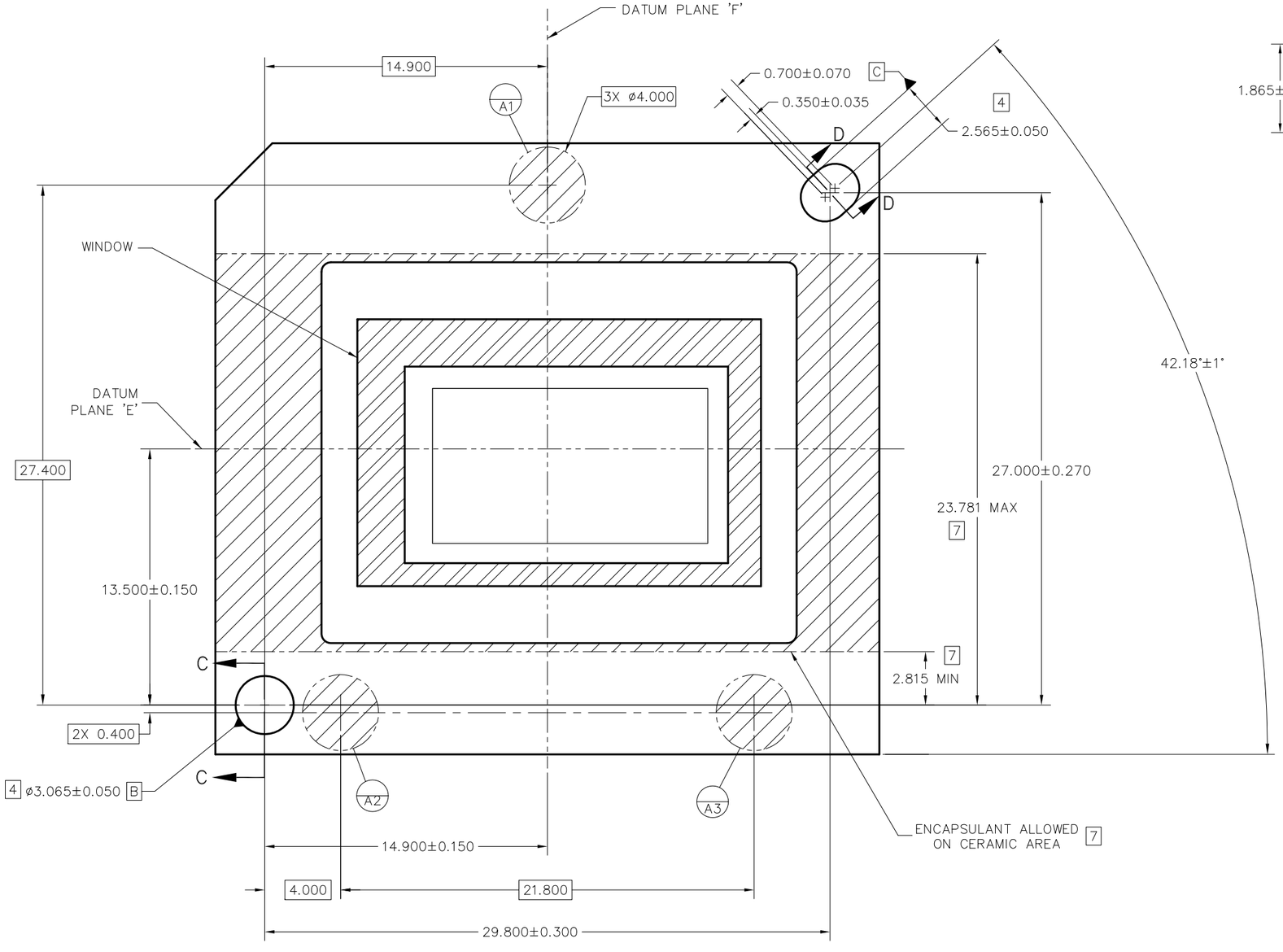
THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

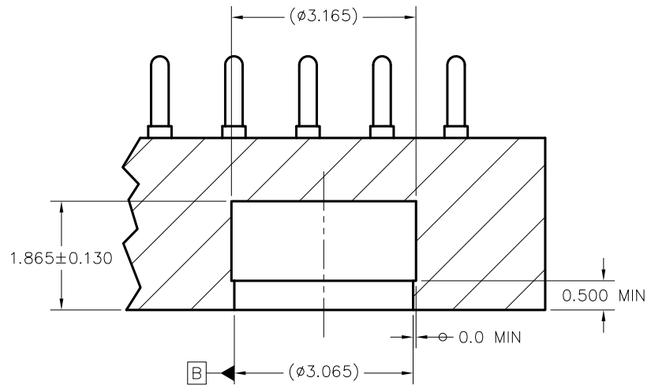
DWN F. ARMSTRONG	DATE 11/02/2010	TEXAS INSTRUMENTS Dallas, Texas
ENGR F. ARMSTRONG	11/02/2010	ICD, MECHANICAL, DMD .65 1080p MVSP 2XLVDS SERIES 600
QA F. KONRAD	11/08/2010	
CQE M. DORAK	11/08/2010	SIZE B · DRAWING NO 2511543 · REV D
		SCALE 4/1 · SHEET 1 OF 4

ACED1g

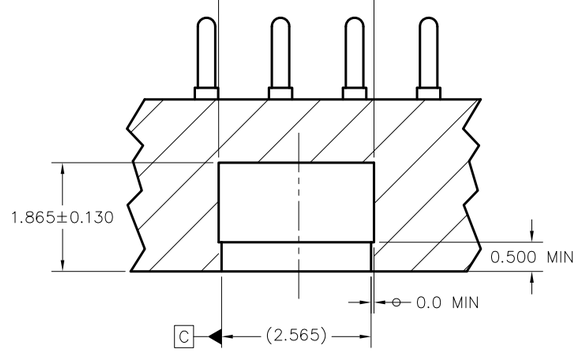




VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



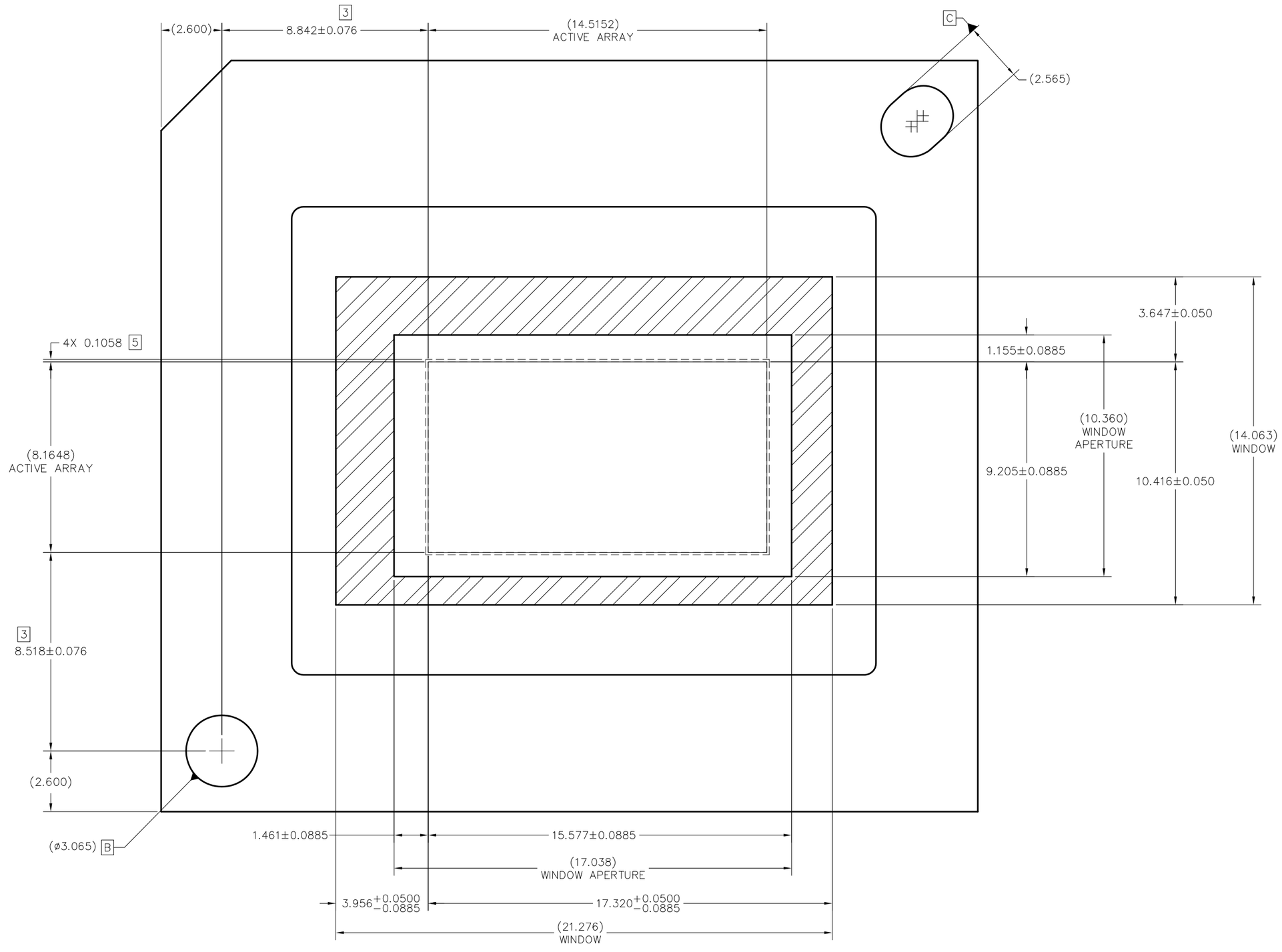
SECTION C–C
DATUM B
SCALE 16/1



SECTION D–D
DATUM C
SCALE 16/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE B	DRAWING NO 2511543	REV D
		SCALE 4/1	SHEET 2	

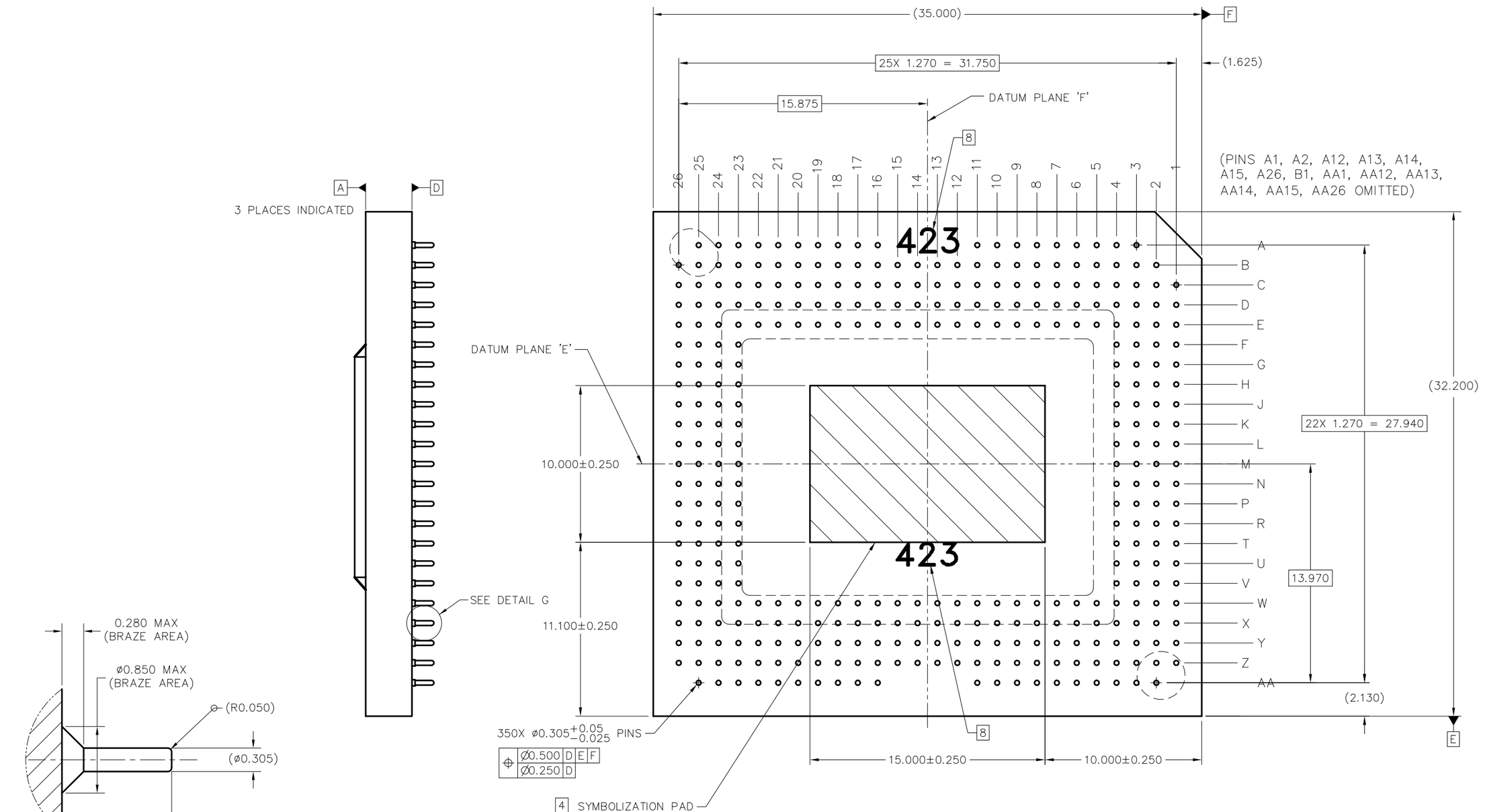
ACED2c



VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

Texas Instruments, Dallas, Texas	DWN	DATE	SIZE B	DRAWING NO 2511543	REV D
	ISSUE DATE		SCALE 4/1	SHEET 3	

ACED2c



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1

DETAIL G (350 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

Texas Instruments, Dallas, Texas	DWN DATE / ISSUE DATE	SIZE B / SCALE 4/1	DRAWING NO 2511543 REV D / SHEET 4

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