CHAPTER 3

Motor Control

AC Motor Control

3.1.1 Noiseless A.C. Motor Control: Introduction to a 20 kHz System

Controlling an a.c. induction motor by the technique of sinewave-weighted pulse-width modulation (PWM) switching gives the benefits of smooth torque at low speeds, and also complete speed control from zero up to the nominal rated speed of the motor, with only small additional motor losses.

Traditional power switches such as thyristors need switching frequencies in the audible range, typically between 400 and 1500Hz. In industrial environments, the small amount of acoustic noise produced by the motor with this type of control can be regarded as insignificant. By contrast, however, the same amount of noise in a domestic or office application, such as speed control of a ventilation fan, might prove to be unacceptable.

Now, however, with the advent of power MOSFETs, three-phase PWM inverters operating at ultrasonic frequencies can be designed. A three-phase motor usually makes even less noise when being driven from such a system than when being run directly from the mains because the PWM synthesis generates a purer sinewave than is normally obtainable from the mains.

The carrier frequency is generally about 20kHz and so it is far removed from the modulation frequency, which is typically less than 50Hz, making it economic to use a low-pass filter between the inverter and the motor. By removing the carrier frequency and its sidebands and harmonics, the waveform delivered via the motor leads can be made almost perfectly sinusoidal. RFI radiated by the motor leads, or conducted by the winding-to-frame capacitance of the motor, is therefore almost entirely eliminated. Furthermore, because of the high carrier frequency, it is possible to drive motors which are designed for frequencies higher than the mains, such as 400Hz aircraft motors.

This section describes a three-phase a.c. motor control system which is powered from the single-phase a.c. mains. It is capable of controlling a motor with up to 1kW of shaft output power. Before details are given, the general principles of PWM motor control are outlined.

Principles of Pulse-Width Modulation

Pulse-width modulation (PWM) is the technique of using switching devices to produce the effect of a continuously varying analogue signal; this PWM conversion generally has very high electrical efficiency. In controlling either a three-phase synchronous motor or a three-phase induction motor it is desirable to create three perfectly sinusoidal current waveforms in the motor windings, with relative phase displacements of 120˚. The production of sinewave

power via a linear amplifier system would have low efficiency, at best 64%. If instead of the linear circuitry, fast electronic switching devices are used, then the efficiency can be greater than 95%, depending on the characteristics of the semiconductor power switch.
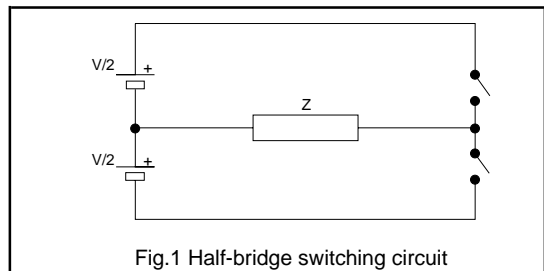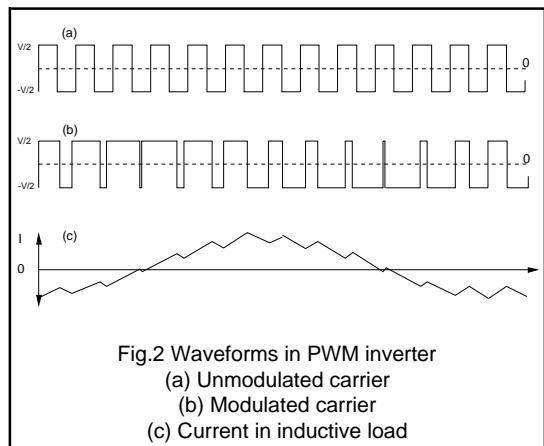

Fig.1 Half-bridge switching circuit

Fig.2 Waveforms in PWM inverter
(a) Unmodulated carrier
(b) Modulated carrier
(c) Current in inductive load

The half-bridge switching circuit in Fig.1 is given as an example: the switches can be any suitable switching semiconductors. If these two switches are turned on alternately for equal times, then the voltage waveform across the load is as shown in Fig.2a. The mean value of this waveform, averaged over one switching cycle is 0. This square wave with a constant 50% duty ratio is known as the 'carrier' frequency. The waveform in Fig.2b shows the effect of a slow variation or 'modulation' of the duty ratio; the mean voltage varies with the duty ratio. The waveform of the resultant load current depends on the impedance of the load Z. If Z is mainly resistive, then the waveform of the current will closely follow that of the modulated square wave. If, however, Z is largely inductive, as with a motor winding or a filter choke, then the switching square wave

will be integrated by the inductor. The result is a load current waveform that depends mainly on the modulation of the duty ratio.

If the duty ratio is varied sinusoidally in time, then the current in an inductive load has the form of a sinewave at the modulation frequency, lagging in phase, and carrying ripple at the switching frequency as shown in Fig.2c. The amplitude of the current can be adjusted by controlling the depth of modulation, that is, the deviation of the duty ratio from 50%. For example, a sinewave PWM signal which varies from 5% to 95%, giving 90% modulation, will produce a current nine times greater than that produced by a signal which varies only from 45% to 55%, giving only 10% modulation.

For three-phase a.c. motor control, three such waveforms are required, necessitating three pairs of switches like those shown in Fig. 1, connected in a three-phase bridge. The inductance required to integrate the waveform can usually be provided by the inductance of the stator windings of the motor, although in some instances it might be provided by the inductance of a separate low-pass filter. The modulations in the three switching waveforms must be maintained at a constant relative phase difference of 120°, so as to maintain motor current sinewaves which are themselves at a constant 120° phase difference. The modulation depth must be varied with the modulation frequency so as to keep the magnetic flux in the motor at approximately the design level.

In practice, the frequency of the modulation is usually between zero and 50Hz. The switching frequency depends on the type of power device that is to be used: until recently, the only devices available were power thyristors or the relatively slow bipolar transistors, and therefore the switching frequency was limited to a maximum of about 1 kHz. With thyristors, this frequency limit was set by the need to provide forced commutation of the thyristor by an external commutation circuit using an additional thyristor, a diode, a capacitor, and an inductor, in a process that takes at least 40µs. With transistors, the switching frequency was limited by their switching frequency and their long storage times.

In this earlier type of control circuit, therefore, the ratio of carrier frequency to modulation frequency was only about 20:1. Under these conditions the exact duty-ratios and carrier frequencies had to be selected so as to avoid all sub-harmonic torques, that is, torque components at frequencies lower than the modulation frequency. This was done by synchronising the carrier to a selected multiple of the fundamental frequency; the HEF4752V, an excellent IC purpose-designed for a.c. motor control, uses this particular approach. The 1kHz technique is still extremely useful for control of large motors because whenever shaft output powers of more than a few kW are required, three-phase mains input must be used, and there are, as yet, few available switching devices with combined high voltage rating, current rating, and switching speed.

However, using MOSFETs with switching times of much less than 1µs, the carrier frequency can be raised to the ultrasonic region, that is, to 20kHz or more. There are obvious system benefits with this higher frequency, but there are also several aspects of PWM waveform generation that become easier. It is possible to use a fixed carrier frequency because the sub-harmonics that are produced as a result of the non-synchronisation of the carrier frequency with a multiple of the fundamental are insignificant when the ratio of the carrier frequency to the fundamental frequency is typically about 400:1.
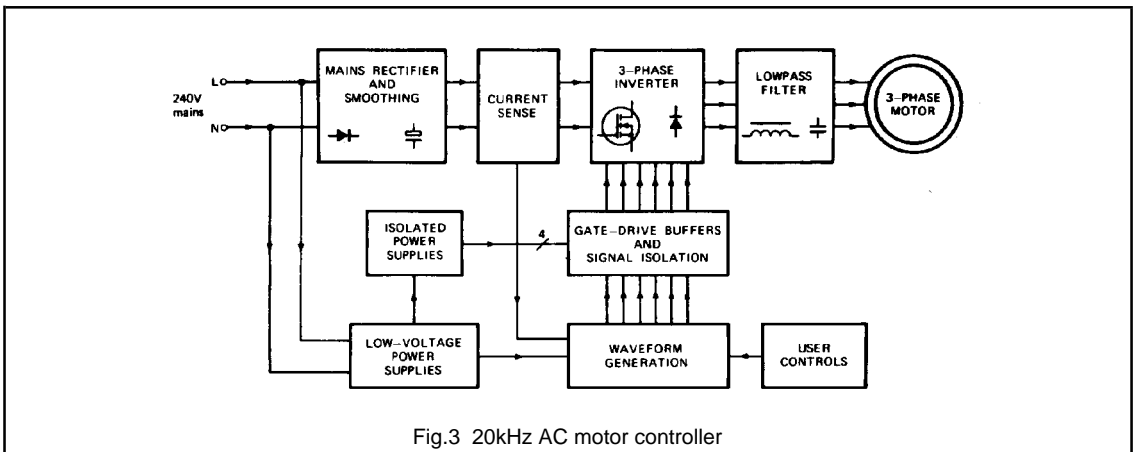

Fig.3 20kHz AC motor controller

To maintain good waveform balance, and thus avoid any d.c. in the motor, and therefore also avoid parasitic torques, a digital waveform generation technique is appropriate. The waveform can be stored as a 'look-up' table of numbers representing the sinewave. To generate the three phases, this table can be read at three points that have the correct 120° phase relationship. The numbers taken from the table represent the duty ratios corresponding to 100% modulation: these numbers can then be scaled down by multiplication or some equivalent technique to give the correct duty-ratio numbers for the modulation depth required.

The speed of the motor is controlled by the rate at which the reading pointers scan the look-up table and this can be as slow as desired. If the pointers are stationary, then the system will be 'frozen' at a particular point on the three-phase sinewave waveform, giving the possibility of obtaining static torque from a synchronous motor at zero speed. The rate at which the numbers are produced by this read-out process from the look-up table is constant and determines the carrier frequency.

To convert these three simultaneous parallel digital numbers into time lengths for pulses, three digital counters are needed. The counters can be designed to give double-edged modulation, such that both the leading edge and the trailing edge of each pulse move with respect to the unmodulated carrier. The line-to-line voltage across the load will have most of its ripple at a frequency of twice the switching frequency, and will have a spectrum with minimum even harmonics and no significant component below twice the switching frequency. Motor ripple current is therefore low and motor losses are reduced.

There is a further advantage to be obtained from the high ratio of carrier to modulation frequency: by adding a small amount of modulation at the third harmonic frequency of the basic fundamental modulation frequency, the maximum line-to-line output voltage obtainable from the inverter can be increased, for the following reason. The effect of the third harmonic on the output voltage of each phase is to flatten the top of the waveform, thus allowing a higher amplitude of fundamental while still reaching a peak modulation of 100%. When the difference voltage between any two phases is measured, the third harmonic terms cancel, leaving a pure sinewave at the fundamental frequency. This allows the inverter output to deliver the same voltage as the mains input without any significant distortion, and thus to reduce insertion losses to virtually zero.

Overview of a practical system

The principles outlined above are applied to a typical system shown in Fig.3. The incoming a.c. mains is rectified and smoothed to produce about 300V and this is fed to the three-phase inverter via a current-sensing circuit. The inverter chops the d.c. to give 300V peak-to-peak PWM waves at 20kHz, each having low-frequency modulation of its mark-space ratio. The output of the inverter is filtered to remove the 20kHz carrier frequency, and the resultant sinewaves are fed to the a.c. motor.
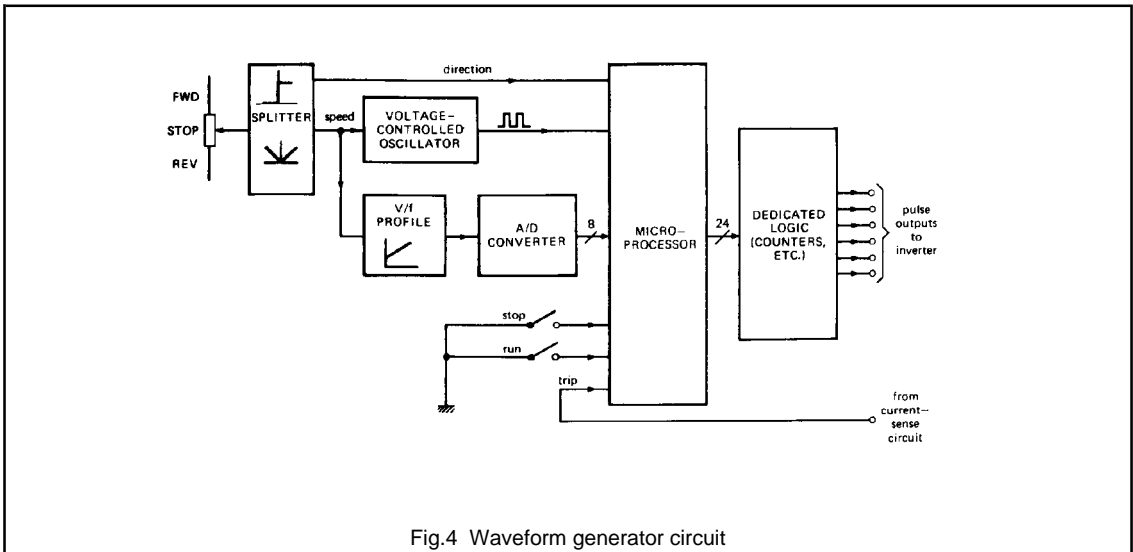

Fig.4 Waveform generator circuit

The six switches in the inverter are under the command of a waveform-generation circuit which determines the conduction time of each switch. Because the control terminals of the six switches are not at the same potential, the outputs of the waveform-generation circuits must be isolated and buffered. A low-voltage power supply feeds the signal processing circuit, and a further low-voltage power supply drives a switch-mode isolating stage to provide floating power supplies to the gate drive circuits.

Signal processing

Fig.4 shows a block diagram of the circuit which generates the PWM control signals for the inverter. The input to the system is a speed-demand voltage and this is also used for setting the required direction of rotation: the analogue speed signal is then separated from the digital direction signal. The speed-demand voltage sets the frequency of the voltage-controlled oscillator (VCO). Information to determine the modulation depth is derived from the speed-control signal by a simple non-linear circuit and is then converted by an analogue-to-digital converter into an 8-bit parallel digital signal.

A dedicated IC, type MAB8051, receives the clock signals from the VCO, the modulation-depth control number from the A/D converter, the direction-control logic signal, and logic inputs from the 'RUN' and 'STOP' switches. By applying digital multiplication processes to internal look-up table values, the microcomputer calculates the 'on-time' for each of the six power switches, and this process is repeated at regular intervals of 50μs, giving a carrier frequency of 20kHz. The pulses from the VCO are used for incrementing the pointers of the look-up table in the microcomputer, and thus control the motor speed.

The output signals of the microcomputer are in the form of three 8-bit parallel numbers: each representing the duty-ratio for the next 50μs switching cycle for one pair of inverter switches, on a scale which represents 0% to 100% on-time for the upper switch and therefore also 100% to 0% on-time for the complementary lower switch. A dedicated logic circuit applies these three numbers from the microcomputer to digital counters and converts each number to a pair of pulse-widths. The two signals produced for each phase are complementary except for a small 'underlap' delay. This delay is necessary to ensure that the switch being turned off recovers its blocking voltage before its partner is turned on, thus preventing 'shoot-through'.
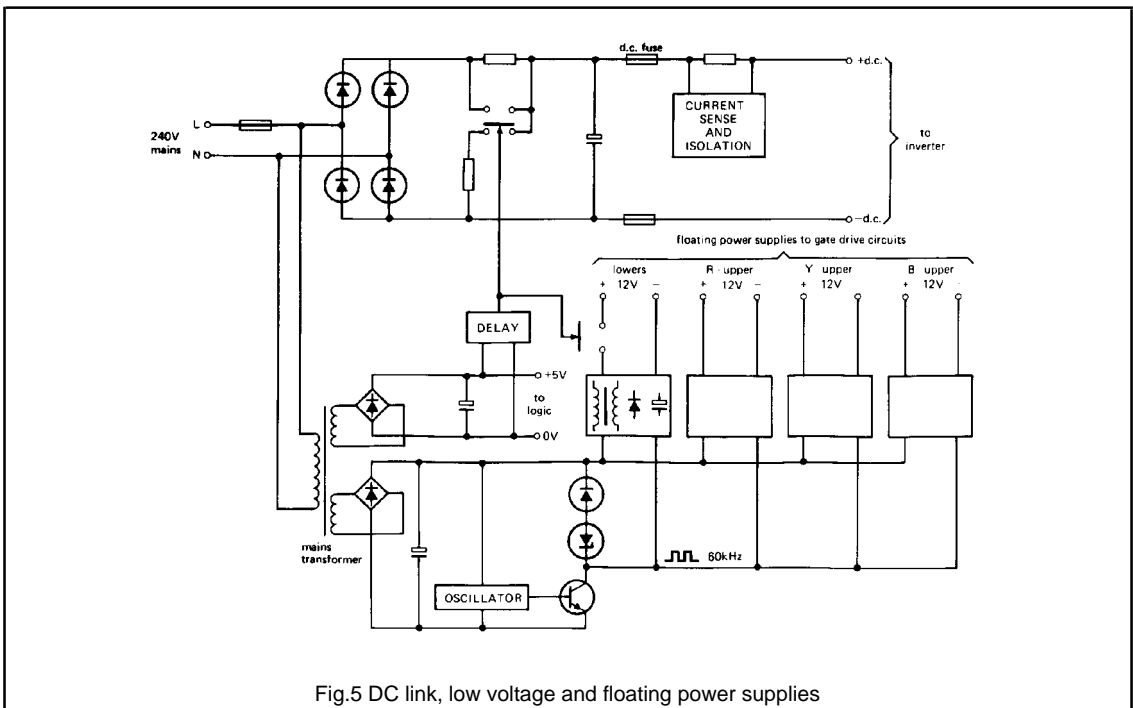

Fig.5 DC link, low voltage and floating power supplies

Other inputs to the microcomputer are the on/off switches, the motor direction logic signal, and the current-sensing signal. Each input triggers a processor interrupt, causing the appropriate action to be taken. The STOP switch and the overcurrent sense signals have the same effect, that of causing the microcomputer to instruct all six power switches in the inverter to turn off. The RUN switch causes the microcomputer to start producing output pulses. Any change in the direction signal first stops the microcomputer which then determines the new direction of rotation and adjusts its output phase rotation accordingly.

D.C. link and power supplies

The d.c. link and the low-voltage power supplies for the system are shown in Fig.5. The high voltage d.c. supply for the inverter is derived from a mains-fed bridge rectifier with a smoothing capacitor; the capacitor conducts both the 100Hz ripple from the rectified single-phase mains, and also the inverter switching ripple. A resistor, or alternatively a thermistor, limits the peak current in the rectifier while the capacitor is being charged initially. This resistor is shorted out by a relay after a time delay, so that the resistor does not dissipate power while the motor is running. As a safety measure, a second resistor discharges the d.c. link capacitor when the mains current is removed.

One of the d.c. link lines carries a low-value resistor to sense the d.c. link current. A simple opto-isolation circuit transmits a d.c. link current overload signal back to the signal processing circuit.

The logic circuitry of the waveform generator is powered conventionally by a 50Hz mains transformer, bridge rectifier, and smoothing capacitor. The transformer has two secondary windings; the second one provides power to a switched-mode power supply (SMPS), in which there is a switching transistor driven at about 60kHz to switch power through isolating transformers. Rectifying the a.c. outputs from the isolating transformers provides floating power supplies for the inverter gate drive circuits. As will be seen below, one supply is needed for the three 'lower' power switches (connected to a common d.c. link negative line), but three separate power supplies are needed for the three 'upper' switches (connected to the three inverter outputs). Thus four isolating transformers are required for the gate supply circuits. For low power systems the gate supplies can be derived directly from the d.c. link without excessive loss.

To prevent spurious turn-on of any inverter switch during the start-up process, the floating power supply to the lower three gate-drive circuits is connected only after a delay. The same delay is used for this as is used for the d.c. link charging-resistor bypass switch.
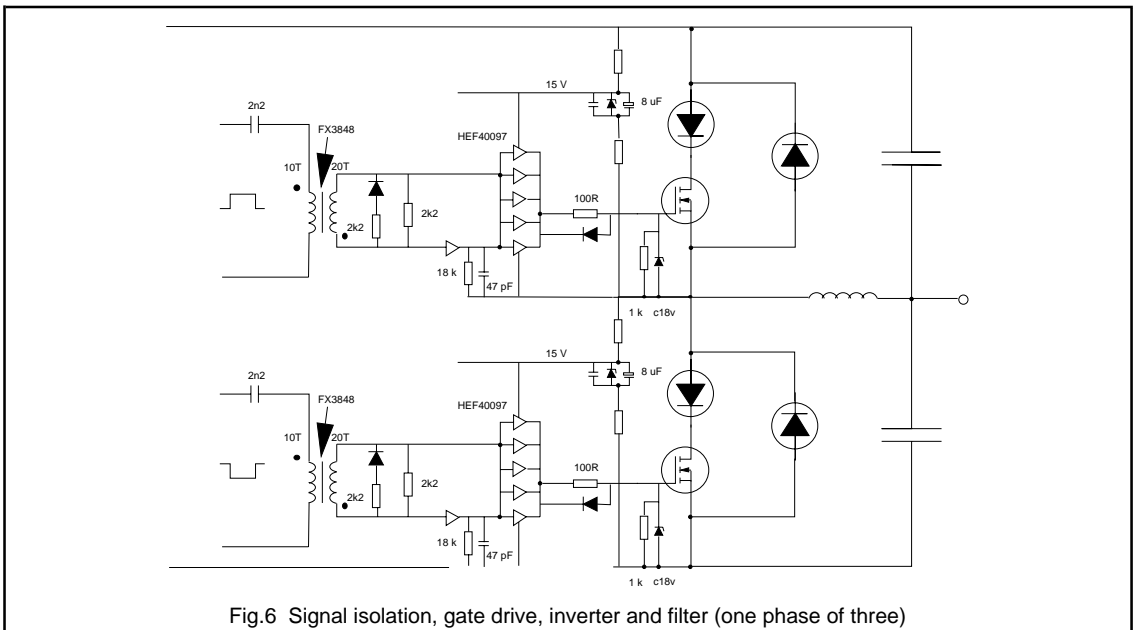

Fig.6 Signal isolation, gate drive, inverter and filter (one phase of three)

Signal isolation, gate drive, and inverter

The most important part of the system is the power inverter and it is the use of MOSFETs, with their short switching times, which makes it possible for the inverter to switch at 20kHz. It is in the area of the drive circuits to the power switches that using MOSFETs gives a saving in the number of components needed. Driving MOSFETs is relatively easy: the total power needed is very small because all that must be provided is the capability to charge and discharge the gate-source capacitance (typically between 1 and 2nF) by a few volts in a short time (less than 100ns). This ensures that the quality of the waveform is not degraded, and that switching losses are minimised.

In this circuit the six pulse outputs from the dedicated logic part of the waveform generator section are coupled to the MOSFET gate driver stages via pulse transformers. (see Fig.6). Each gate drive circuit is powered from one of the four floating power supplies described above. The three 'lower' stages share a common power supply, as the source terminals of the three 'lower' MOSFETs are all at the same potential. Each of the three 'upper' stages has its own floating power supply. The isolated signals are coupled to the gate terminals of the six MOSFETs by small amplifiers capable of delivering a few amperes peak current for a short time. Alternative gate driver circuits may use level shifting devices or opto-couplers. (Refer to "Power MOSFET Gate Drive Circuits" for further details.)

It will be seen from Fig.6 that each MOSFET has two associated diodes. These are necessary because the MOSFETs have built-in anti-parallel diodes with relatively long reverse-recovery times. If these internal diodes were allowed to conduct, then whenever load current commutated from a diode to the opposite MOSFET, a large current would be drawn from the d.c. supply for the duration of the diode reverse-recovery time. This would greatly increase the dissipation in the inverter. To avoid this, an external fast epitaxial diode is connected in anti-parallel with the MOSFET. Because the internal diode of the MOSFET has a very low forward voltage drop, a second low-voltage epitaxial diode must be connected in series with each MOSFET to prevent the internal diode from conducting at all. Thus, whenever the MOSFET is reverse-biased, it is the external anti-parallel diode which conducts, rather than the internal one. FREDFETs have internal diodes which are much faster than those of MOSFETs, opening the way for a further cost-saving by omitting the twelve diodes from the 3-phase inverter.

Output low-pass filter

For conventional, lower frequency inverters the size, weight and cost of output filter stages has held back their proliferation. An advantage of the constant high carrier frequency is that a small, economical low-pass filter can be designed to remove the carrier from the inverter output waveform. Compared with low frequency systems the filter component has been reduced by an order of magnitude, and can often be eliminated completely. In unfiltered systems cable screening becomes an important issue although on balance the increased cost of screening is less than the cost and weight of filter components.

A typical filter arrangement was shown in Fig.6. As an example, for a 50Hz motor-drive the filter would be designed with a corner-frequency of 100Hz, so that the attenuation at 20kHz would be about 46dB. The carrier frequency component superimposed on the output sinewave would therefore be only a few mV in 200Vrms. Fig.7 shows the relative spectral characteristics of different types of inverter switching strategies.

Fig.7 Spectral characteristics for different inverter
switching strategies
(a) Quasi-square
(b) 1kHz, 15 pulse, Synchronous
(c) 20kHz, Non-synchronous
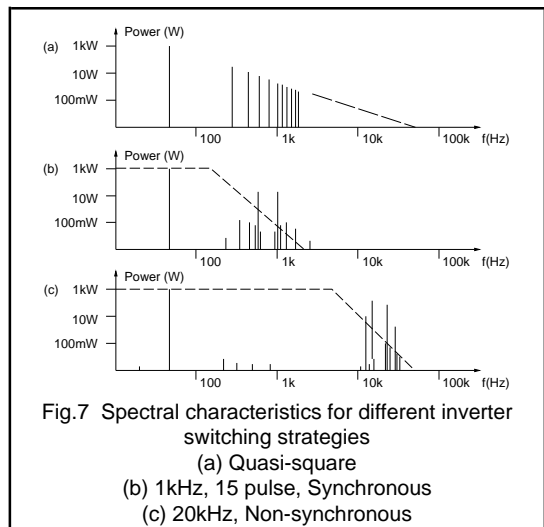
There are two main advantages in supplying the motor with pure sinewave power. First, the motor losses are small, because there is no rms motor current at the switching frequency, and second, there is less radio-frequency interference (RFI), because the switching frequency current components circulate entirely within the inverter and filter and do not reach the outside world.

Advantages of a 20 kHz system

The principal advantages of the system described here are:

- Controller and motor are acoustically quiet.
- PWM waveform is simple and thus easy to generate.
- Output filter for removal of carrier is economic.
- RFI is low because of output filter.
- No snubbers are required on power devices.
- High efficiency is easily obtainable.
- No insertion loss.

3.1.2 The Effect of a MOSFET's Peak to Average Current Rating on Inverter Efficiency

The control of induction motors using a synthesised sinewave generated using pulse width modulation (PWM) control is becoming increasingly popular. The peak current requirement of switches used for the inverter bridge is based on the maximum current when the output is short circuited. The overcurrent during a short circuit fault is limited by an inductor connected in series with the switches. There is therefore a trade off between the peak current carrying capability of the switch and the size of the inductor. It is demonstrated in this note that the efficiency of the circuit during normal operation of the inverter is affected by the size of this choke. The ratio of peak to average current carrying capability of Philips Powermos is typcially about four. This compares favourably with the typical ratio of Insulated Gate Bipolar Transistors (IGBTs) which is about three.

A simplified diagram of the inverter and the windings of the induction motor is shown in Fig. 1. The MOSFETs are driven with a PWM signal as shown in Fig. 2. The voltages at the outputs of each leg of the inverter are smoothed using a low pass filter and the inductance of the motor windings. The system has the following advantages; it uses an induction motor which is relatively cheap and maintenance free and it has the facility for 0 to 100% speed control. The near perfect sinewaves generated by the PWM technique produce a smooth torque, audible noise is reduced and filtering is made easier since MOSFETs make possible the use of switching frequencies above 20 kHz.
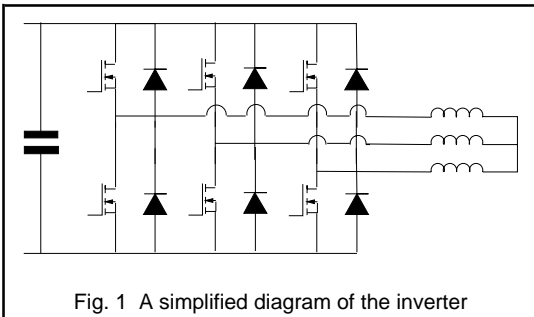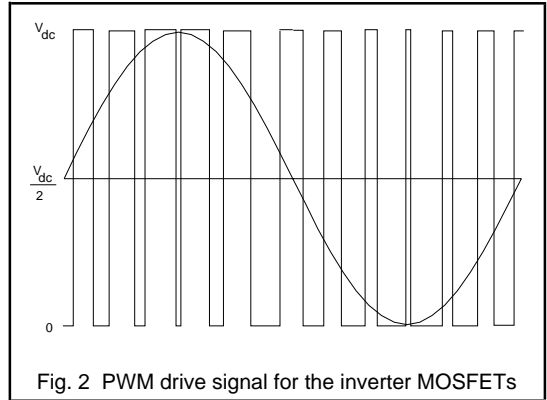
Fig. 2 PWM drive signal for the inverter MOSFETs

If the output of the inverter is short circuited there will be a rapid rise of current in the switches. To limit this peak current an inductor, L_s is often connected in each leg of the inverter as shown in Fig 3. The rate of rise of current under short circuit conditions, is then given in equation 1.

$$\frac{dI_T}{dt} = \frac{V_D}{L_s} \tag{1}$$
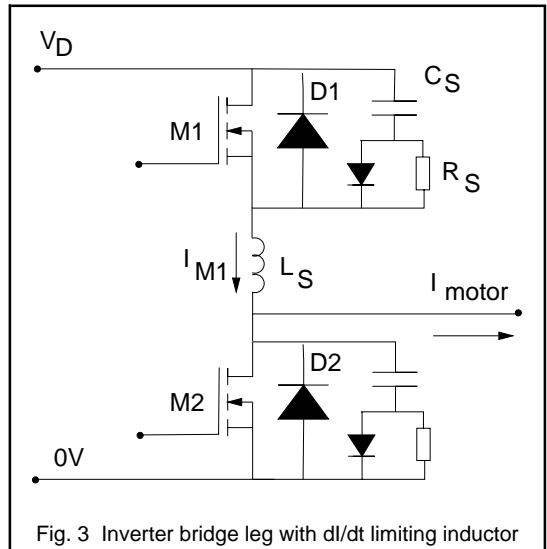
Fig. 3 Inverter bridge leg with dI/dt limiting inductor

Fig. 1 A simplified diagram of the inverter

When the MOSFETs turn this fault current (I_{SC}) off the energy in the inductor is transferred to a snubber capacitor, C_S. The overvoltage across the MOSFETs is given by equation 2.

$$V = \sqrt{\frac{L_s}{C_s}}.I_{SC} \qquad (2)$$

The presence of inductor L_S affects the normal operation of the inverter. When the MOSFET M1 in Fig. 3 turns off the diode D2 does not turn on until the voltage across C_s is equal to the d.c. link voltage, V_D. If the diode did turn on then the rate of rise of current in L_S would be given by equation 3.

$$\frac{dI_{M1}}{dt} = \frac{V_D - V_{CS} - V_{diode}}{L_s} \qquad (3)$$

This would be greater than the rate of rise of motor current so $I_{M1} > I_{motor}$ and the diode would have to conduct in the reverse direction, which is clearly not possible.

During the time when the capacitor C_S is charging up to V_D, the voltage across L_S will always be such as to increase the current in the bottom MOSFET, I_{M1}. When $V_{CS}=V_D$ the voltage across L_S will reverse and I_{M1} will fall. Diode D2 will now turn on. The energy stored in L_S will now be transferred to C_S. This energy will subsequently be dissipated in R_S and the MOSFET.

If the ratio of peak to average current carrying capability of the switch is large then it follows from equation 1 that L_S can be made smaller. This reduces the energy that is transferred to C_S when the MOSFETs switch off during normal operation. Hence the efficiency of the inverter is improved.

The short circuit fault current can be limited by connecting an inductor in the d.c. link as shown in Fig. 4. In this case analysis similar to that outlined above shows that the excellent ratio of peak to average current carrying capability of Philips Powermos again reduces the losses in the inverter. It has been shown that components chosen to ensure safe shutdown of inverters for motor drives can have deleterious effects on the efficiency of the inverter. In particular the addition of an inductor to limit the peak current through the semiconductor switches when the output is short circuited can increase the switching losses. The high peak to average current carrying capability of Philips Powermos reduces the size of this choke and the losses it causes.
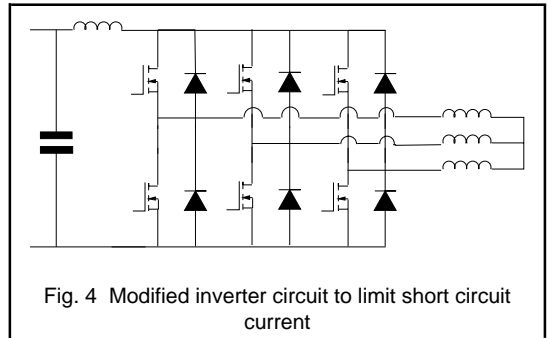
Fig. 4 Modified inverter circuit to limit short circuit current

3.1.3 MOSFETs and FREDFETs for Motor Drive Equipment

The paper discusses the properties of the FREDFET, a technology which yields a MOSFET with a very fast built-in reverse diode with properties similar to a discrete fast epitaxial rectifier. It is shown that its characteristics make the device an excellent choice for high frequency bridge leg systems such as 20 kHz AC motor control systems.

Investigations have been carried out in dedicated test circuits as well as in a 20 kHz ACMC system which show that the FREDFET exhibits very low diode losses. It compares favorably with a discrete solution, using two extra diodes to overcome the slow speed of the standard built-in diode, and also with devices from the present standard ranges.

Introduction

The Power MOSFET has inherent in its structure a large built-in diode which is present between the source and drain of the device. Under single switch applications such as forward and flyback converters, this diode isn't forward biased and consequently its presence can be ignored. In the case of bridge legs, however, this diode is forced into forward conduction and the properties of the diode become of prime importance. The reverse recovery of the built-in diode is relatively slow when compared with discrete fast recovery epitaxial diodes (FRED's). As a consequence, the currents flowing through the MOSFET and its diode can be high and the losses considerable.

Fig.1. ACMC bridge leg.
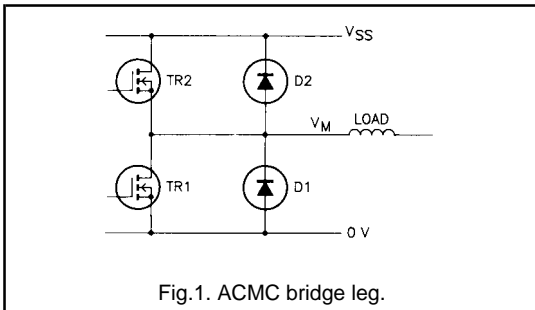
These losses can be reduced through the application of two extra diodes as discussed in section 2. A more elegant solution is a MOSFET with a built-in diode which exhibits properties similar to discrete fast epitaxial rectifiers. The FREDFET has been designed to satisfy this requirement. This paper presents the results of studies, carried out with new FREDFETs, comparing them with both the conventional MOSFET and the discrete solution.

MOSFETS in half bridge circuits

MOSFETS have gained popularity in high frequency AC motor controllers, since they enable frequencies above 20kHz to be used. The short on-times required in ACMC systems make the use of bipolar devices very difficult, due to the storage times. Both the short switching times and the ease of drive of the MOSFET are essential ingredients in the design of a ultrasonic ACMC. Difficulties can arise, however, when trying to use the built in source to drain diode of the MOSFETs.

One bridge leg of an ACMC is shown in Fig.1. When current is flowing out of the load, MOSFET T1 and freewheel diode D2 conduct alternately. Conversely, when flowing into the load, the current alternates between TR2 and D1. Consider the case when current is being delivered by the load, such that the pair TR1/D2 carries the current. When the MOSFET conducts current, the voltage at the drain is almost zero and the diode blocks. When the MOSFET is turned off by the drive circuit, the inductive load forces the voltage to increase making diode D2 conductive. Associated with conduction of the diode is a volume of stored charge which must be removed as the MOSFET TR1 returns to its on-state.

Fig.2. Recovery waveforms
Top: VDS, ID of TR1 turning on
Bottom: VD, ID of D2. (t=200ns/div)
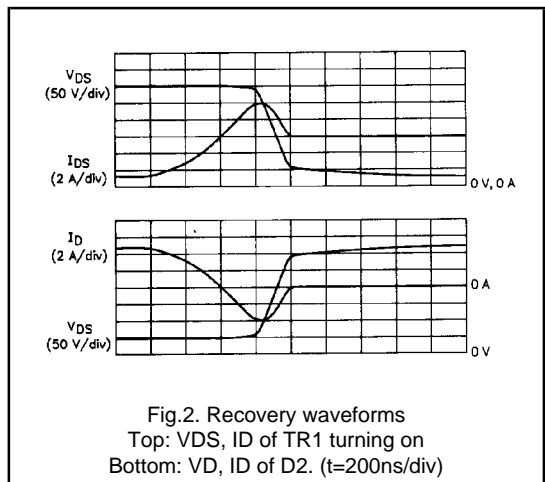
The waveforms appropriate to this situation can be found in Fig.2. One may observe that during the diode recovery time, the voltage across the MOSFET remains high whilst at the same time its current increases rapidly. Temporarily the drain current will increase to a level higher than the load current since the diode recovery current is added to it. Long recovery times and excessive charge storage result in a very high power dissipation in the MOSFET.
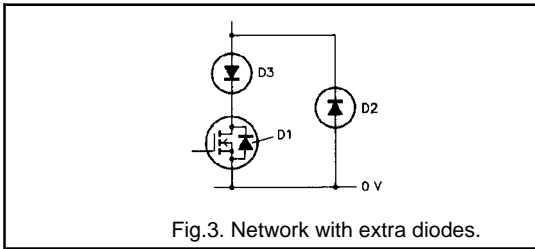
Fig.3. Network with extra diodes.

Using the inherent source drain diode of a conventional MOSFET as the freewheel diode results in considerable losses, since it is not optimised for fast switching or low stored charge. To avoid such losses the internal diode is usually deactivated by means of a special circuit (see Fig.3). This circuit, using two diodes D2 and D3, ensures that all freewheel current is flowing through the external diode D2 and not through the internal diode D1. When the MOSFET is switched on, the current flows via D3. This circuit is required for each MOSFET in the bridge. The FREDFET, which has a fast built-in diode offers the prospect of a much neater solution for these kind of circuits.

Technology of the FREDFET
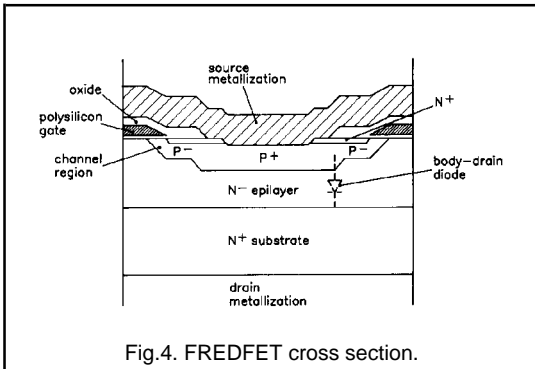
Fig.4. FREDFET cross section.

The power MOSFET is a majority carrier device and features fast turn-on and, in particular, fast turn-off. There are no charge storage effects such as in bipolar devices. In bridge leg applications the internal diode can become forward biased and the N- epitaxial region (see Fig.4) is flooded with holes, which must later be removed when the source becomes negatively biased again with respect to the drain.

The stored charge can be removed by holes diffusing from the N- epilayer into the P+ and P-body regions, and also by recombination of holes and electrons in the N- epitaxial region. A significant reduction in the stored charge Qrr can be achieved by doping the devices with heavy metal atoms to introduce recombination centres. A standard MOSFET will normally have a low concentration of recombination

centres. In the FREDFET the heavy metal doping does not have any significant effects on the threshold voltage or the transconductance, however, the efficiency with which the extra recombination centres remove the stored charge is improved substantially. This can be observed when comparing Qrr and trr results for killed and non-killed devices as described in the next section.

FREDFET measurements

A comparison of the reverse recovery characteristics of the internal diode has been made for a BUK637-500B FREDFET and a similar competitor conventional MOSFET. The devices were tested using an 'LEM 20 A Qrr' gear.
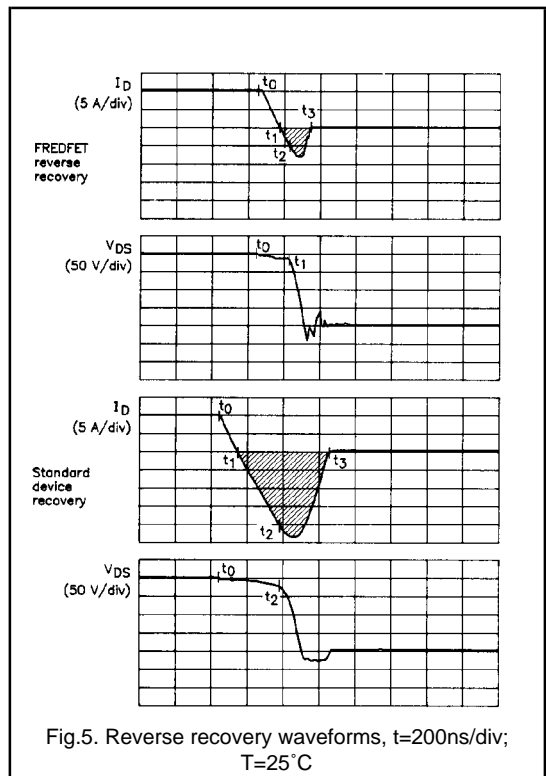
Fig.5. Reverse recovery waveforms, t=200ns/div; T=25°C

Oscillograms are presented in fig.5. showing the test waveforms for both the FREDFET and the conventional device. The diode turn-off process commences at $t=t_0$, where upon the forward current (set at 10A) is reduced at a preset 100A/usec. The current falls through zero and the diode passes into reverse conduction signifying the removal of stored charge. At $t=t_2$ sufficient charge has been removed for the formation of a depletion layer across the p-n junction. The dI/dt starts to fall and a voltage builds across an inductance in the source circuit such that the source becomes negatively biased with respect to drain.

Beyond t_2 the dI/dt reverses and the diode current begins to fall as the drain-source voltage rises to the clamp setting. The moment t_3 identifies the point at which the diode current has fallen to 10% of its peak value, Irrm.

The reverse recovery time, trr is defined as t_3-t_1 while the total stored charge Qrr is equal to the area of the shaded region, fig.5. A direct comparison of the diode reverse recovery at 25˚C is shown in fig.6. The respective values for trr, Qrr and Irrm are presented in Table 1.

T_j = 25˚C	trr (ns)	Qrr (uC)	Irrm (A)
BUK637-500B	193	1.2	8
Conventional device	492	7.5	23

Table 1.

It can be seen that Qrr is 84 % lower for the FREDFET while Irrm and trr approximately 60 % less. Fig.7 shows the same comparison measured at a junction temperature of 150˚C. Corresponding values of trr, Qrr and Irrm are shown in Table 2.
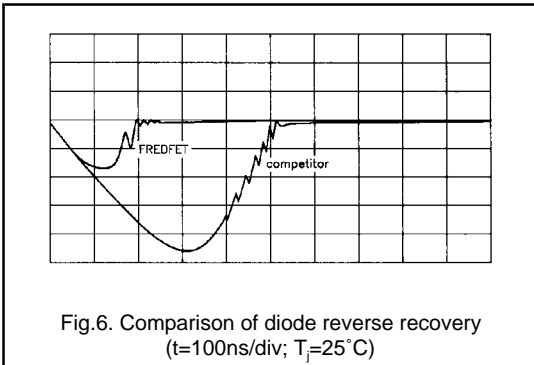
Fig.6. Comparison of diode reverse recovery
(t=100ns/div; T_j=25˚C)
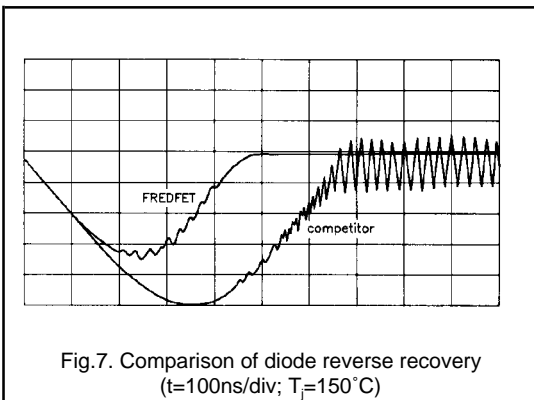
Fig.7. Comparison of diode reverse recovery
(t=100ns/div; T_j=150˚C)

T_j = 150˚C	trr (ns)	Qrr (uC)	Irrm (A)
BUK637-500B	450	4.5	17
Conventional device	650	10.5	26

Table 2.

While higher temperatures are known to reduce the effectiveness of recombination centres, it is clear that significant improvements still exist even at the peak junction temperature with savings of 55 % in Qrr and over 30 % in Irrm and trr evident for the FREDFET

Performance in a bridge circuit

The circuit of Fig.8 is a simplified representation of a bridge circuit, and was used to evaluate the performance of the BUK637-500B FREDFET against a conventional MOSFET and a conventional MOSFET configured with both series and parallel diodes.
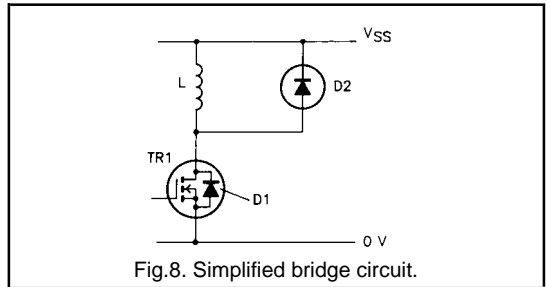
Fig.8. Simplified bridge circuit.

In each case the MOSFET in the bottom leg was switched on until the load current reached the desired value, at which point it was switched off, forcing the load current to flywheel through the inverse diode of the upper leg. The lower device was then switched on again to obtain reverse recovery of the upper diode. The current levels were set to simulate the conditions found in a 20 kHz 1 kVA ACMC. The device in the upper leg was mounted on a temperature controlled heatsink and the test was performed at very low duty cycle such that T_{case} approximated to T_j.

Oscillograms of current and voltage in relation to the lower leg are shown for the conventional device, conventional device plus external diodes and the FREDFET in Fig.9. The freewheel current in the upper diode is related to current in the MOSFET as shown in Fig.2. Also presented are the power waveforms for both the upper and lower legs in each case.

Fig.9. Waveforms (100ns/div; T_j=110˚C)
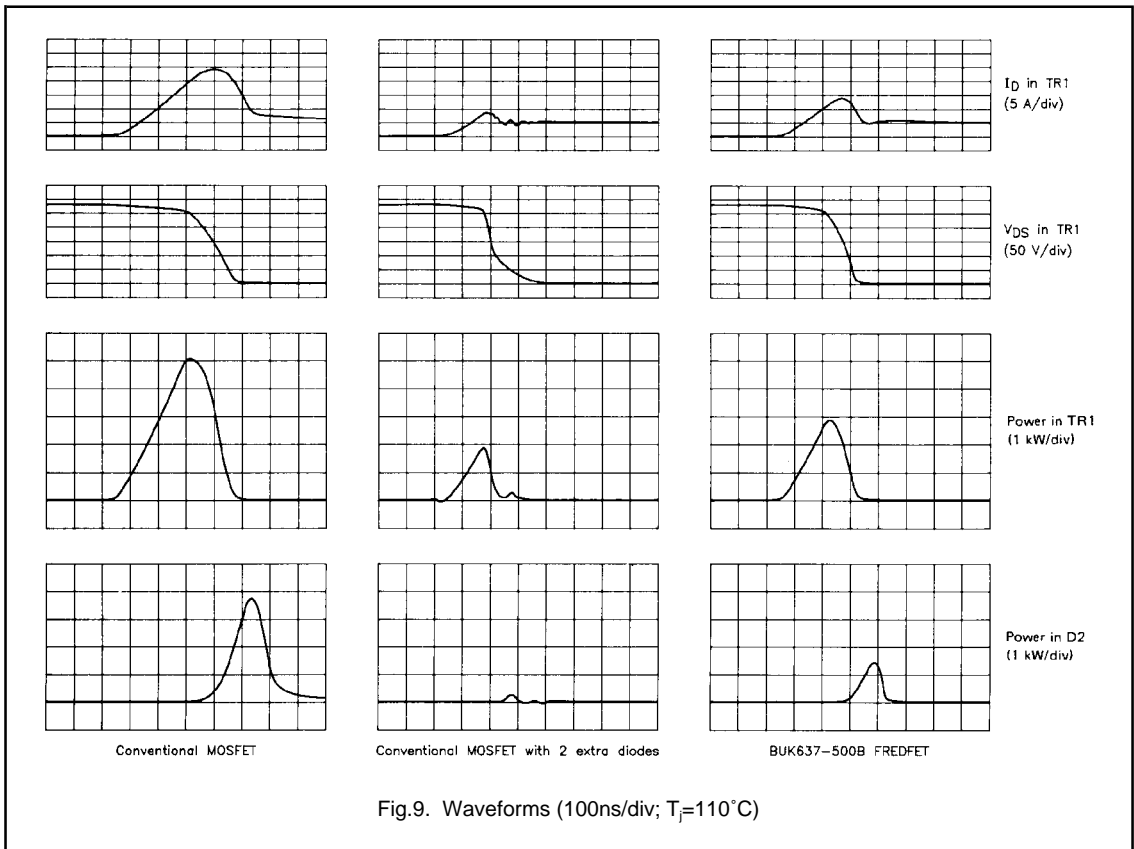
The superior performance of the FREDFET when compared to the conventional device is clear with the current overshoot kept to below 8 A compared to over 18 A using the latter. The lower reverse recovery current and faster trr are reflected in the power waveforms with nearly double the peak power being dissipated in the lower leg using a conventional device compared to that dissipated using the FREDFET. The power dissipated by the internal diode of the FREDFET is also observed to be remarkably reduced in comparison with the conventional MOSFET.

The performance of the three device implementations is summarised in table 3 which shows the total energy dissipated during switching in both legs for each case.

It can be seen that using a conventional MOSFET without the external diode circuitry involves a six fold increase in the energy dissipated in the MOSFET. However if a FREDFET implementation is used the turn-on energy is only a factor of two above the minimum achievable with the extra diodes. Energy loss in the diode itself is relatively small for both the FREDFET and the external diode configuration,

T_j = 110˚C	Energy Dissipated	
	Lower Leg (mJ)	Upper Leg (mJ)
Conventional MOSFET	1.2	0.533
MOSFET plus external diodes	0.2	0.035
BUK637-500B FREDFET	0.4	0.095

Table 3.

being less than 25 % that dissipated in the lower leg. For the conventional device the diode loss is more significant, equal to 44 % of the power dissipated during turn-on in the lower leg. The energy value presented above represent only the losses during turn-on, in addition to these are the on-state losses which for the external diode configuration include the extra power dissipated by the series diode.
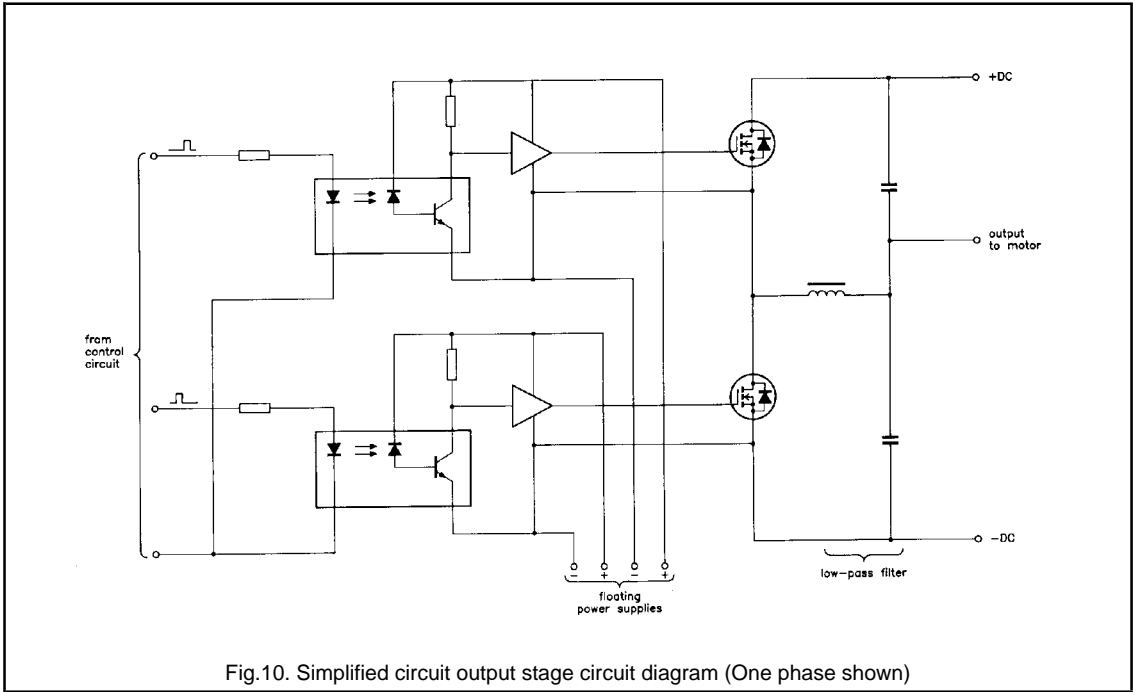
Fig.10. Simplified circuit output stage circuit diagram (One phase shown)

20 kHz ACMC with FREDFETS

The three device options discussed above have each been implemented in a 20 kHz AC Motor Control circuit. The inverter provides a three phase 1 kVA output from a single phase mains input. A simplified diagram of one of the output stages is presented in Fig.10.

Figure 11 shows the current waveforms as the load current commutates from the upper leg (anti-parallel diode in conduction) to the lower leg (turn-on of the MOSFET) for each device option. In each case the load current is 4.5 A. Fig.11a illustrates the large overshoot current obtained with a conventional device while Fig.11b shows what is achieved when the two external diodes are incorporated. Finally Fig.11c shows the current waveform for the FREDFET implementation where the current overshoot is kept below 1.5 A by the built-in fast recovery diode of the device.

Conclusions

It has been shown that the FREDFET compares favorably in ACMC systems compared with the standard MOSFET. The normally employed extra diodes can be omitted thus saving considerable costs in the system. The fast internal diode is seen to be comparable with the normally used fast epitaxial rectifiers and enables a simple ultrasonic ACMC.
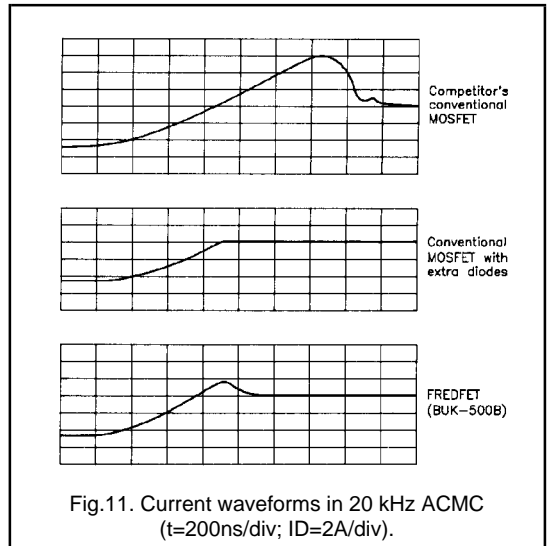
Fig.11. Current waveforms in 20 kHz ACMC (t=200ns/div; ID=2A/div).

3.1.4 A Designers Guide to PowerMOS Devices for Motor Control

This section is intended to be used as a designers guide to the use and selection of power MOSFETS and FREDFETS in a.c. motor control (ACMC) applications. It is particularly concerned with the variable speed operation of induction motors using pulse width modulation (PWM) techniques. One of the most important considerations in the design of ACMC inverters is the optimum choice of power switching device and heatsinking arrangement. Other factors which relate to the losses in the power switch are switching speed and design of suitable gate drive circuits. This section addresses each of these factors and presents a series of design graphs relating system operating temperature to device type and heatsink size for systems rated up to 2.2kW and operated from a single phase supply.

It should be noted that this article refers to some products which may not be available at this time.

Introduction

Variable speed control of induction motors is a widespread requirement in both industrial and domestic applications. The advantages of an induction motor drive over alternative systems such as d.c. motor controllers include:

> -high reliability and long life
> -low maintenance requirements
> -brushless operation
> -availability of standard machines.

With the advent of power switching devices able to provide the required ratings for ACMC applications and the availability of fast PWM pattern generation circuits these advantages have lead to an increasing number of applications where the inverter-fed induction motor system produces a cost effective drive. Before considering in detail the use of MOSFETs and FREDFETs in ACMC inverters it is worth briefly considering the principles and operation of the induction motor, the PWM method of voltage control and the characteristics of the switching devices.

The induction motor

Induction motors are three phase machines where the speed of rotation of the stator field (the synchronous speed, N_s) is determined by the number of poles, p, and the frequency of the applied voltage waveforms, f_s.

$$N_s = \frac{120.f_s}{p} \qquad (rpm) \qquad (1)$$

Torque production in an induction motor is due to the interaction of the rotating stator field and currents in the rotor conductors. Torque is developed when the rotor speed 'slips' behind the synchronous speed of the stator travelling field. Fig.1 shows the torque-speed characteristic of an induction motor where ω_s is the speed of the stator field ($\omega_s=2\pi f_s$) and ω_r is the rotor speed. The difference between the two is usually relatively small and is the slip speed. The solid portion of the characteristic is the main region of interest where the motor is operating at rated flux and at low slip. In this region the rotor speed is approximately proportional to the stator supply frequency, except at very low speeds. The operating point of the motor on its torque-speed characteristic is at the intersection of the load torque line and the motor characteristic. For small amounts of slip and at constant airgap flux the motor torque is proportional to the slip speed.
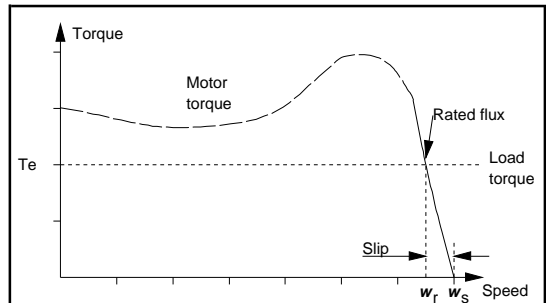
Fig.1 AC induction motor, Torque-Speed characteristic.
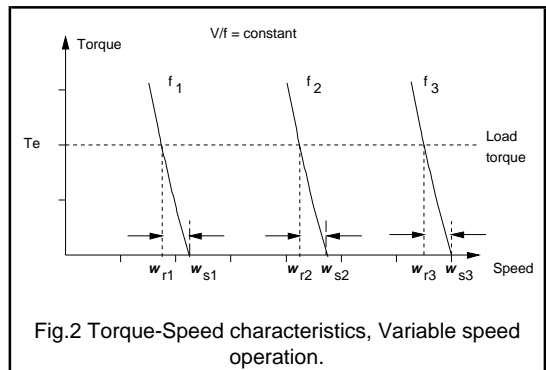
Fig.2 Torque-Speed characteristics, Variable speed operation.

In a variable speed system the motor is operated on a series of torque-speed characteristics as the applied frequency is increased. Fig.2 shows a set of characteristics for three conditions, ω_{s1}, ω_{s2} and ω_{s3}. The corresponding rotor speeds are ω_{r1}, ω_{r2} and ω_{r3}. However in order that the airgap flux in the motor is maintained at its rated value then the applied voltage must be reduced in proportion to the applied frequency of the travelling field. This condition for constant airgap flux gives the constant v/f requirement for variable speed control of a.c. induction motors. At low speeds this requirement may be modified by voltage boosting the supply to the motor in order to overcome the increased proportion of 'iR' voltage drop in the motor windings which occurs at low speeds.

The PWM Inverter

A variable voltage, variable frequency three phase supply for the a.c. induction motor can be generated by the use of a pulse width modulated (PWM) inverter. A schematic diagram of the system is shown in Fig.3. The system consists of a rectified single phase a.c. supply, which is usually smoothed to provide the d.c. supply rails for the main switching devices. Alternate devices in each inverter leg are switched at a high carrier frequency in order to provide the applied voltage waveforms to the motor. During each switching cycle the motor current remains approximately constant due to the inductive nature of the AC motor load.

Fig.3 PWM inverter, block diagram.
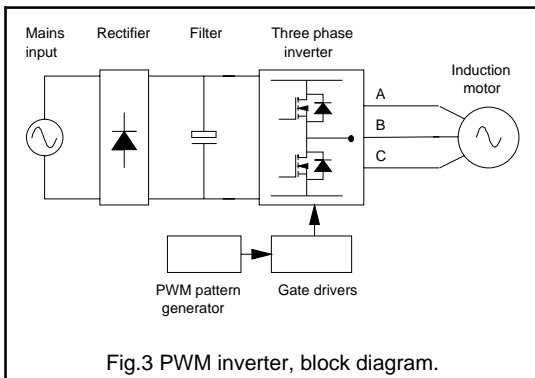
In the circuit of Fig.3 the main switching devices are MOSFETs and each MOSFET has a freewheeling diode connected in antiparallel. The motor load current is determined by the circuit conditions. When the load current in a particular phase is flowing into the motor then conduction alternates between the top MOSFET and the bottom freewheel diode in that inverter leg. When the load current is flowing from the motor then the bottom MOSFET and top diode conduct alternately. Fig.4 shows a typical

Fig.4 PWM phase voltage waveform.
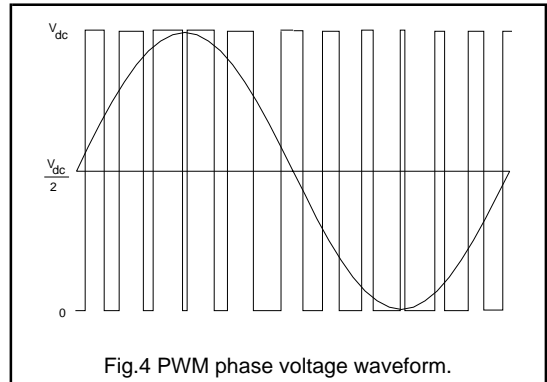
sinusoidal PWM voltage waveform for one motor phase. The three phases are maintained at 120° relative to each other.

Both the frequency and amplitude of the fundamental component of the output voltage waveform can be varied by controlling the timing of the switching signals to the inverter devices. A dedicated i.c. is usually used to generate the switching signals in order to maintain the required v/f ratio for a particular system.[1] The PWM algorithm introduces a delay between the switching signal applied to the MOSFETs in each inverter leg which allows for the finite switching times of the devices and thus protects the system from shoot-through conditions.

Additional harmonic components of output voltage, such as the third harmonic, can be added to the PWM switching waveform.[2,3] The effect of adding third harmonic to the output voltage waveform is to increase the amplitude of the fundamental component of output voltage from a fixed d.c. link voltage. This is shown in Fig.5. The third harmonic component of output phase voltage does not appear in the output line voltage due to the voltage cancellation which occurs in a balanced three phase system. Using this technique it is possible to obtain an output line voltage at the motor terminals which is nearly equal to the voltage of the single phase supply to the system.

For many applications the PWM ACMC system is operated at switching speeds in the range 1kHz to 20kHz and above. Operation at ultrasonic frequencies has advantages that the audible noise and RFI interference are considerably reduced. The advantages of PowerMOS devices over bipolar switching devices are most significant at these switching speeds due to the low switching times of PowerMOS devices. Additional advantages include good overload capability and the fact that snubber circuits are not usually required. It is usually straightforward to operate PowerMOS devices in parallel to achieve higher system currents than can be achieved with single devices. This is because the devices have a positive temperature coefficient of resistance and so share the load current

Fig.5 Addition of third harmonic to output voltage waveform.

Fig.6 Inverter bridge leg.

Fig.7 Diode reverse recovery waveforms.

Fig.8 Circuit to deactivate MOSFET intrinsic diode.
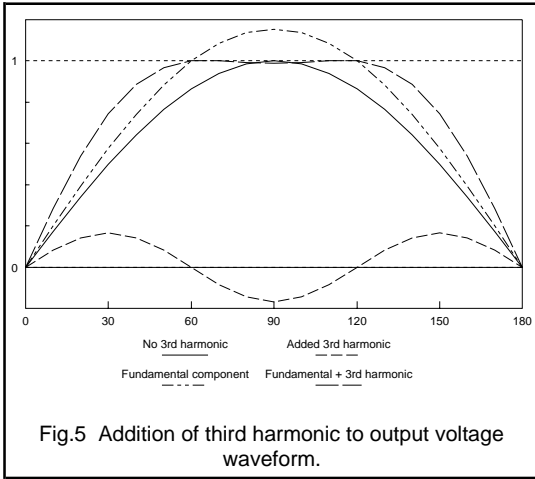
equally. The simple gate drive requirements of PowerMOS devices means that a single gate circuit can often be used for a range of devices without modification.

MOSFETs and FREDFETs in ACMC

One of the features associated with the transfer of conduction between the switching devices and the freewheel diodes in an inverter circuit is the reverse recovery of the freewheel diode as each conducting MOSFET returns to its on-state. Reverse recovery current flows due to the removal of stored charge from a diode following conduction. Fig.6 shows the device current paths in an inverter leg when conduction is transferred from the top diode to the bottom MOSFET.

The switching waveforms are shown in Fig.7 where the diode reverse recovery current is I_{rr} and the time taken for the reverse recovery currents to be cleared is t_{rr}. The amount of stored charge removed from the body of the diode is represented by the area Q_{rr}. The reverse recovery current flows through the MOSFET which is being turned on in addition to the load current and thus causes additional turn-on losses. The amount of stored charge increases with increasing temperature for a given diode. Both the magnitude of the reverse recovery current and its duration must be reduced in order to reduce the switching losses of the system.

This effect is important because inherent in the structure of a power MOSFET is a diode between the source and drain of the device which can act as a freewheeling diode in an inverter bridge circuit. The characteristics of this diode are not particularly suited to its use as a freewheel diode due to its excessive charge storage and long recovery time. These would lead to large losses and overcurrents during the MOSFET turn-on cycle.
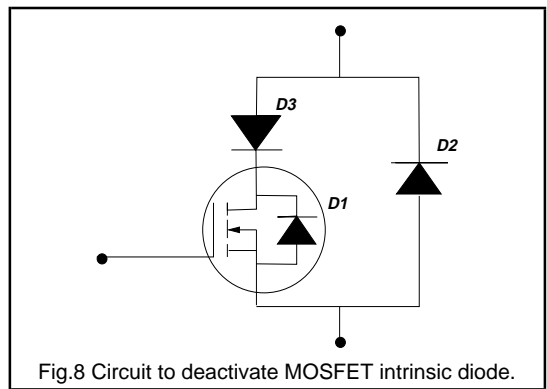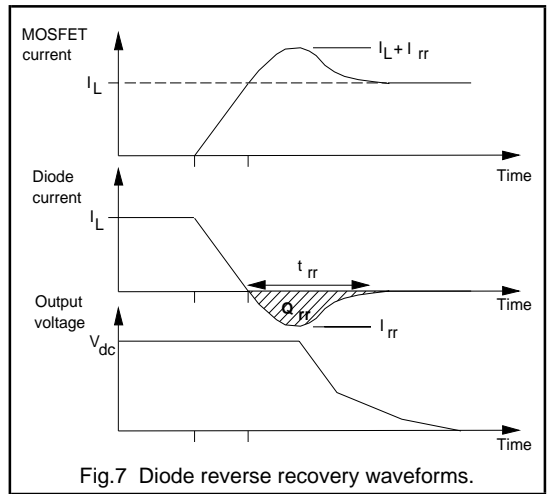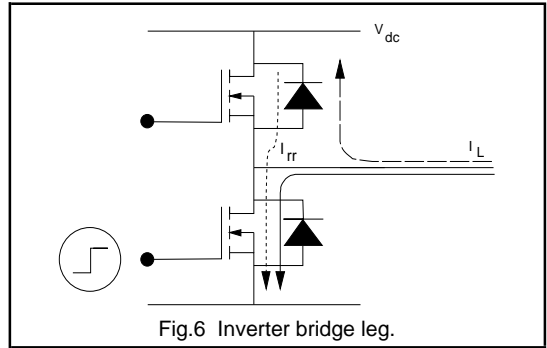
In inverter applications the internal diode of a MOSFET is usually deactivated by the circuit of Fig.8. Conduction by the internal MOSFET diode is blocked by the series Schottky diode (D3). This series device must carry all the MOSFET current and so contributes to the total conduction losses. The external diode, usually a fast recovery epitaxial

diode (FRED), carries the freewheel current. This device is chosen such that its low values of I_{rr} and t_{rr} reduce the overall switching losses. The FREDFET is essentially a MOSFET with a very fast built-in diode, and hence can replace the network of Fig.8 with a single device giving a very compact ACMC inverter design using only six power switches.[4] The reverse recovery properties of a FREDFET diode are similar to those of a discrete FRED thus giving a considerably neater circuit without any loss in switching performance.

ACMC design considerations

Voltage rating

The first selection criteria for a PowerMOS device in an inverter application is the voltage rating. For a 240V a.c. single phase supply the peak voltage is 340V. Assuming that the rectifier filter removes the voltage ripple components which occur at twice the mains frequency, and dependent on the values of the filter components and rectifier conduction voltage, then the dc link voltage will be around 320V. Devices with a voltage rating of 500V will allow sufficient capability for transient overvoltages to be well within the capability of the device. Thus the dc link voltage is given by:

$$V_{dc} = \sqrt{2}.V_{ac} \qquad (2)$$

where V_{ac} is the rms ac input line voltage.

The output phase voltage, shown in Fig.4, switches between the positive and negative inverter rail voltages. The mean value of the output voltage is $V_{dc}/2$. Neglecting the delays which occur due to the finite switching times of the devices then the maximum rms output phase voltage is given by:

$$V_{ph} = \frac{1}{\sqrt{2}}.\frac{V_{dc}}{2} \qquad (3)$$

and hence the rms output line voltage is:

$$V_{line} = \sqrt{3}.V_{ph} = \sqrt{3}.\frac{V_{dc}}{2.\sqrt{2}} \qquad (4)$$

Comparing equations (2) and (4) shows that:

$$V_{line} = 0.866.V_{ac} \qquad (5)$$

This shows that the fundamental rms line output voltage is 13% less than the rms ac input voltage. Adding third harmonic to the PWM output waveform can restore this rms output voltage to the ac input voltage. In a practical system the effect of switching delays and device conduction voltages can reduce the output voltage by upto 10-15%.

Current rating

The nameplate rating of an induction motor is usually quoted in terms of its power (W) and power factor ($\cos\varphi$). The VA requirement of the inverter is found from the simple equation:

$$Power(W) = \eta.\cos\varphi.VA \qquad (6)$$

where η is the efficiency. In terms of the rms motor line voltage (V_{line}) and output current (I_L):

$$VA = \sqrt{3}.V_{line}.I_L \qquad (7)$$

The efficiency of small ac induction motors can be quite high but they usually run at quite poor power factors, even at rated conditions. For small induction motors (<2.2kW) the efficiency-power factor product is typically in the range 0.55 to 0.65. The exact value will vary from motor to motor and improves with increasing size. Thus from equations (6) and (7) it is possible to calculate the approximate rms current requirement. The peak device current for sinusoidal operation is given by equation (8). (NB. The devices will experience currents in excess of this value at switching instants.)

$$I_{max} = \sqrt{2}.I_L \qquad (8)$$

Device package

The device package chosen for a particular application will depend upon device rating, as discussed above, as well as circuit layout and heatsinking considerations. Philips PowerMOS devices are available in a range of package types to suit most applications.

Drive considerations

Unlike bipolar devices the MOSFET is a majority carrier device and so no minority carriers must be moved in and out of the device as it turns on and off. This gives the fast switching performance of MOSFET devices. During switching instants the only current which must be supplied by the gate drive is that required to charge and discharge the device capacitances. In order to switch the device quickly the gate driver must be able to rapidly sink and source currents of upto 1A. For high frequency systems the effect of good gate drive design to control switching times is important as the switching losses can be a significant proportion of the total system losses.

Fig.9 shows an equivalent circuit of the device with the simplest gate drive arrangement. The drain-source capacitance does not significantly affect the switching performance of the device. Temperature only has a small effect on the values of these capacitances and so the device switching times are essentially independent of temperature. The device capacitances, especially C_{GD}, vary with V_{DS} and this variation is plotted in data for all PowerMOS devices.
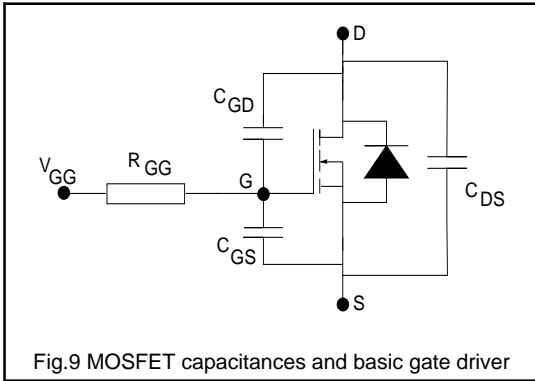
Fig.9 MOSFET capacitances and basic gate driver

Turn-on (Fig.*10*)

A turn-on gate voltage pulse commences at t_0. The gate voltage v_{GS} rises as current flows into the device via R_{GG}. C_{GS} starts to charge up until v_{GS} reaches its threshold value $v_{GS(TO)}$ at time t_1. The device is now operating in its active region with a relatively high power loss. The MOSFET current, rises as a function of $v_{GS}-v_{GS(TO)}$ and causes a corresponding fall in the diode current. Thus the rate of fall of diode current, and hence the amount of diode reverse recovery current, is controllable by the rate of rise of v_{GS}. At time t_4 the diode has recovered and the MOSFET current is equal to the load current, I_L. V_{GS} is clamped to $v_{GS(IL)}$ and so the gate current is given by:

$$i_G = \frac{v_{GG} - v_{GS(IL)}}{R_{GG}} \quad (9)$$

This current flows through C_{GD}, discharging it and so the rate of fall of output voltage is given by:

$$\frac{dv_{DS}}{dt} = \frac{i_G}{C_{GD}} = \frac{(v_{GG} - v_{GS(IL)})}{R_{GG}.C_{GD}} \quad (10)$$

The fall in v_{DS} commencing at time t_3 is not linear, principally because C_{GD} increases with reducing v_{DS}. At time t_5 C_{GD} is fully discharged and the device is on. The gate voltage continues to charge up to its final value, v_{GG}. It is usual to have a value of v_{GG} significantly higher than $v_{GS(IL)}$ because $r_{DS(on)}$ falls with increasing v_{GS}. Additionally a high value if v_{GG} speeds up the turn-on time of the device and provides some noise immunity.

Switching losses occur during the period t_1 to t_5. The minimum turn-on time is usually governed by the dv/dt capability of the system. Reducing the turn-on time increases the amount of diode reverse recovery current and hence increases the peak power dissipation, however the total power dissipated tends to reduce.
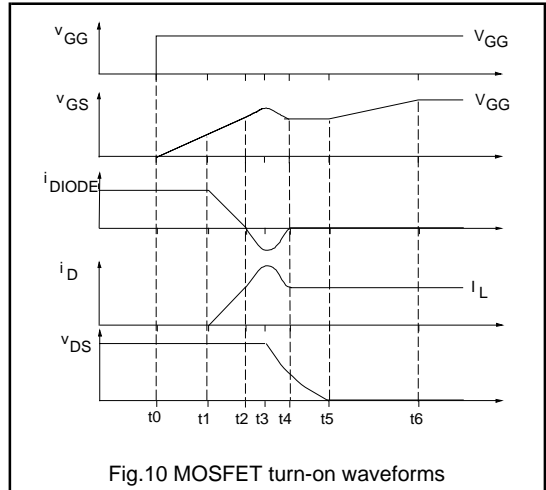
Fig.10 MOSFET turn-on waveforms
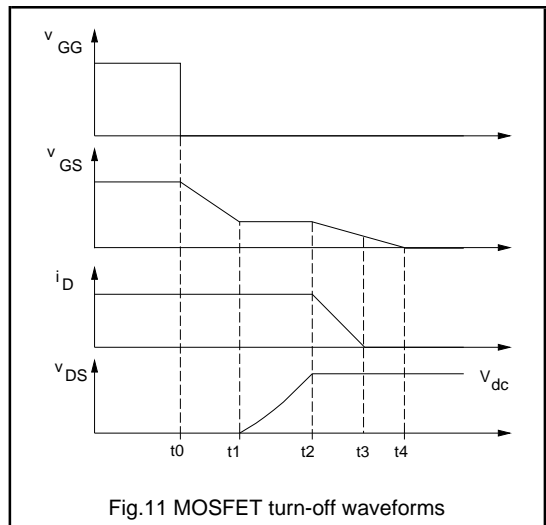
Fig.11 MOSFET turn-off waveforms

Turn-off (Fig.*11*)

Unlike the conditions which occur at turn-on there is no interaction between the switching devices at turn-off. The switching waveforms are, therefore, relatively straightforward. The gate voltage is switched to ground or, if very fast turn-off is required, to a negative voltage. During the delay time t_0 to t_1 the gate voltage falls to the value required to maintain the output current, I_O. From time t_1 to t_2 the gate supply is sinking current and C_{GD} charges the drain up to the positive rail voltage. V_{GS} then continues to fall and so the device current falls between times t_2 and t_3, At t_3 the gate voltage falls below its threshold value and the device turns off. The rate of rise of output voltage is:

$$\frac{dv_{DS}}{dt} = \frac{i_G}{C_{GD}} = \frac{v_{GS(IL)}}{R_{GG}.C_{GD}} \qquad (11)$$

Parasitic turn-on

In a high frequency system the device switching times are necessarily short and so the rates of change of inverter output voltage are high. The high values of dv/dt which occur when one device turns on can cause a sufficiently high voltage at the gate of the other device to also turn it on. The coupling occurs via C_{GD} and C_{GS}. If the rate of change of output voltage due to one device turning on is given by dv_{DS}/dt then the voltage that would be seen at the gate of the other device if it were left open circuit is:

$$\frac{dv_{GS}}{dt} = \frac{C_{GD}}{C_{GS}+C_{GD}}.\frac{dv_{DS}}{dt} \qquad (12)$$

If C_{GS} is shorted out by a zero impedance, then clearly dV_{GS}/dt can be reduced to zero. In practice achieving a zero impedance in the gate-source circuit is extremely difficult and dV_{GS}/dt will not be zero. In the worst case this rising gate voltage will turn the device fully on and a destructive shoot-through condition occur. If the conditions are less severe then the MOSFET may only turn on for a short period of time giving rise to an additional overcurrent in the turn-on cycle of the device being switched. Parasitic turn-on, as this effect is referred to, must be prevented by either limiting dv_{DS}/dt or by ensuring that v_{GS} is clamped off. In systems where the off-state gate-source voltage is negative then the possibility of parasitic turn-on can be reduced.

Gate drive circuits for ACMC inverters

The previous section discussed device switching waveforms using a resistive gate drive circuit. In this section various alternative gate drive circuits for ACMC applications are presented and compared. The discussion assumes that each MOSFET gate drive circuit is isolated and driven using a CMOS buffer capable of sinking and sourcing the required gate current. In unbuffered gate drive circuits the leakage inductance of an isolating pulse transformer can increase the gate impedance, thus reducing the maximum possible switching rate and making the MOSFET more susceptible to parasitic turn-on. A zener diode clamp protects the gate-source boundary from destructive overvoltages. Identical drivers are used for the top and bottom devices in each inverter leg. The gate drive circuits presented here were tested using BUK638-500A FREDFETS and BUK438-500A MOSFETS in a 20kHz, 2.2kW ACMC system.

Figure 12 shows the simplest arrangement which gives independent control of the turn-on and turn-off of the MOSFET. Increasing the gate impedance to reduce dV_{DS}/dt levels will raise the susceptibility to parasitic turn-on problems. The gate-source voltage can be clamped off
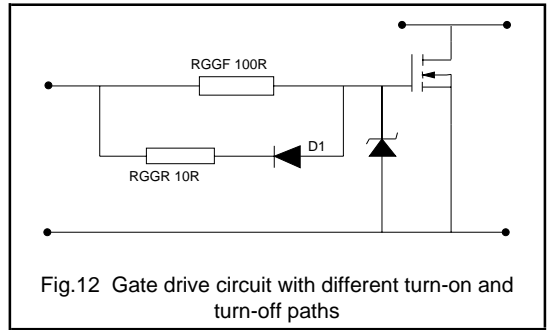
Fig.12 Gate drive circuit with different turn-on and turn-off paths
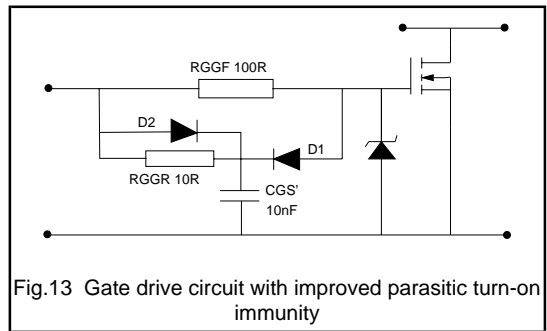
Fig.13 Gate drive circuit with improved parasitic turn-on immunity

more effectively if the dynamic impedance between gate and source is reduced as shown in the circuit of Fig.13. The additional gate-source capacitance ensures that v_{GS} does not rise excessively during conditions when parasitic turn-on could occur (Equation 12). The external capacitor C_{GS}' must be charged up at turn-on. If C_{GS}' is made too large then the current required may be beyond the rating of the drive buffer. The speed-up diode, D2, ensures that the turn-on is not compromised by C_{GS}' and R_{GGR}. At turn off the additional capacitance slows down dI_D/dt since the gate-source RC time constant is increased. It must be noted that one effect of the turn-off diode, D1, is to hold the off-state value of v_{GS} above 0V, and hence somewhat closer to the threshold voltage of the device.

An alternative circuit which may be used to hold the MOSFET off-state gate-source voltage below its threshold value is shown in Fig.14. The pnp transistor turns on if the gate-source voltage is pulled up via C_{GD} and C_{GS} and thus the device remains clamped off.
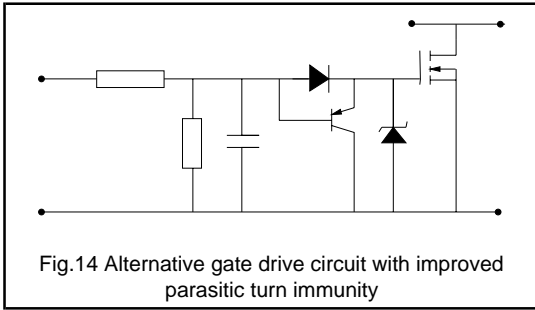
Fig.14 Alternative gate drive circuit with improved parasitic turn immunity
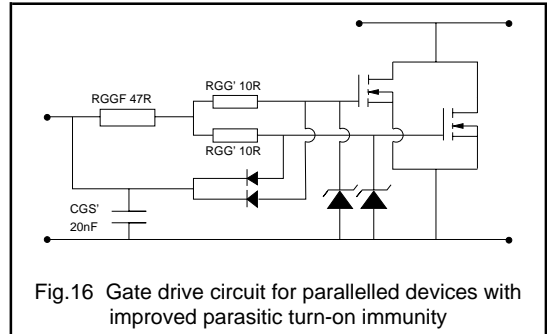
Fig.16 Gate drive circuit for parallelled devices with improved parasitic turn-on immunity

Parallelling of PowerMOS devices

Moving to a system using parallelled MOSFETs requires only slight modifications to the gate drive circuit. One consideration may be the capability of the drive buffer to provide the currents required at the switching instants. The switching speed of the system can be maintained. using a lower impedance gate drive. It is recommended that small differential resistors, as shown in Fig.15, are used to damp out any oscillations which may occur between the switching devices and the rest of the circuit. The circuit of Fig.13 can be modified for operation with parallelled devices to that shown in Fig.16.

Circuit layout considerations

The effects of poor circuit design and layout are to increase RFI and noise and to compromise the performance and speed of the system due to stray inductances. The precautions which must be taken to minimise the amount of stray inductance in the circuit include:

- positioning the gate drive circuits, especially zener diodes and dv/dt clamping circuits as close as possible to the power MOSFETs.
- reducing circuit board track lengths to a minimum and using twisted pairs for all interconnections.
- for parallelled devices, keeping the devices close to each other and keeping all connections short and symmetrical.
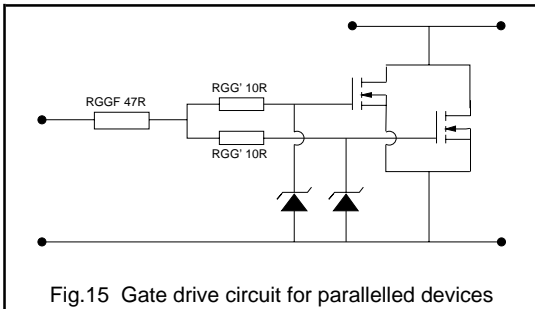
Fig.15 Gate drive circuit for parallelled devices

Modelling of parasitic turn-on

Using the simple MOSFET model of Fig.9 it is possible to study the susceptibility to parasitic turn-on of alternative gate drive circuits. Considering the switching instant when the bottom MOSFET is held off and the top MOSFET is switched on, the voltage across the bottom MOSFET swings from the negative inverter rail to the positive one. The switching transient can be modelled by an imposed dv_{DS}/dt across C_{GD} and C_{GS} and hence the effect of gate circuit design and dv_{DS}/dt on v_{GS} can be studied using simple SPICE models.

Typical data sheet values of C_{GD} and C_{GS} for a 500V MOSFET were used. The simulated results assume constant dv_{DS}/dt, that freewheel diode reverse recovery can be neglected and that the off-state gate drive buffer output is at 0V with a sink impedance of around 5Ω. In practice the dv_{DS}/dt causing parasitic turn-on is not constant and is only at its maximum value for a small proportion of the voltage transition. Thus the results shows here represent a 'worst-case' condition for the alternative gate drive circuits used to clamp v_{GS} to below its threshold value, typically 2V to 3V. (The simple circuit model used here ceases to become valid once v_{GS} reaches $v_{GS(TO)}$ (time t_1 in Fig.10) when the MOSFET starts to turn on.)

Fig.17 shows the relevant waveforms for the circuit of Fig.9 with R_{GG}=100Ω. The top waveform in Fig.17 shows an imposed dv_{DS}/dt of 3.5V/ns and a dc link voltage of 330V. The centre trace of Fig.17 shows that v_{GS} rises quickly (reaching 3V in 25ns); at this point the MOSFET would start to turn on. The bottom trace shows the C_{GD} charging current sinking through the gate drive resistor R_{GG}. For the circuit of Fig.12 with R_{GGF}=100Ω and R_{GGR}=10Ω, Fig.18 shows that the gate source voltage is held down by the reduced drive impedance but still reaches 3V after 35ns.
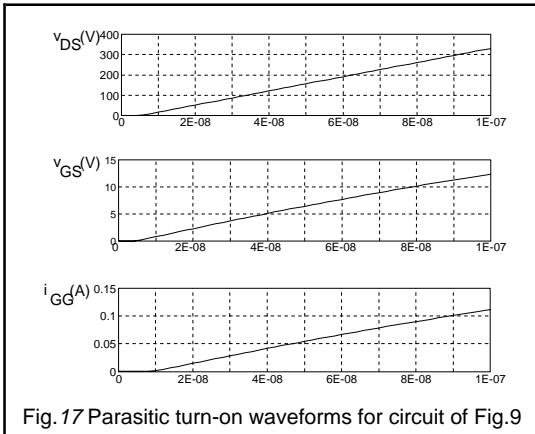
Fig.*17* Parasitic turn-on waveforms for circuit of Fig.9
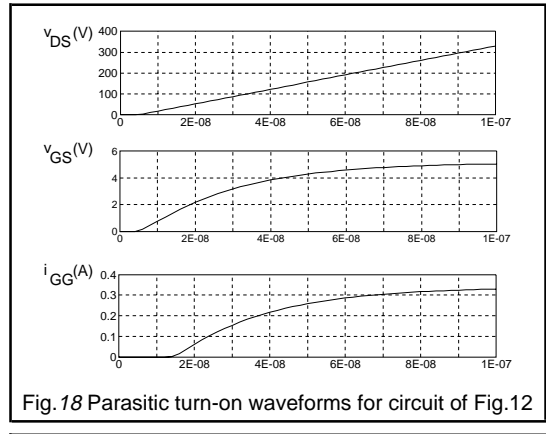
Fig.*18* Parasitic turn-on waveforms for circuit of Fig.12
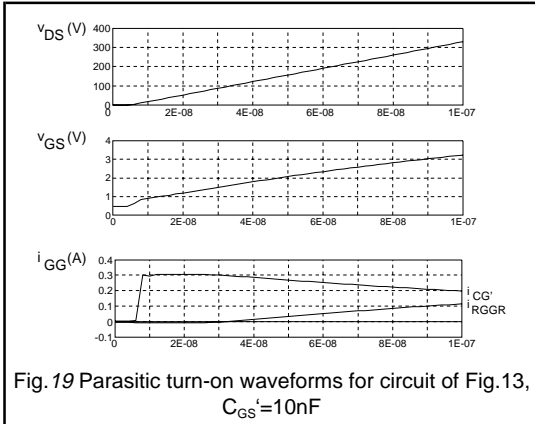
Fig.*19* Parasitic turn-on waveforms for circuit of Fig.13,
C_{GS}'=10nF
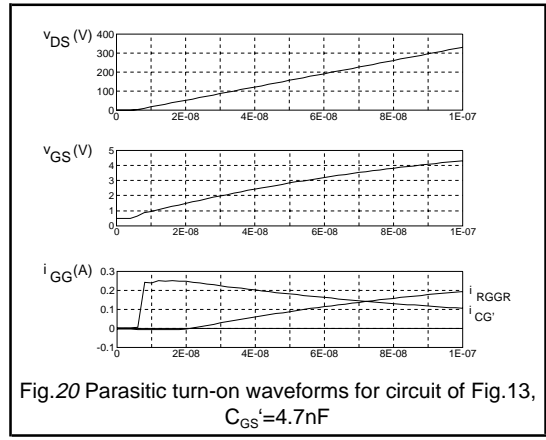
Fig.*20* Parasitic turn-on waveforms for circuit of Fig.13,
C_{GS}'=4.7nF
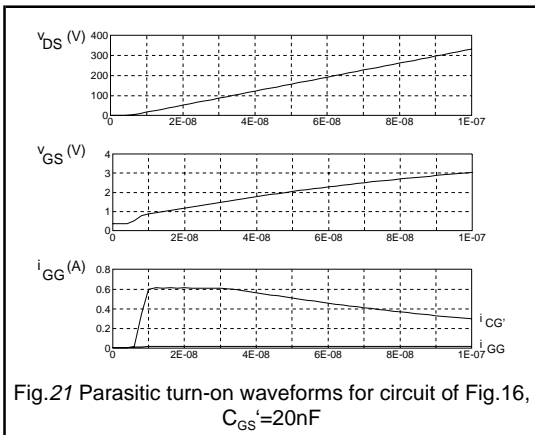
Fig.*21* Parasitic turn-on waveforms for circuit of Fig.16,
C_{GS}'=20nF
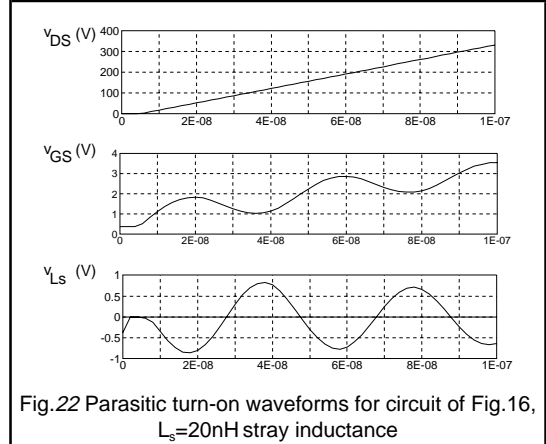
Fig.*22* Parasitic turn-on waveforms for circuit of Fig.16,
L_s=20nH stray inductance

Figure 19 shows the response of the circuit of Figure 13 with $C_{GS}'=10nF$. Here the gate-source voltage is held down during the parasitic turn-on period and so the MOSFET stays off. If the value of C_{GS}' is reduced to 4.7nF then the results given in Fig.20 show that v_{GS} reaches 3V after 55ns thus reducing immunity to parasitic turn-on.

Figures 21 and 22 show the conditions for parallel connected MOSFETs using the circuit of Fig.16. In Fig.21, for $R_{GG1}=47\Omega$, $R_{GG}'=10\Omega$ and $C_{GS}'=20nF$, the bottom trace in the figure shows that a potential parasitic turn-on condition is avoided and v_{GS} is held below its threshold value. The bottom trace in Fig.21 shows most of the parasitic turn-on current is taken by C_{GS}'. Figure 22 shows the effect of stray inductance between the gate drive circuit and the PowerMOS device. The circuit of Fig.16 has been modified by the addition of 20nH of stray inductance between the gate node and the dv/dt clamping network. During switching of the top device with dv/dt=3.5V/ns the stray inductance develops over 0.6V due to coupling via C_{GD}. Clearly this could significantly affect the performance of the drive during normal turn-on, and increase the prospect of the bottom MOSFET being subject to parasitic turn-on problems.

These results show that immunity to parasitic turn-on can be greatly improved by alternative gate circuit design. The SPICE modelled circuits show the worst case conditions of constant dv_{DS}/dt and show that v_{GS} can be held below its threshold voltage using the circuits shown in the previous section. Experimental measurements have confirmed these results in a prototype 20kHz ACMC system.

Device losses in ACMC inverters

It is important to be able to calculate the losses which occur in the switching devices in order to ensure that device operating temperatures remain within safe limits. Cooling arrangements for the MOSFETs or FREDFETs in an ACMC system will depend on maximum allowable operating temperatures, ambient temperature and operating conditions for the system. The components of loss can be examined in more detail:

MOSFET Conduction losses

When a MOSFET or FREDFET is on and carrying load current from drain to source then the conduction 'i²R' loss can be calculated. It is important to note that the device current is not the same as the output current, as demonstrated by the waveforms of Fig.23. The figure shows a sinusoidal motor load current waveform and the top and bottom MOSFET currents. The envelopes of the MOSFET

currents are half sinusoids; however the actual device currents are interrupted by the instants when the load current flows through the freewheel diodes. For the purposes of calculating MOSFET conduction losses it is acceptable to neglect the 'gaps' which occur when the freewheel diodes are conducting for the following reasons:
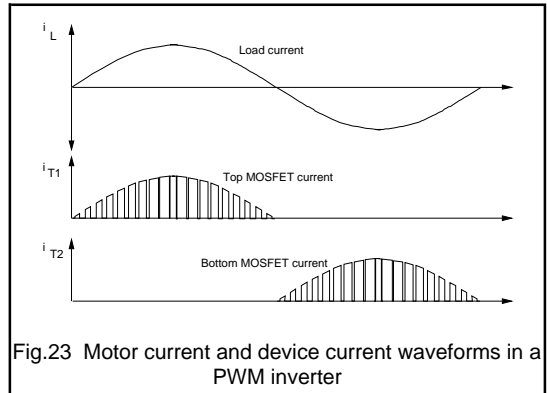
Fig.23 Motor current and device current waveforms in a PWM inverter

-When the motor load current is near its maximum value the switching duty cycle is also near its maximum and so the proportion of time when the diode conducts is quite small and can be neglected.
-When the motor load current is near zero then the switching duty cycle is low but the MOSFET is only conducting small amounts of current. As the MOSFET current is low then the contribution to total conduction loss is small.

Thus if the MOSFET is assumed to be conducting load current for the whole half-period then the conduction losses can be calculated using the current envelope of Fig.23. These losses will be overestimated but the discrepancy will be small. The conduction losses can be given by:

$$P_{M(ON)} = I_T^2.R_{DS(ON)}(T_j) \tag{13}$$

where I_T is the rms value of the half sinusoid MOSFET current envelope.

and: $\quad R_{DS(ON)}(T_j) = R_{DS(ON)}(25°C).e^{k(T_j-25)} \tag{14}$

where k=0.007 for a 500V MOSFET, and k=0.006 for a 500V FREDFET.

I_T is related to the rms motor current, I_L, by:

$$I_T = \frac{I_{max}}{2} = \frac{I_L}{\sqrt{2}} \tag{15}$$

PHILIPS 500V FREDFETS

Frequency = 5kHz

PHILIPS 500V MOSFETS (+ diode network)

Frequency = 5kHz

PHILIPS 500V FREDFETS

Frequency = 20kHz

PHILIPS 500V MOSFETS (+ diode network)

Frequency = 20kHz

Fig.24 Selection graphs for a 1.7A motor

NB. Device selection notation: 1X655-A denotes a single BUK655-500A FREDFET, etc.
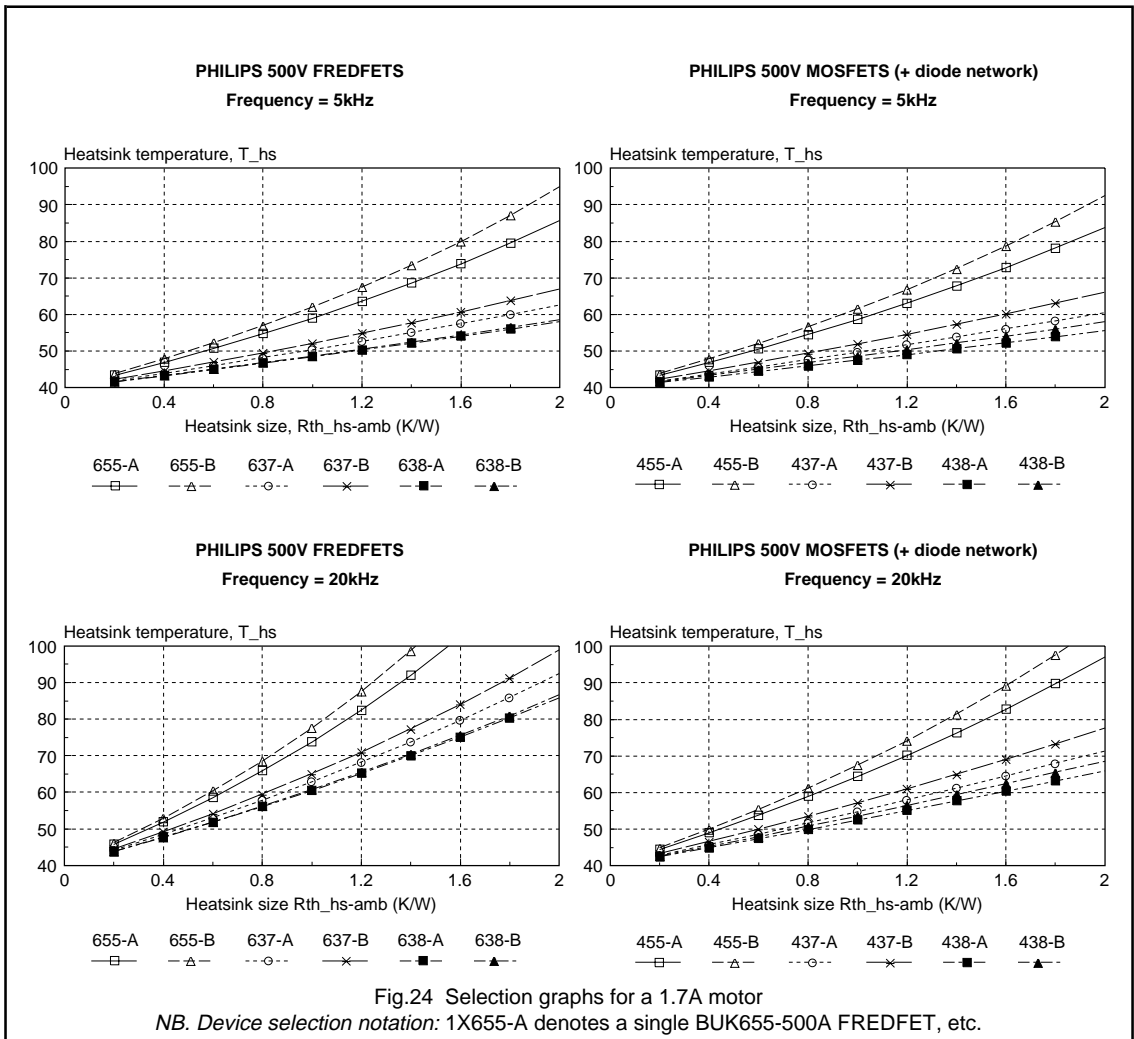
Additionally in a MOSFET inverter the series blocking Schottky diode (D3 of Fig.8) has conduction losses. The current in this diode is the main MOSFET current and so its loss is approximated by:

$$P_{Sch(ON)} = V_f(T_j).I_T \qquad (16)$$

Diode conduction losses

In a MOSFET inverter the freewheel diode losses occur in a discrete device (D2 of Fig.8) although this device is often mounted on the same heatsink as the main switching device. In a FREDFET circuit the diode losses occur in the main device package. The freewheeling diode carries the 'gaps' of current shown in Fig.23 during the periods when its complimentary MOSFET is off. Following the argument used above the diode conduction loss is small and can be neglected. Using this simplification we have effectively transferred the diode conduction loss and included it in the figure for MOSFET conduction loss.

MOSFET switching losses

During the half-cycle of MOSFET conduction the load current switched at each instant is different (Fig.23). The amount of current switched will also depend on the reverse recovery of the bridge leg diodes and hence on the

PHILIPS 500V FREDFETS
Frequency = 5kHz

Heatsink temperature, T_hs

655-A   655-B   637-A   637-B   638-A   638-B

PHILIPS 500V MOSFETS (+ diode network)
Frequency = 5kHz

Heatsink temperature, T_hs

455-A   455-B   437-A   437-B   438-A   438-B

PHILIPS 500V FREDFETS
Frequency = 20kHz

Heatsink temperature, T_hs

655-A   655-B   637-A   637-B   638-A   638-B

PHILIPS 500V MOSFETS (+ diode network)
Frequency = 20kHz

Heatsink temperature, T_hs

455-A   455-B   437-A   437-B   438-A   438-B

Fig.25 Selection graphs for a 3.4A motor
NB. Device selection notation: 1X655-A denotes a single BUK655-500A FREDFET, etc.

temperature of the devices. The total turn-on loss ($P_{M(SW)}$) will be a summation of the losses at each switching instant:

$$P_{M(SW)} = \sum_{n=0}^{\infty} f(T_j, I_n) \qquad (17)$$

MOSFET turn-off times are usually only limited by dv/dt considerations and hence are as short as possible. The turn-off loss of the MOSFETs or FREDFETs in an inverter is small compared with the turn-on loss and can usually be neglected.

Diode switching losses

Diode turn-off loss ($P_{D(SW)}$) is calculated in a similar manner

to the MOSFET turn-on loss. The factors which affect the diode turn-off waveforms have been discussed earlier. Diode turn-on loss is usually small since the diode will not conduct current unless forward biassed. Thus at turn-on the diode is never simultaneously supporting a high voltage and carrying current.

Gate drive losses

Some loss will occur in the gate drive circuit of a PowerMOS device. As the gate drive is only delivering short pulses of current during the switching instants then these losses are negligibly small.

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PHILIPS 500V FREDFETS
Frequency = 5kHz

PHILIPS 500V MOSFETS (+ diode network)
Frequency = 5kHz

PHILIPS 500V FREDFETS
Frequency = 20kHz

PHILIPS 500V MOSFETS (+ diode network)
Frequency = 20kHz

Fig.26 Selection graphs for a 6.8A motor
NB. Device selection notation: 1X638-A denotes a single BUK638-500A FREDFET, etc.
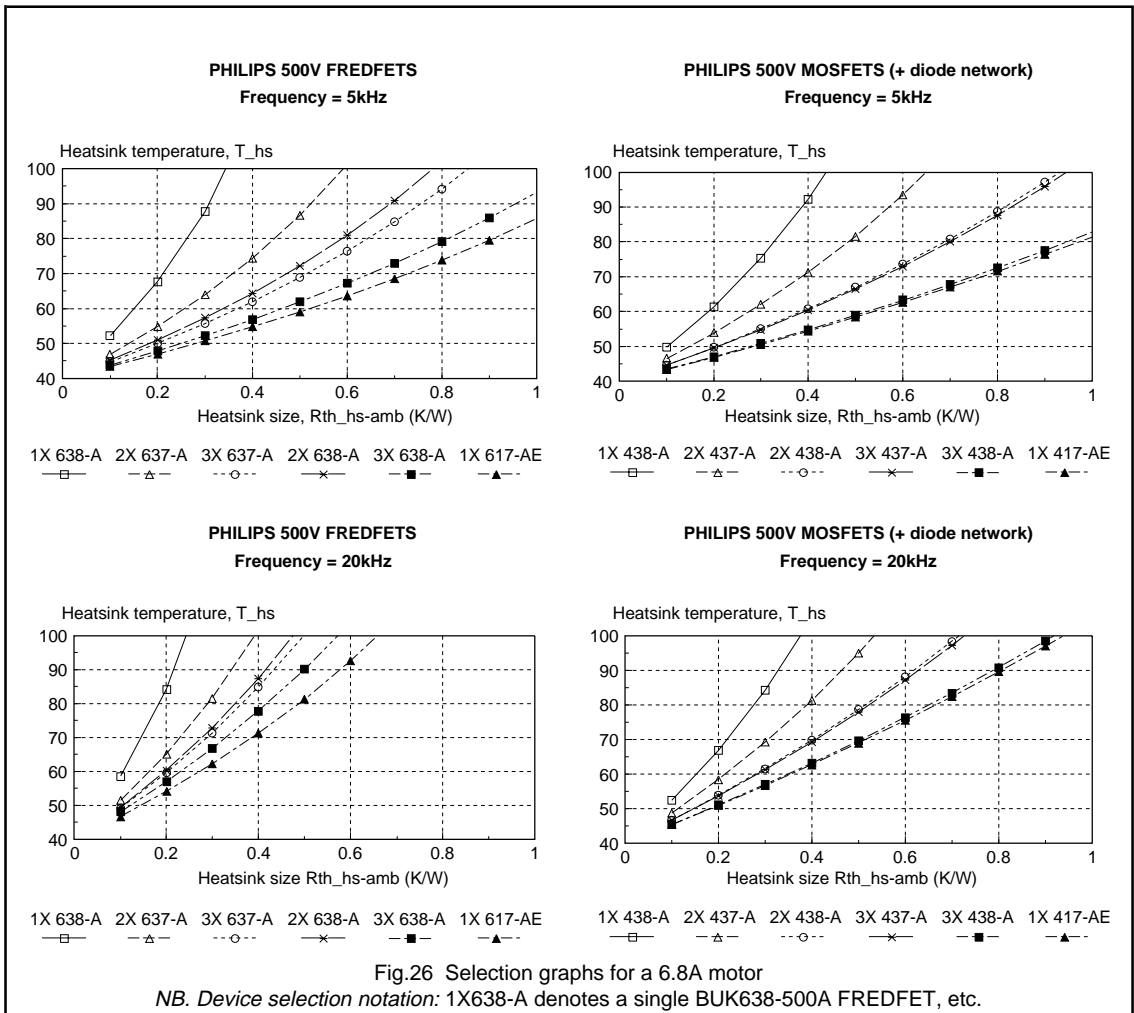
System operating temperatures

In this section the device losses discussed in the previous section are calculated and used to produce a design guide for the correct selection of Philips PowerMOS devices and appropriate heatsink arrangements for ACMC applications. The following factors must be take into account when calculating the total system loss, P_{LOSS}:

- Device characteristics
- Switching frequency
- Operating temperature
- Load current
- Number of devices used in parallel.
- Additional snubber or di/dt limiting networks.

$$P_{LOSS} = P_{M(ON)} + P_{M(SW)} + P_{D(SW)} + P_{Sch(ON)} \qquad (18)$$

For the results presented here the device parameters were taken for the Philips range of 500V MOSFETs and FREDFETs. The on-state losses can be calculated from the equations given above. For this analysis the device switching losses were measured experimentally as functions of device temperature and load current. As there are six sets of devices in an ACMC inverter then the total heatsink requirement can be found from:

$$T_{hs} = T_{ahs} + 6 . P_{LOSS} . R_{th(hs-ahs)} \qquad (19)$$

$$T_j = T_{hs} + P_{LOSS} . R_{th(j-hs)} \qquad (20)$$

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PHILIPS 500V FREDFETS
Frequency = 5kHz

PHILIPS 500V MOSFETS (+ diode network)
Frequency = 5kHz

PHILIPS 500V FREDFETS
Frequency = 20kHz

PHILIPS 500V MOSFETS (+ diode network)
Frequency = 20kHz

Fig.27 Selection graphs for a 10A motor
NB. Device selection notation: 2X638-A denotes two parallelled BUK638-500A FREDFETs, etc.
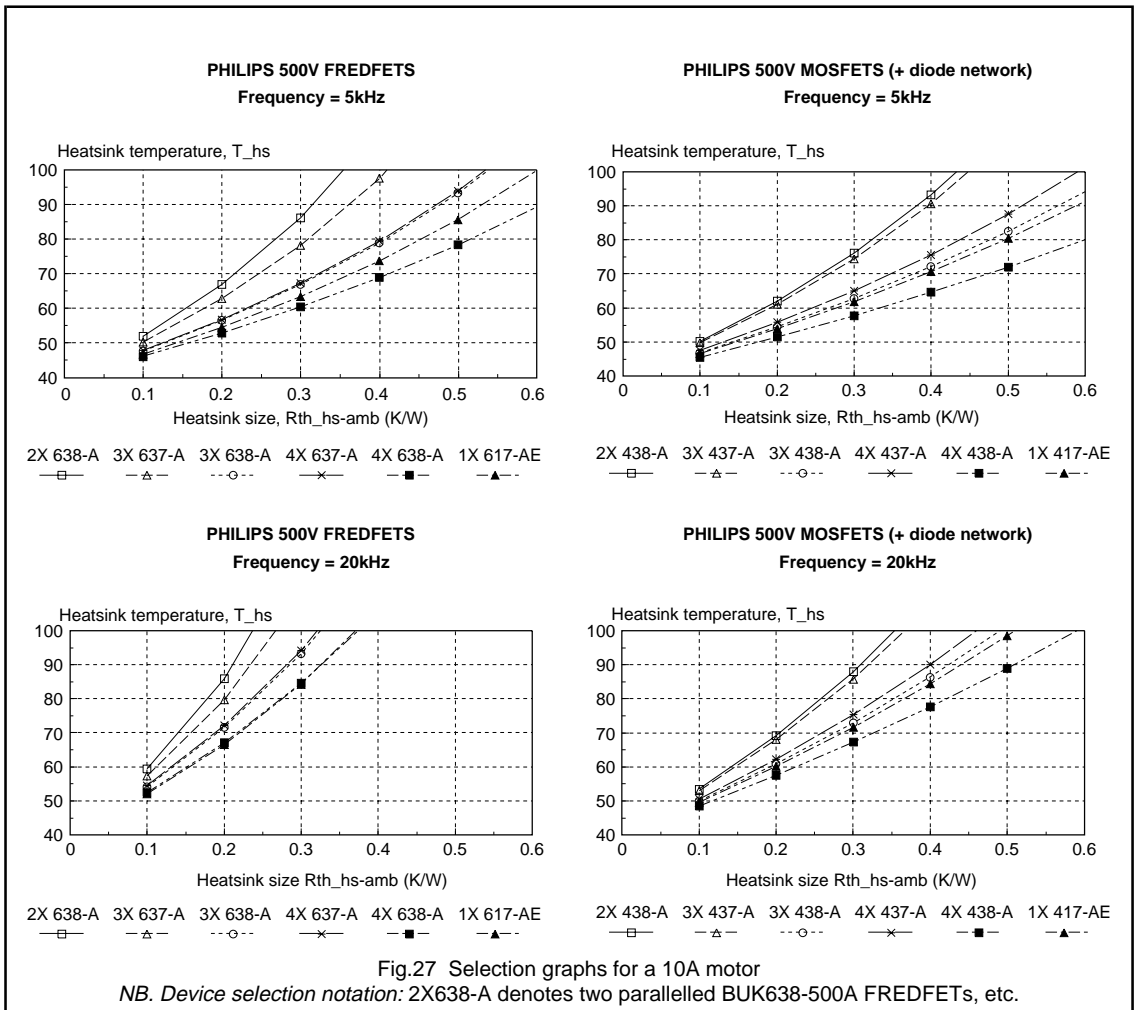
Equations 18 to 20 can be used to find the heatsink size ($R_{th(hs-ahs)}$) required for a particular application which will keep the heatsink temperature (T_{hs}) within a required design value. Results are plotted in Figures 24 to 27 for motor currents of I_L = 1.7A, 3.4A, 6.8A and 10.0A. These currents correspond to the ratings of several standard induction motor sizes. The results assume unsnubbed devices, an ambient temperature of T_{ahs}=40˚C, and are plotted for inverter switching frequencies of 5kHz and 20kHz.

Two examples showing how these results may be used are given below:

1) -The first selection graph in Fig.24 shows the possible device selections for 500V FREDFETs in a 5kHz ACMC

system where the full load RMS motor current is 1.7A. Using a BUK655-500A FREDFET, T_{hs} can be maintained below 70˚C with a total heatsink requirement of 1.2K/W (if each FREDFET was mounted on a separate heatsink then each device would need a 7.2K/W heatsink). The same heatsinking arrangement will give T_{hs}=50˚C using a BUK638-500A. Alternatively T_{hs} can be maintained below 70˚C using a 2K/W heatsink (12K/W per device) and the BUK637-500B.

2) -In Fig.27 the selection graphs for a 10A system are given. The fourth selection graph is for a 20kHz switching frequency using 500V MOSFETs. Here two BUK438-500A devices connected in parallel for each switch will require a total heatsink size of 0.3K/W if the

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heatsink temperature is to remain below 90°C. The same temperature can be maintained using a 0.5K/W heatsink and a single BUK417-500AE ISOTOP device.

For different motor currents or alternative PWM switching frequencies the appropriate device and heatsink arrangement for a particular application can be found by interpolating the results presented here.

Conclusions

This section has outlined the basic principles and operation of PWM inverters for ACMC applications using Philips PowerMOS devices. MOSFETs and FREDFETs are the most suitable devices for ACMC systems, especially at high switching speeds. This section has been concerned with systems rated up to 2.2kW operating from a single phase supply and has shown that there is a range of Philips PowerMOS devices ideally suited for these systems.

The characteristics and performance of MOSFETs and FREDFETs in inverter circuits and the effect of gate drive design on their switching performance has been discussed. The possibility of parasitic turn-on of MOSFETs in an inverter bridge leg can be avoided by appropriate gate drive circuit design. Experimental and simulated results have

shown that good switching performance and immunity to parasitic turn-on can be achieved using the Philips range of PowerMOS devices in ACMC applications . Using the device selection graphs presented here the correct MOSFET or FREDFET for a particular application can be chosen. This guide can be used to select the heatsink size and device according to the required motor current, switching frequency and operating temperature.

References

1. Introduction to PWM speed control system for 3-phase AC motors: J.A.Houldsworth, W.B.Rosink: Electronic Components and Applications, Vol 2, No 2, 1980.

2. A new high-quality PWM AC drive: D.A.Grant, J.A.Houldsworth, K.N.Lower: IEEE Transactions, Vol IA-19, No 2, 1983.

3. Variable speed induction motor with integral ultrasonic PWM inverter: J.E.Gilliam, J.A.Houldsworth, L.Hadley: IEEE Conference, APEC, 1988, pp92-96.

4. MOSFETs and FREDFETs in motor drive equipment: Chapter 3.1.3.

3.1.5 A 300V, 40A High Frequency Inverter Pole Using Paralleled FREDFET Modules

Introduction

Voltage source inverters which are switched using some form of pulse width modulation are now the standard in low to medium rated AC and brushless DC variable speed drives. At present, because of device limitations the switching (modulation) frequencies used in all but the lowest drive ratings are restricted to a few kHz. There is however a strong technical advantage in using much higher ultrasonic switching frequencies in excess of 20 kHz, the benefits of which include:

i) The low frequency distortion components in the inverter output waveform are negligible. As a result there is no longer a need to derate the electrical machine in the drive as a consequence of harmonic loss.

ii) The supply derived acoustic noise is eliminated.

iii) The DC link filter component values are reduced.

The device best suited for high switching frequencies is the power MOSFET because of its extremely fast switching time and the absence of secondary breakdown. However, being surface conduction devices, high power rated MOSFETs are difficult and expensive to manufacture and at present single MOSFETs are only suitable for inverter ratings of typically 1-2 kVA per pole. Although higher rated power devices such as bipolar transistors and IGBTs can be switched at medium to high frequencies, the switching losses in these circuits are such that frequencies in excess of 20 kHz are at present difficult to achieve.

Switches with high ratings and fast switching times can be constructed by hard paralleling several lower rated power devices. MOSFETs are particularly suitable because the positive temperature coefficient of the channel resistance tends to enforce good steady-state current sharing between parallel devices. However to achieve good dynamic current sharing during switching, considerable care must be taken in the geometric layout of the paralleled devices on the common heatsink. In addition, the device characteristics may need to be closely matched. As a result modules of paralleled MOSFETs are often expensive.

Within each mdule: Good transient + steady state load sharing
                        Isolated drive circuit

Fig.1
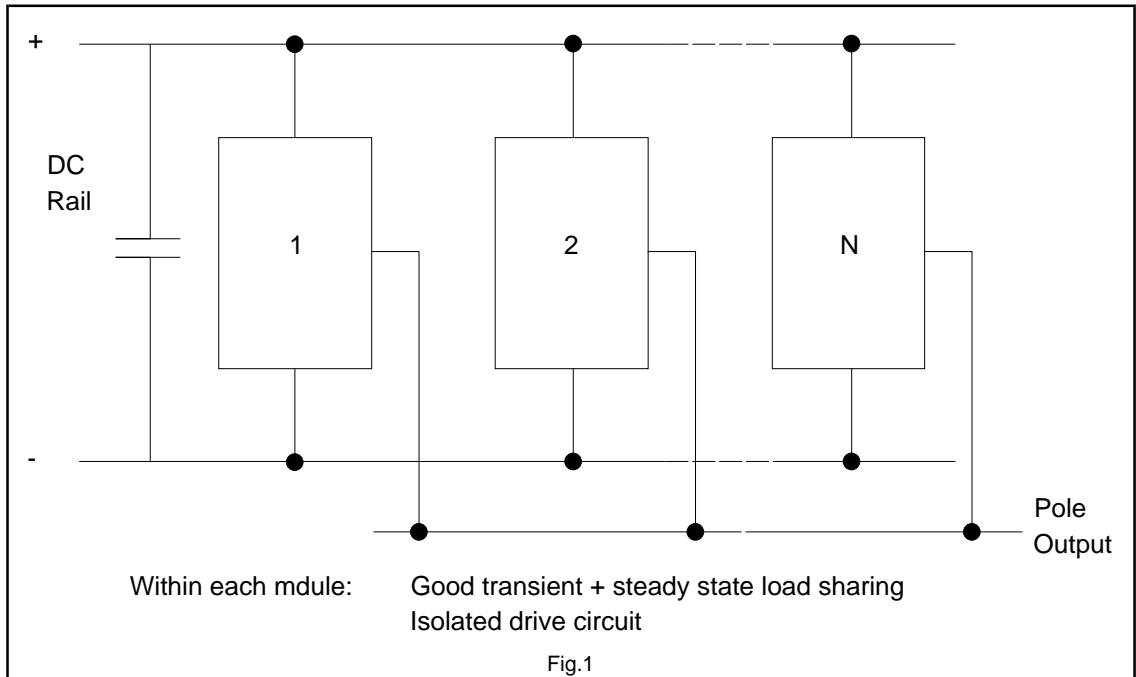
An alternative approach to paralleling is to use small switching aid networks which overcome the constraints of hard paralleling by improving the dynamic load sharing of the individual devices. It is possible to envisage an inverter design where each pole consists of a number of identical pole modules which share a common supply and have outputs connected in parallel, as shown in Fig.1. Each module is designed to operate individually as an inverter pole and contains two power MOSFETs with associated isolated gate drive circuitry. When the modules are connected in parallel their design is such that they will exhibit good transient and steady-state load sharing, the only requirement being that they are mounted on a common heatsink. In this manner any inverter volt-amp rating can be accommodated by paralleling a sufficient number of pole modules.

Pole module

The power circuit diagram of an individual pole module which is suitable for the second form of paralleling is shown in Fig.2. The design makes use of the integral body diode of the main switching devices and for this purpose the fast recovery characteristics of FREDFETs are particularly suitable. Two snubber circuits and a centre tapped inductance are included in the circuit. These small switching aid networks perform a number of functions in the circuit:
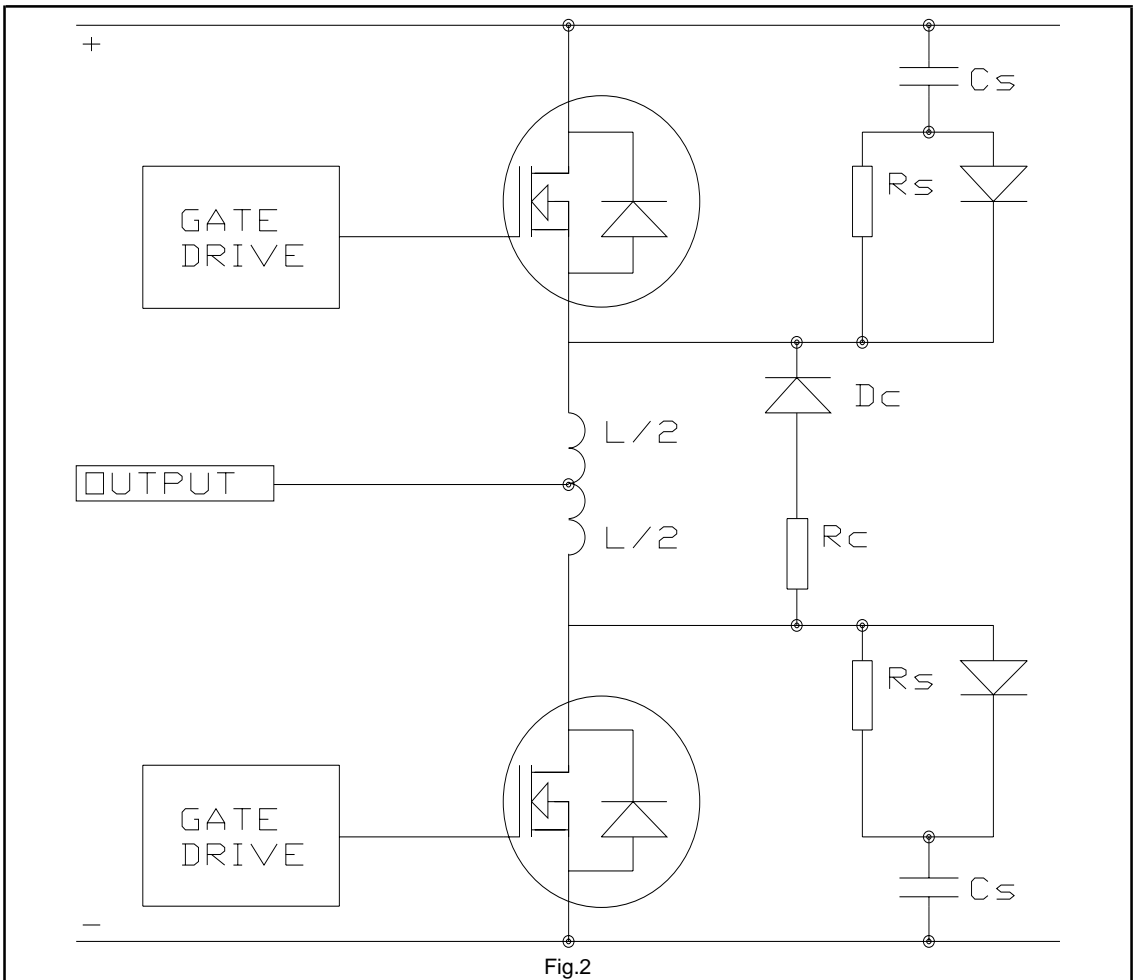
Fig.2

i) They act to improve the dynamic current sharing between the pole modules when connected in parallel.

ii) They ensure safe operation of the MOSFET integral body diode. The central inductance controls the peak reverse current of the diode and the snubber network prevents secondary breakdown of the MOSFET parasitic internal transistor as the integral body diode recovers.

iii) They reduce the switching losses within the main power devices and thus allows maximum use of the available rating.
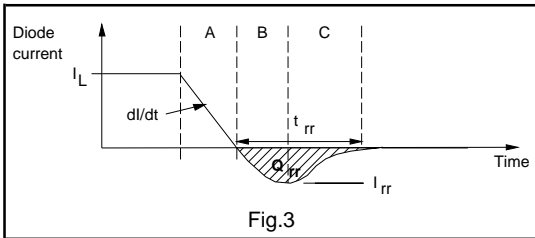
Fig.3

The operation of the circuit is typical of this form of inverter pole. The commutation of the integral body diode will be discussed in detail since it is from this section of the operation that the optimal component values of the switching aid network are determined. The value of the inductor L is chosen to give a minimum energy loss in the circuit and the snubber network is designed to ensure safe recovery of the integral diode at this condition. For example consider the case when there is an inductive load current I_L flowing out of the pole via the integral body diode of the lower MOSFET just prior to the switching of the upper MOSFET. With reference to Fig.3, the subsequent operation is described by the following regions:

Region A: Upper MOSFET is switched on. The current in the lower integral body diode falls at a rate (dI/dt) equal to the DC link voltage V_{DD} divided by the total inductance L of the centre tapped inductance.

Region B: The diode current becomes negative and continues to increase until the junction stored charge has been removed, at which stage the diode recovers corresponding to a peak reverse current I_{RR}.

Region C: The voltage across the lower device increases at a rate (dV/dt) determined by the capacitance C_s of the lower snubber network. The current in the upper MOSFET and the inductor continues to increase and reaches a peak when the voltage across the lower device has risen to the DC link value. At this point the diode D_c becomes forward biased and the stored energy in the inductor begins to discharge through the series resistance R_c.

The energy E_1 gained by the switching aid networks over the above interval is given by:

$$E_1 = \frac{1}{2}I_{RR}^2 L + \frac{1}{2}C_s V_{DD}^2 \qquad (1)$$

and is ultimately dissipated in the network resistors R_s, R_c. For a given forward current, the peak reverse current I_{RR} of the diode will increase with increasing dI/dt and can be approximately represented by a constant stored charge, (Q_{RR}) model, where:

$$I_{RR} = \sqrt{2\left(\frac{dI}{dt}\right)Q_{RR}} \qquad (2)$$

Although in practice I_{RR} will tend to increase at a slightly faster rate than that given by equation (2).

Since in the inverter pole circuit

$$\frac{dI}{dt} = \frac{V_{DD}}{L} \qquad (3)$$

$$I_{RR} = \sqrt{\frac{2V_{DD}Q_{RR}}{L}} \qquad (4)$$

Inspection of equations (1) and (4) shows that the energy loss E_1 remains approximately constant as L is varied.

During the subsequent operation of the inverter pole when the upper MOSFET is turned off and the load current I_L returns to the integral body diode of the lower device, an energy loss E_2 occurs in the inductor and the upper snubber equal to:

$$E_2 = \frac{1}{2}I_L^2 L + \frac{1}{2}C_s V_{DD}^2 \qquad (5)$$

This loss can be seen to reduce with L. However as L is reduced both I_{RR} and the peak current in the upper MOSFET will increase and result in higher switching loss in the diode and higher conduction loss in the channel resistance of the upper device.

The value of L which gives minimum energy loss in the pole occurs when there is an optimal balance between the effects described above. Typical measured dependencies of the total energy loss on the peak reverse diode current as L is varied are shown in Fig.4. The characteristics of a similarly rated conventional MOSFET and a fast recovery FREDFET are compared in the figure. In both cases the minimum energy loss occurs at the value of L which gives a reverse recovery current approximately equal to the design load current. However the loss in the FREDFET circuit is considerably lower than with the conventional device. The optimal value of L can be found from the manufacturers specified value of stored charge using equation (4), where

POWER LOSS (W)

STANDARD
EQUIVALENT
MOSFET

BUK638-500B
MODULE

NORMALISED RECOVERY CURRENT (IRR/IL)

Fig.4
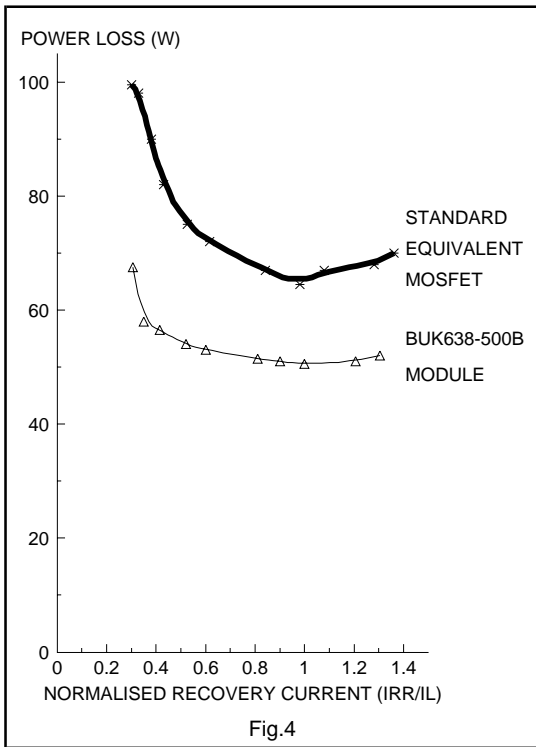
$$L_{opt} = \frac{2V_{DD}Q_{RR}}{I_L^2} \qquad (6)$$

The snubber capacitor value C_s is chosen to limit the dV/dt across the integral body diode as it recovers. Experience has shown that a value of 1V/nS will ensure safe operation, hence:

$$C = (I_L)\,\text{nF} \qquad (7)$$

The resistive component of the switching aid networks are chosen in the usual manner.

Parallel operation of pole modules

The principle behind the 'soft' paralleling adopted here is to simply connect the outputs of the required number of modules together and feed them with a common DC link and control signals. The transient load sharing between the parallel modules will be influenced by the tolerances in the individual inductor and snubber capacitor values and any variations in the switching instances of the power devices, the latter being as a result of differences in device characteristics and tolerances in the gate drive circuitry. These effects were investigated using the SPICE circuit

simulation package. The SPICE representation of the modules is shown in Fig.5, in which the upper MOSFET channel is modelled by an ideal switch with a series resistance R_{DS}. The full SPICE diode model is used for the lower MOSFET integral body diode, however ideal diode representations are sufficient for the devices in the switching aid networks. The load is assumed to act as a constant current sink over the switching interval.

Fig.5
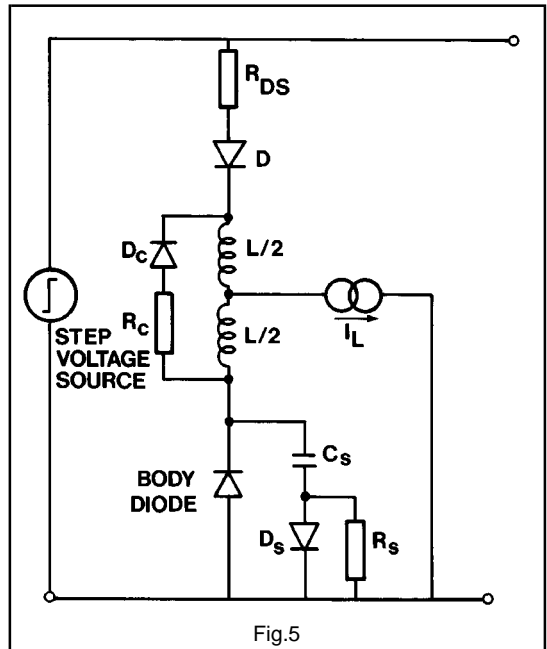
From the SPICE simulation an estimate of the peak transient current imbalance between the MOSFETs of the two modules was obtained for various differences in the inductors, capacitors and device turn-on times. It was found that the transient current sharing was most sensitive to unequal device switching times. An example of the results obtained from a simulation of two paralleled modules using BUK638-500B FREDFETs are shown in Fig.6. With good gate drive design the difference between device switching times is unlikely to exceed 50nS resulting in a peak transient current mismatch of less than 10%. The load sharing would improve if the value of inductor is increased but this has to be traded off against the increase in switching loss. The effect of the tolerance of the inductor values on the load sharing is given for the same module in Fig.7, where it can be seen that a reasonable tolerance of 10% results in only a 7% imbalance in the currents. The load sharing was found to be relatively insensitive to tolerances in the snubber capacitor values.

% MOSFET PEAK CURRENT MISMATCH vs GATE DRIVE DELAY (ns)

Fig.6

% MOSFET PEAK CURRENT MISMATCH

% TOLERANCE OF NOMINAL TOTAL CENTRAL INDUCTANCE
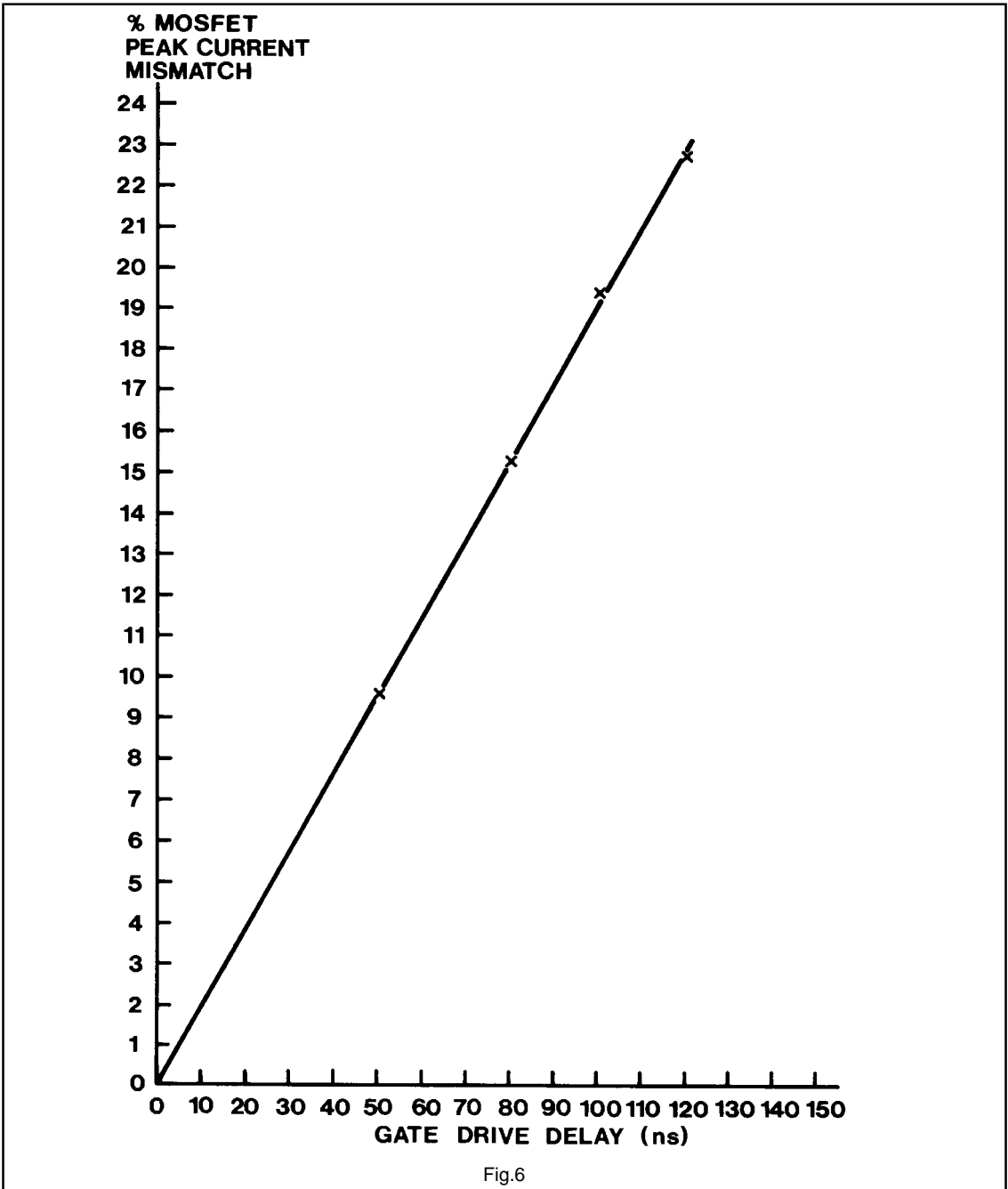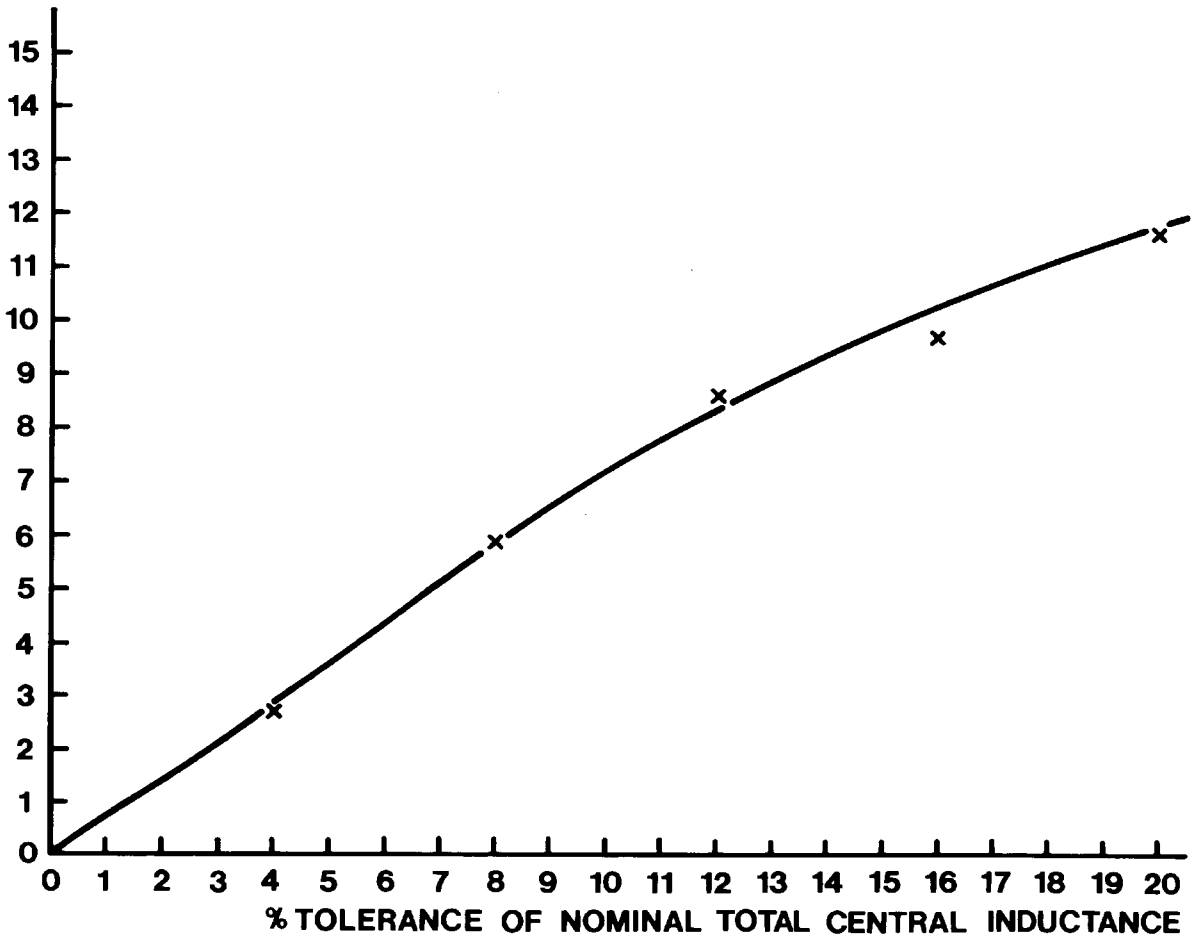
Fig.7

A 300V, 10A pole module design using BUK638-500B FREDFETs

The circuit diagram of a 300V, 10A pole module based on BUK638-500B FREDFETs is given in Fig.8. The inductor value was chosen using the criteria discussed in Section 2.

The conventional R-C snubber network has been replaced by the active circuit shown in Fig.9 and involves the use of a second, low rated BUK455-500B MOSFET which is made to act as a capacitance by invoking the 'Miller' effect. The active snubber is more efficient at low load currents because it tends to maintain a constant (dV/dt) regardless of the load, and thus the snubber loss is proportional to the current, as opposed to the conventional circuit in which the loss remains constant. In addition the active circuit is compact and lends itself more readily to a hybrid assembly. The major component costs are the secondary MOSFET and a low voltage power diode and compare favourably with those of the conventional high voltage capacitor and high voltage diode.
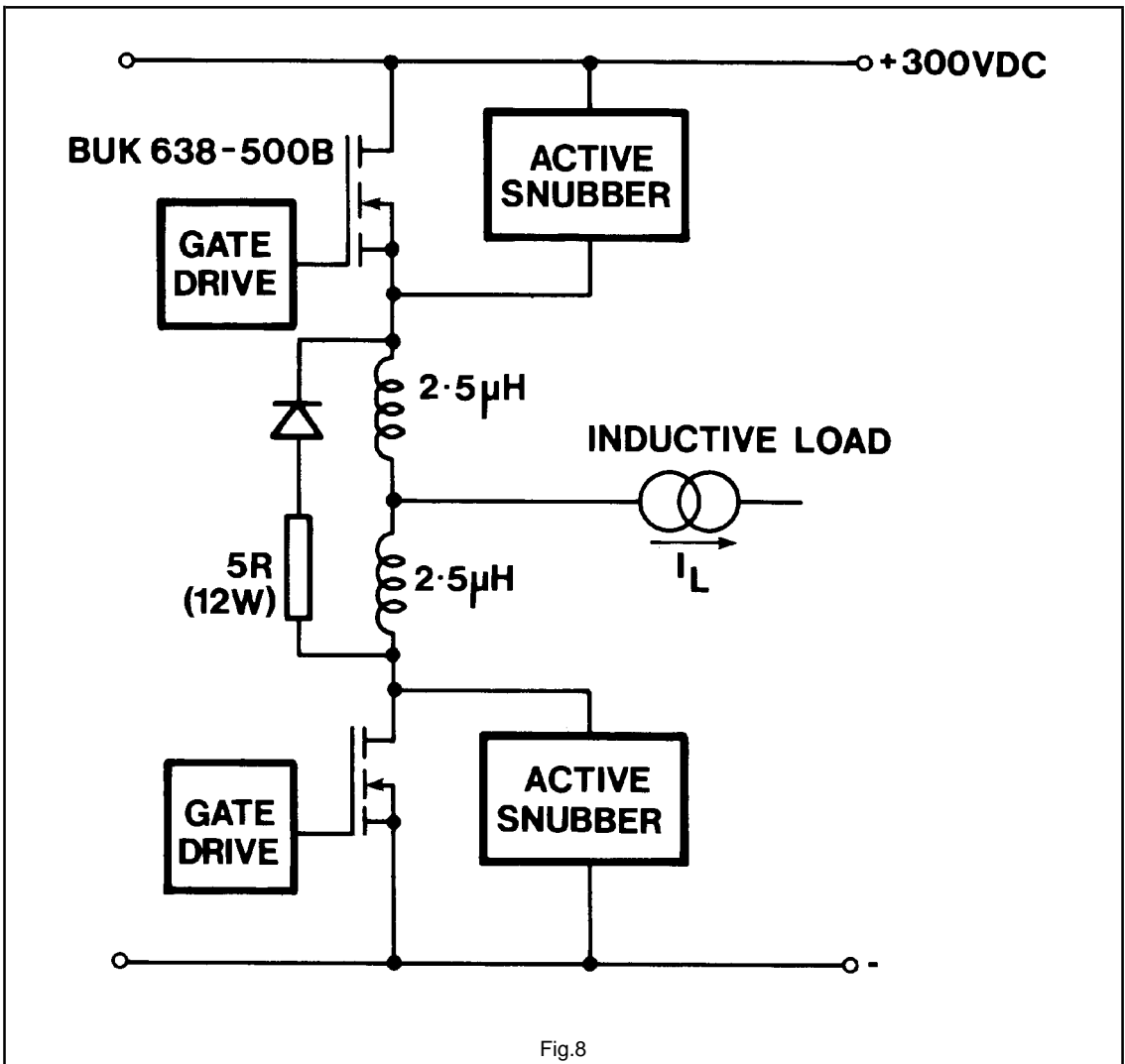
Fig.8

The gate drive circuits are given in Fig.10 and are based upon the pulse transformer configuration described in chapter 1.2.3. A PNP transistor has been added between the gate and source to reduce the drive off-state impedance, to improve the switching and prevent any Miller effect in the main device.
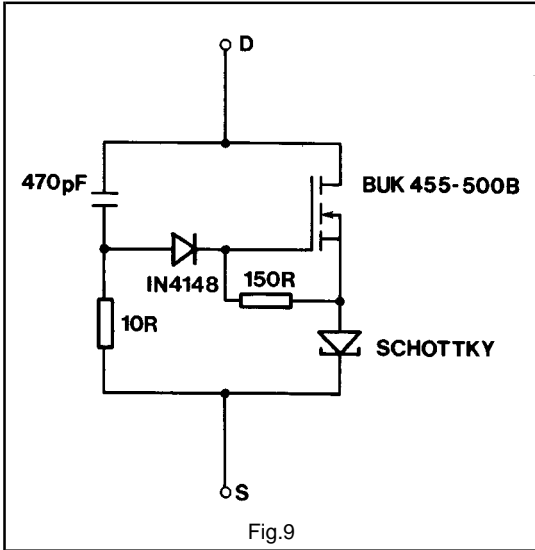
Fig.9

FREDFET module performance

The typical voltage and current waveforms of the upper and lower switching devices are shown in Figures 11 and 12 for the case of a single pole module sourcing the rated current of 10 Amps from a 300V DC link. Fig.12 illustrates how the use of the series inductor and active snubber gives a controlled recovery of the fast integral body diode of the FREDFET.

Fig.10

5 A/div
50 V/div
200 ns/div
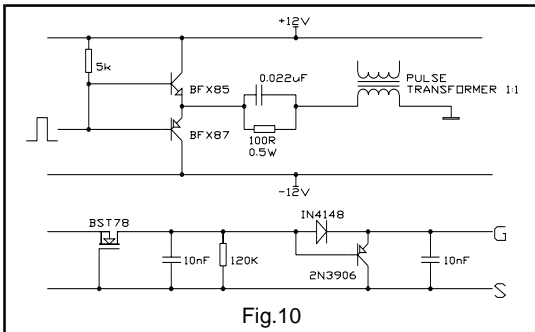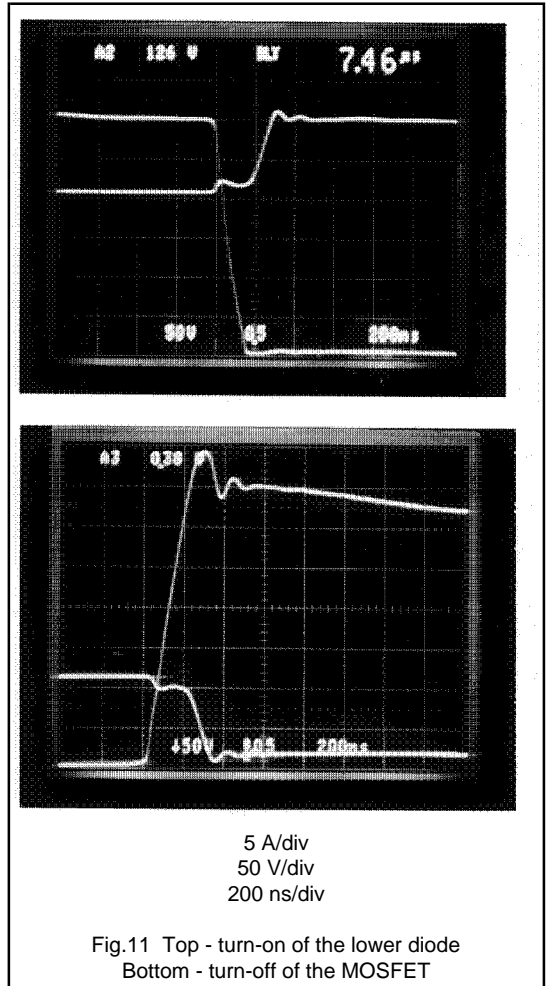
Fig.11 Top - turn-on of the lower diode
Bottom - turn-off of the MOSFET

The losses of an individual module switched at 20 kHz are plotted in Fig.13 as a function of output current. They mainly stem from conduction loss, the switching loss representing only a third of the maximum loss. Because the switching loss occurs mainly in the aid networks the main FREDFETs can be used at close to their full rating. Similarly operation at higher frequencies will not result in a substantial reduction in efficiency, for example at 40 kHz, 10A operation the losses are 95W.
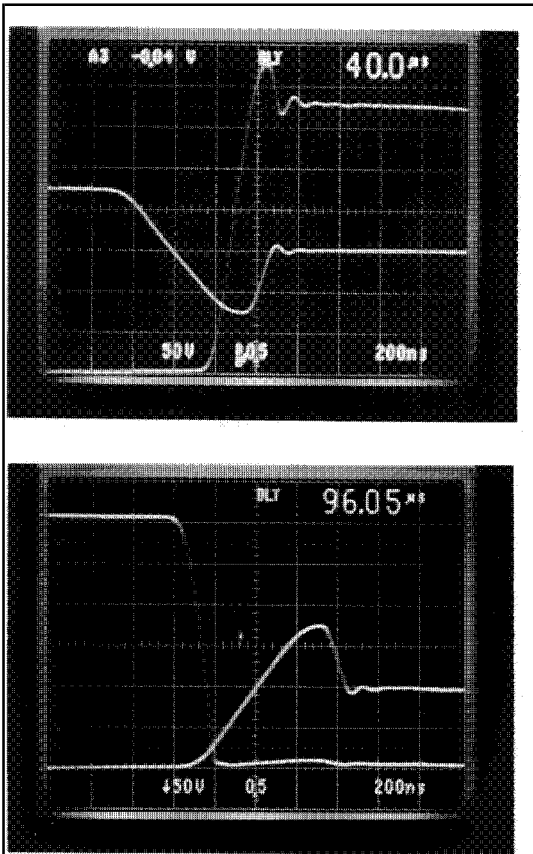
5 A/div
50 V/div
200 ns/div

Fig.12 Top - turn-off of the lower diode
Bottom - turn-on of the MOSFET

LOAD CURRENT (A)
Fig.13

Four modules were connected in parallel and mounted on a common heatsink. The modules operated successfully at 300V with total loads in excess of 40A, four times their individual rating. The common heatsink, which had a thermal resistance to ambient of 0.33°C/W was sufficient to achieve the full 40A, 300V continuous rating of the parallel units at 20 kHz. The current waveforms of the upper FREDFETs in each module are overlaid in Fig.14, where it can be seen that the load sharing is very even, particularly after the initial switching transients.

5 A/div
2 μs/div
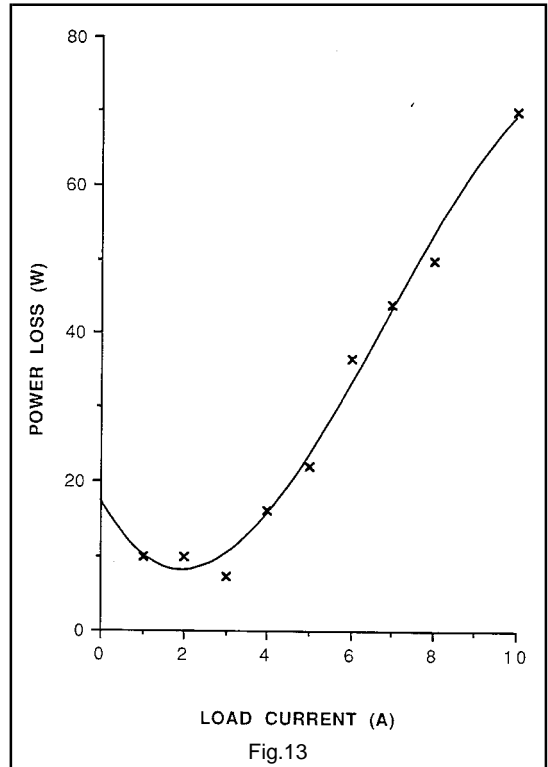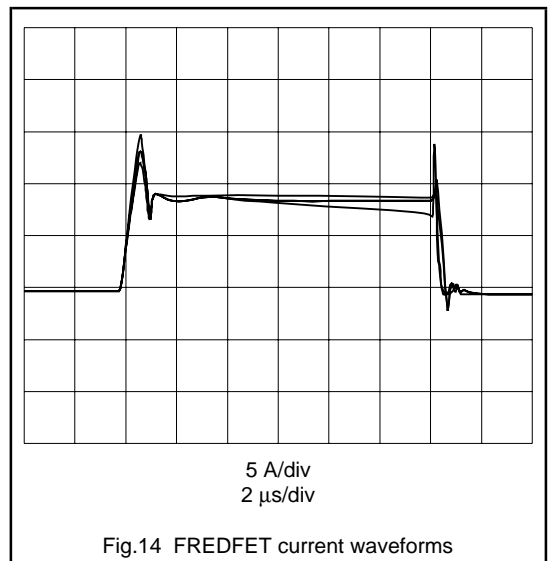
Fig.14 FREDFET current waveforms

Conclusion

Parallel, separate MOSFET pole modules provide a method of designing medium rated inverter poles, which can be switched efficiently at frequencies in excess of 20 kHz. The approach is flexible since a single pole module design can be used to achieve a range of inverter volt-amp ratings by paralleling a sufficient number of units.

Through the use of small switching aid networks it is possible to obtain excellent transient and steady-state current sharing between the paralleled modules. The current sharing remains good even if there are substantial variations in component tolerances and the power device

switching times. The switching aid networks also reduce the switching losses in the main devices and allows them to be used to their full rating.

The presented design of a 300V, 10A module based on BUK638-500B, FREDFETs has a full load loss of only 70W. Four of these modules connected in parallel and mounted on a 0.33°C/W heatsink gave an inverter pole with a 300V, 40A continuous rating when switched at 20 kHz. Excellent current sharing between these modules was observed and as a result there would seem to be no technical reasons why further modules could not be paralleled to achieve even higher ratings.

DC Motor Control

3.2.1 Chopper circuits for DC motor control

DC motor drives are used for many speed and position control systems where their excellent performance, ease of control and high efficiency are desirable characteristics. DC motor speed control can be achieved using switch mode DC-DC chopper circuits. For both mains-fed and battery supplied systems, power MOSFETs and FREDFETs are the ideal switching devices for the converter stage. The Philips range of PowerMOS devices includes devices suitable for most DC-DC converters for motor control applications. Additionally, due to the ease with which MOSFETs and FREDFETs can be paralleled, Philips PowerMOS devices can easily be used in chopper circuits for both low power and high power DC motor drives for vehicle, industrial or domestic applications.

Introduction to DC motor drives

In a DC motor, the static field flux is established using either permanent magnets or a stator field winding. The armature winding, on the rotor of a dc machine, carries the main motor current. The armature winding is a series of coils, each connected to segments of a commutator. In order that the motor develops constant torque as the rotor moves, successive armature coils must be connected to the external dc circuit. This is achieved using a pair of stationary brushes held in contact with the commutator.

The motor torque is produced by the interaction of the field flux and the armature current and is given by:

$$T_e \propto I_a \tag{1}$$

The back emf developed across the armature conductors increases with the motor speed:

$$E_a \propto \omega_m \tag{2}$$

Permanent magnet DC motors are limited in terms of power capability and control capability. For field wound DC motors the field current controls the flux and hence the motor torque and speed constants. The field winding can be connected in series with the armature winding, in shunt with it, or can be separately excited. For the separately excited dc motor, shown in Fig.1 the field flux is controlled and the motor can be made to operate in two distinct modes: constant torque operation up to the rated speed of the motor, and then constant power operation above rated speed, as shown in Fig.2. The steady state operation of the motor is described by:

$$V_a = E_a + R_a . I_a \tag{3}$$

For normal motor operation E_a and I_a are positive and the motor is operating in its 'first quadrant'. The motor is said to be operating in its second quadrant, that is braking or regenerating, by reducing V_a below E_a such that I_a is negative. These two quadrants are shown in Fig.3a). If the polarity of the applied voltage is reversed then motoring and regenerating operation can occur with the direction of rotation reversed. Thus by controlling the armature voltage and current polarities, full four-quadrant operation, as shown in Fig.3b), can be achieved.
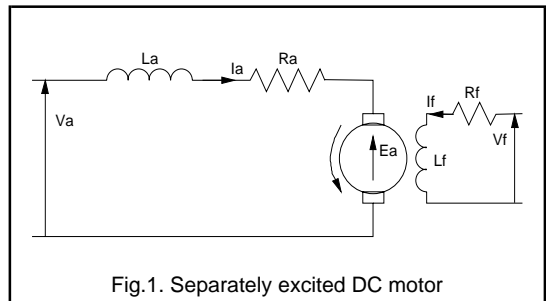
Fig.1. Separately excited DC motor
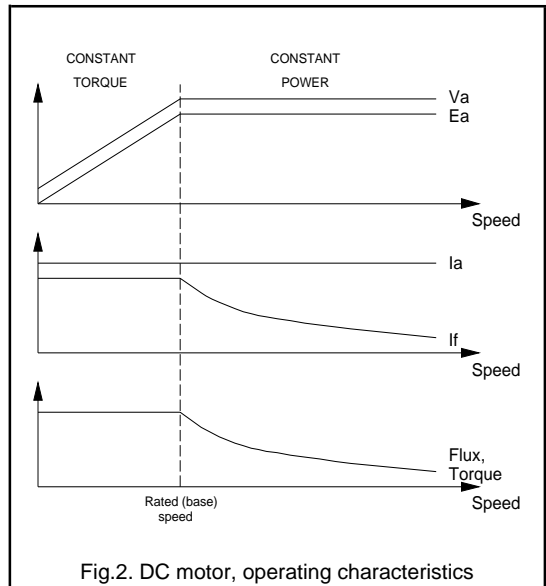
Fig.2. DC motor, operating characteristics

a) Two quadrant operation

b) Four quadrant operation
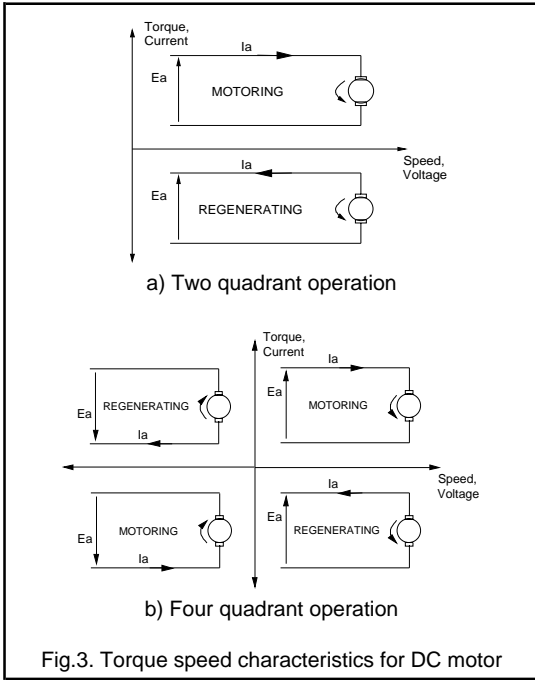
Fig.3. Torque speed characteristics for DC motor
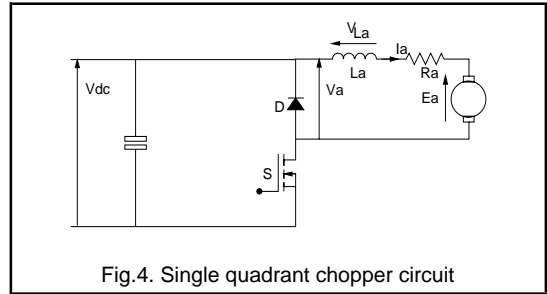
Fig.4. Single quadrant chopper circuit
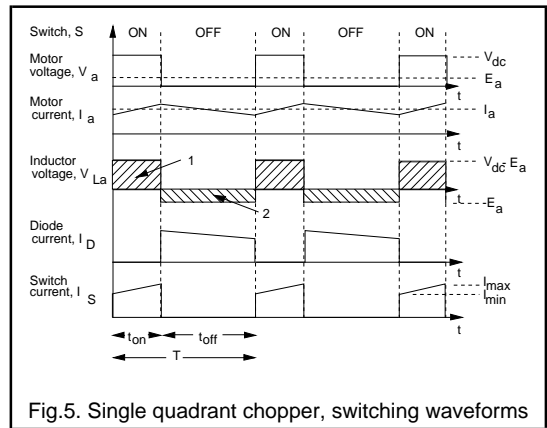
Fig.5. Single quadrant chopper, switching waveforms

Converter topologies for DC motor drives

Single quadrant (step down) converter

For single quadrant operation the chopper circuit of Fig.4 can be used. The average voltage applied to the motor, and hence its speed, is controlled by varying the duty cycle of the switch, S. Fig.5 shows the switching waveforms for the circuit. During the on time, t_{on}, the supply voltage, V_{dc}, is applied to the motor and the armature current starts to increase. Neglecting the on-state resistance of the switch and the armature winding resistance the voltage across the armature inductance is V_{dc}-E_a and so the rate of rise of armature current is given by:

$$\frac{dI_a}{dt} = \frac{V_{dc} - E_a}{L_a} \qquad (4)$$

When the switch turns off the energy stored in the armature inductance must be dissipated. The polarity of the voltage across L_a reverses, the diode D becomes forward biased and the armature current continues to flow. Assuming that the motor speed remains constant and neglecting the forward voltage drop of the freewheeling diode the inductor voltage is equal to -E_a. The rate of fall of armature current is given by:

$$\frac{dI_a}{dt} = -\frac{E_a}{L_a} \qquad (5)$$

If this switching sequence is repeated at some frequency, then the motor voltage can be controlled by altering the relative duration of the on period and off period. Variation of the duty cycle of the switch (t_{on}/T) to control the motor voltage is referred to as Pulse Width Modulation (PWM) control. As the average voltage across the inductor over a period must be zero then:

$$\int_0^T v_L \cdot dt = \int_0^{t_{on}} v_L \cdot dt + \int_{t_{on}}^T v_L \cdot dt = 0 \qquad (6)$$

The integral of inductor voltage for the interval t_{on} corresponds to the shaded area 1 in Fig.5, whilst the integral of inductor voltage for the t_{off} interval corresponds to the shaded area 2 in the Figure. These two areas must be equal and so from equations 4 to 6 or Fig.5 the transfer function of the controller is given by:

$$V_a = \frac{t_{on}}{T} \cdot V_{dc} \qquad (7)$$

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Two quadrant, half-bridge converter

Figure 6 shows a half bridge circuit for two quadrant dc drive. For motoring operation S1 and D2 operate as described above for the single quadrant controller. The freewheel diode D2 may be the internal diode of a MOSFET or FREDFET, or a discrete device. For regenerative operation the DC motor acts as the active power source and the power flow is from right to left in Fig.6. The regenerating current is controlled by varying the duty cycle of S2. When S2 is on, the negative armature current increases through the switch and the armature inductance. When S2 is turned off D1 becomes forward biased and the current regenerates into the supply. The relevant circuit waveforms are shown in Fig.7, showing the equal areas of the inductor volt-seconds over each period of the switching cycle. During regeneration the transfer function of the converter is given by:

$$V_a = \left(1 - \frac{t_{on}}{T}\right).V_{dc} \qquad (8)$$

Fig.6. Two quadrant half bridge chopper circuit

Fig.7. Two quadrant half bridge chopper, switching waveforms
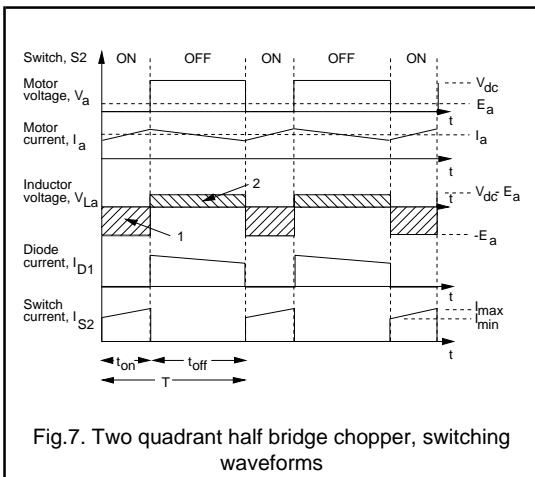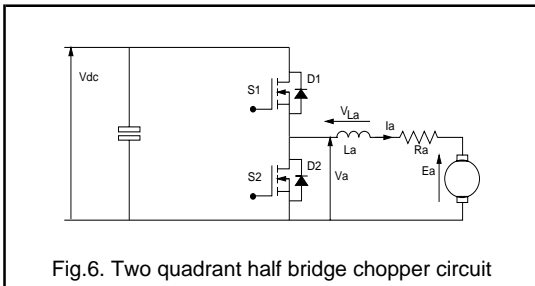
Four quadrant, full-bridge converter

If motoring and regenerating operation are required with both directions of rotation then the full bridge converter of Fig.8 is required. Using this configuration allows the polarity of the applied voltage to be reversed, thus reversing the direction of rotation of the motor. Thus in a full bridge converter the motor current and voltage can be controlled independently. The motor voltage Va is given by:

$$V_a = V_{12} - V_{34} \qquad (9)$$

where V_{12} is controlled by switching S1 and S2 as described above, and V_{34} by switching S3 and S4. The usual operating mode for a full bridge converter is to group the switching devices so that S1 and S3 are always on simultaneously and that S2 and S4 are on simultaneously. This type of control is then referred to as bipolar control.

Fig.8. Four quadrant full bridge circuit
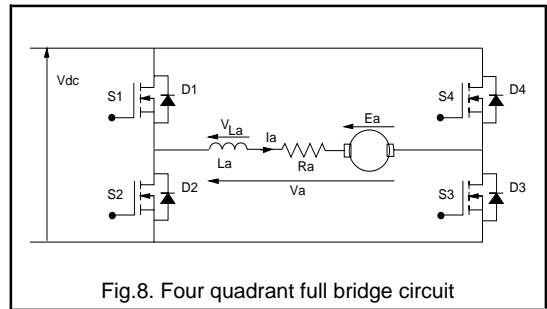
MOSFETs and FREDFETs in bridge circuits

In a bridge circuit, conduction transfers between the switching devices and freewheeling diodes as the load current is controlled (eg. switch S2 and diode D1 in Fig.4). Associated with the transfer of conduction between the freewheel diodes and the switching devices is the reverse recovery of the diode as each conducting MOSFET returns to its on-state. Reverse recovery current flows due to the removal of stored charge from a diode PN junction following conduction. Fig.9 shows the device current paths in a half bridge circuit when conduction is transferred from the top diode to the bottom MOSFET.

The switching waveforms are shown in Fig.10 where the diode reverse recovery current is I_{rr} and the time taken for the reverse recovery currents to be cleared is t_{rr}. The amount of stored charge removed from the body of the diode is represented by the area Q_{rr}. The reverse recovery current flows through the MOSFET which is being turned on in addition to the load current and thus causes additional turn-on losses. The amount of stored charge increases with increasing temperature for a given diode. Both the

magnitude of the reverse recovery current and its duration must be reduced in order to reduce the switching losses of the system.

This effect is important because inherent in the structure of a power MOSFET there is a diode between the source and drain of the device which can act as a freewheeling diode when forward biased. For most DC motor control applications the reverse recovery characteristics of the MOSFET intrinsic diode are acceptable and do not compromise the switching performance of the half bridge circuit. However, the characteristics of a MOSFET intrinsic diode are not optimised for minimum reverse recovery and so, especially in high frequency systems, the FREDFET is more suitable for use in half bridge circuits.
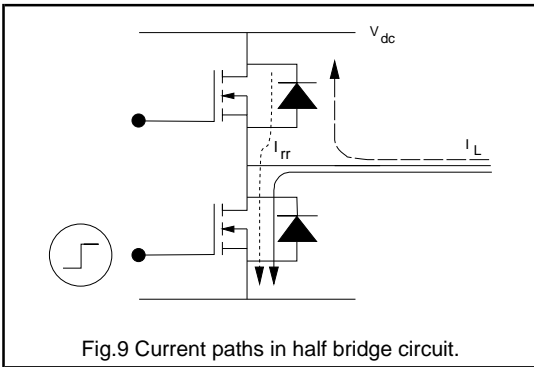
Fig.9 Current paths in half bridge circuit.
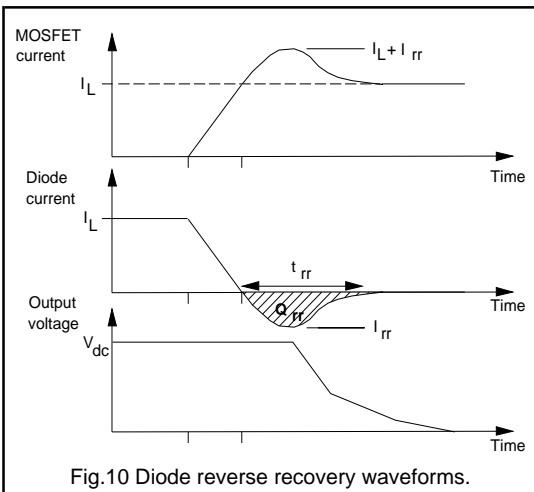
Fig.10 Diode reverse recovery waveforms.

The FREDFET is essentially a MOSFET with a very fast built-in diode where the reverse recovery properties of a FREDFET diode are similar to those of a discrete fast recovery epitaxial diode (FRED). This gives improved switching performance in high frequency applications.

Considerations for converter driven DC motors

Device current rating

The power electronic converter must be matched to the requirements of the motor and the load. DC motor drives can be used to provide torques in excess of the maximum continuous rated torque of the motor for short intervals of time. This is due to the long thermal time constants of the motor. The peak torque requirement of the motor will determine its peak current demand, and hence the peak current requirement for the power switches. The current rating of a PowerMOS device is limited by the maximum junction temperature of the device, which should not be exceeded even for short periods of time due to the short thermal time constant of the devices. The devices must therefore be rated for this peak current condition of the drive. Operation at maximum current usually occurs during acceleration and deceleration periods necessary to meet the performance requirements of DC servo systems.

Device voltage rating

The voltage rating of the power switches will be determined by the power supply DC link voltage and the motor emfs, including those which occur when the motor is operating in its constant power region at above rated speed but below rated torque.

Motor performance

It can be seen from the waveforms of Figures 5 and 7 that the armature current supplied to the motor by the switching converter is not constant. The presence of ripple current in addition to the normal DC current affects the performance of the motor in the following ways:

Torque pulsations. Ripple in the motor current waveform will cause a corresponding ripple in the motor output torque waveform. These torque pulsations may give rise to speed fluctuations unless they are damped out by the inertia of the mechanical system. The torque pulsations occur at high frequencies where they may lead to noise and vibration in the motor laminations and mechanical system.

Losses. Winding losses in a DC motor are proportional to i_{RMS}^2, whereas the torque developed by the motor is proportional to i_{DC}. Ripple in the motor current will increase the RMS current and thus give rise to additional losses and reduce the system efficiency.

Overcurrents. If the ripple current is large then the peak device current will be significantly higher than the design DC value. The devices must then be rated for this higher current. Current ripple will also increase the current which must be handled by the motor brushes possibly increasing arcing at the brush contacts.

The amount of current ripple depends primarily upon the switching frequency and amount of motor inductance (See equations 4 and 5). Increasing L_a and f_s will both reduce the amount of current ripple. The motor inductance is fixed by the motor selection but can be increased by the addition of a discrete component. Increasing the switching frequency of the system will reduce the amount of current ripple but will increase the switching losses in the power devices.

Using PowerMOS devices in DC drives

For many applications the motor control system is operated at switching speeds in the range 1kHz to 20kHz. PowerMOS devices are ideally suited for this type of converter giving the following advantages:

Switching performance

Unlike bipolar devices the MOSFET is a majority carrier device and so no minority carriers must be moved in and out of the device as it turns on and off. This gives the fast switching performance of MOSFET devices. However, at higher switching speeds the switching losses of the system become important and must be considered in addition to the device on-state losses. The device conduction loss depends on the MOSFET on-state resistance, RDS(ON), which increases with the temperature of the device. Switching times are essentially independent of device temperature. PowerMOS devices have good overload capability and Safe Operating ARea (SOAR) which makes them easy to us in a chopper circuit, although the need for snubber circuits will depend on the system operating and performance requirements.
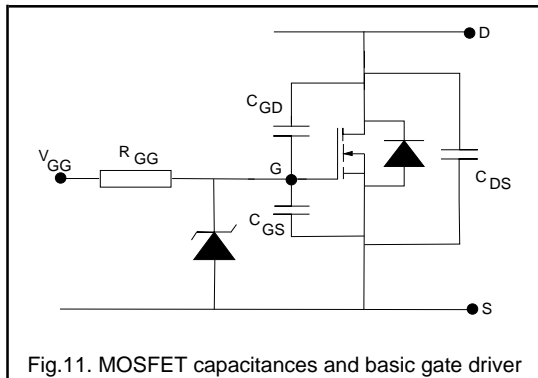
Fig.11. MOSFET capacitances and basic gate driver

Ease of use

PowerMOS devices are essentially voltage driven switches and so the gate drive circuits required to switch the devices are usually relatively simple low power circuits. It is only during switching instants that the gate drive is that required provide current in order to charge and discharge the device capacitances (shown in Fig.11) and thus switch the device. In order to switch the device quickly the gate driver must be able to rapidly sink and source currents of up to 1A. For the simplest gate drive circuit the MOSFET can be switched using a resistive drive and some gate-source overvoltage protection, as shown in Fig.11. Alternative MOSFET gate drive circuits are discussed more fully elsewhere in this handbook.

Parallelling of PowerMOS devices

It is usually straightforward to operate PowerMOS devices in parallel to achieve higher system currents than can be achieved using single devices. The problems of parallelling PowerMOS are much less than those which occur when using bipolar devices. MOSFETs and FREDFETs have a positive temperature coefficient of $R_{DS(ON)}$ and so tend to share the total load current equally. Any discrepancy in device or circuit resistance which causes one device to be carrying a higher proportion of the total current will cause the losses in that device to increase. The device carrying the increased current will then heat up, its resistance will increase and so the current carried will be reduced. The total load current will therefore be equally shared out between all the parallelled MOSFETs. Current sharing during dynamic (switching) instants is achieved by ensuring good circuit design and layout.
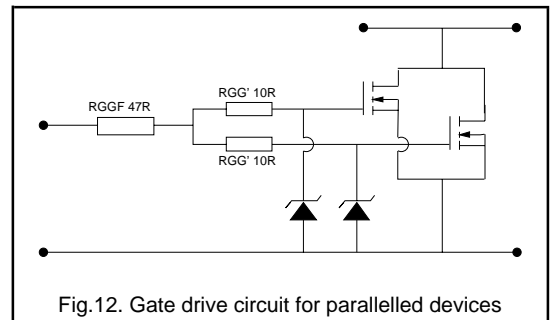
Fig.12. Gate drive circuit for parallelled devices

Moving to a system using parallelled MOSFETs requires only slight modifications to the gate drive circuit. One consideration may be the capability of the drive circuit to provide the currents required at the switching instants. It is recommended that small differential resistors, as shown in Fig.12, are used to damp out any oscillations which may occur between the switching devices and the rest of the circuit.
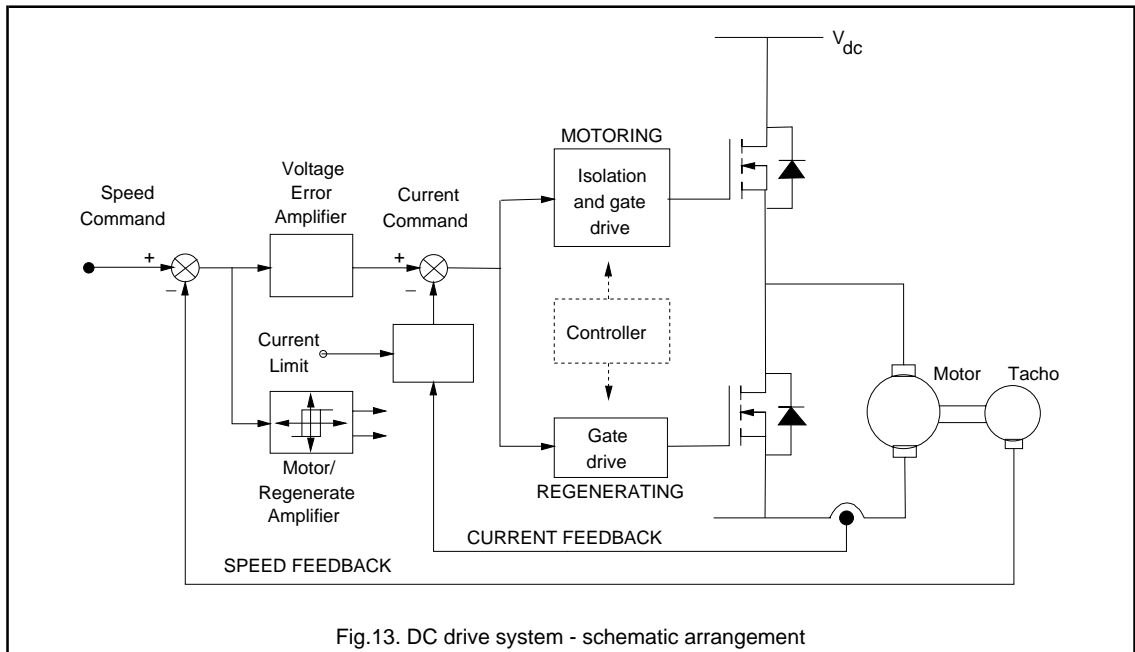
Fig.13. DC drive system - schematic arrangement

Circuit layout considerations

The effects of poor circuit design and layout are to increase RFI and noise and to compromise the performance and speed of the system due to stray inductances. The precautions which must be taken to minimise the amount of stray inductance in the circuit include:

• positioning the gate drive circuits as close as possible to the power MOSFETs.
• reducing circuit board track lengths to a minimum and using twisted pairs for all interconnections.
• for parallelled devices, keeping all connections short and symmetrical.

DC motor control system

Figure 13 shows a schematic arrangement for a two quadrant controller, showing the outer speed control loop and the inner current control loop. The speed feedback signal is derived from a tachogenerator (TGF), although alternatively an approximation to the motor speed can be derived by feeding back a signal proportional to the motor voltage, (AVF). Position feedback can be included for servo applications by using a position encoder on the motor shaft. The speed feedback loop compares the tacho- output voltage with a speed reference signal. The voltage error signal gives the current reference command.

The current command signal is compared with the actual motor current in the inner control loop. This control loop includes a current limit setting which protects the motor and the devices from overcurrents. If the controller demands a large speed change then the current demand is maintained below the maximum level by this current limit setting. Motoring or regenerating operation is detected directly from the polarity of the voltage error signal and used to determine whether it is the top or bottom MOSFET which is controlling the current. The motoring/regenerating logic circuit includes some hysteresis to ensure that control does not oscillate between the motoring and regenerating modes at low motor currents.

There are several possible ways of controlling motor current by controlling the switching sequences to the main PowerMOS devices. In tolerance band control the motor current is compared with the reference signal and an allowed current ripple tolerance. During motoring operation if the actual current is greater than the allowed maximum value of the tolerance band then the output comparator turns off the gate drive to the power MOSFET thus allowing the motor current to fall. The current then freewheels until it reaches the lower limit of the tolerance band, when the comparator turns the MOSFET back on. Using this current control strategy the effective switching frequency is variable, depending on the rate at which the armature current changes, but the peak to peak current ripple in the system is constant. Alternatively the devices can be

switched a constant frequency using a PWM method current control. Here the current error signal is compared with a fixed frequency triangular wave and the comparator output is then used to provide the signal for the main switching devices. When the error signal is greater than the triangular wave then the power device is switched on, when the error signal is less than the triangular carrier then the device is switched off.

Conclusions

DC motor controllers using PowerMOS devices can be used in many speed control and servo applications giving excellent drive performance. The advantages of PowerMOS devices include their simple gate drive requirements, rugged performance and their ease of use in parallel configurations. The intrinsic diode between the drain and source of MOSFETs and FREDFETs can be used as the freewheel diode in half bridge and full bridge circuit configurations giving a cost effective, compact design with the minimum of switching devices. PowerMOS choppers can operate at much higher switching frequencies than thyristor or power transistor controllers, giving reduced current ripple, reduced noise and interference and good dynamic system response. Using higher switching frequencies reduces the need for additional discrete inductances in the motor circuit whilst still achieving low ripple currents in separately excited, permanent magnet and series connected field wound motors.

3.2.2 A switched-mode controller for DC motors

The purpose of this paper is to demonstrate the use of an integrated switched-mode controller generally used for DC power conversion as the primary control and element in a practical Pulse Width Modulated (PWM) DC drive. Basic principles relating to DC motor specifications and drive frequency are presented. The PWM method of switched-mode voltage control is discussed with reference to armature current control, and hence output torque control, of DC motors. A series of circuit configurations are shown to illustrate velocity and position servo applications using a switched mode driver IC. Philips Semiconductors produce a wide range of control ICs for Switched Mode Power Supply (SMPS) applications which can also be used as controllers for PWM driven DC motors. This paper demonstrates how one switched-mode controller, the NE5560, can be used to give a velocity and position servo systems using Philips power MOSFETs as the main power switches. Additional application ideas using the NE5560 controller for constant speed and constant torque operation are also presented.
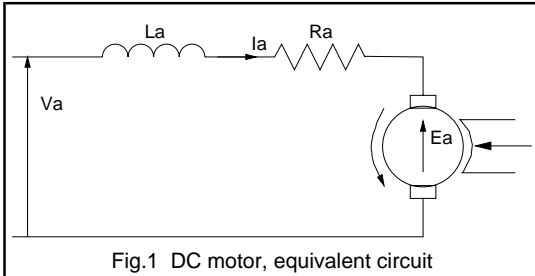
Fig.1 DC motor, equivalent circuit

Principles of the PWM DC motor drive

Pulse width modulated drives may be used with a number of DC motor types: wound field or permanent magnet. The discussion here will be particularly concerned with permanent magnet excited DC motors. This does not impose a restriction on the applicability of switched mode control for DC drives since permanent magnet motors are available in a wide range of sizes, ratings and configurations to suit many applications. The design of a pulse width modulated drive is affected by the characteristics of the DC motor load, and this will now be considered in more detail.

The permanent magnet DC motor may be represented by the simplified equivalent circuit shown in Fig.1. L_a represents the total armature inductance, R_a is the equivalent series resistance, and E_a the armature back emf. This induced emf represents that portion of the total input

energy which is converted to mechanical output. The magnitude of the armature emf is proportional to motor speed.

Motor inductance, which may vary from tens of μH to mH, will have a significant effect on PWM drive designs. This is due to the fact that average motor current is a function of the electrical time constant of the motor, τ_a, where. $\tau_a = L_a/R_a$. For a PWM waveform with a period T the ratio of pulse width to switching period is denoted by δ. The average pulse current will depend upon the ratio of the current pulse-width, δT, to the motor electrical time constant, τ_a.
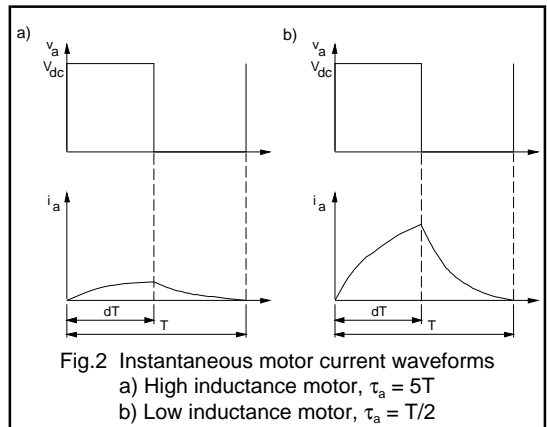
Fig.2 Instantaneous motor current waveforms
a) High inductance motor, $\tau_a = 5T$
b) Low inductance motor, $\tau_a = T/2$

Figure 2 shows the conditions for two different motors and a fixed period PWM waveform. For the case when the motor time constant is much greater than the pulse width, in Fig.2(a) then the current cannot be established in the inductive motor windings during the short duration of the applied pulse. For a low inductance motor and the same pulse width, Fig.2(b), the armature current is easily established. In most instances a motor which has high armature inductance will require a lower PWM drive frequency in order to establish the required current levels, and hence develop the necessary torque. A low inductance motor allows the use of a high switching drive frequency thus resulting in an overall faster system response.

In general, to achieve optimum efficiency in a PWM motor drive at the highest practical frequency, the motor should have an electrical time constant, τ_a, close to the duration of the applied waveform T. ($\tau_a = kT$ where k is small). The printed circuit motor is one of the lowest inductance DC motors available since the armature is etched from a flat disc-like material much like a double-sided printed circuit board. Consequential these low inductance, low inertia

motors also exhibit very fast response with quite high torque. Electrical time constants in the order of 100μs allow these motors to be used with switching rates as high as 100kHz, with typical drive circuits being operated at 10kHz.

Thus an appropriate choice of switching frequency and motor inductance ensures a high average motor current during each switching pulse. Motor current control, and hence torque control, is achieved by varying the width of the applied pulsed waveforms. As the base, or carrier, frequency is held constant then the pulse width relays torque control information to the motor. Torque is dependent on average motor current (equation 1) which, in turn, is controlled by duty cycle.

$$T_e = K_T \bar{I}_a \qquad (1)$$
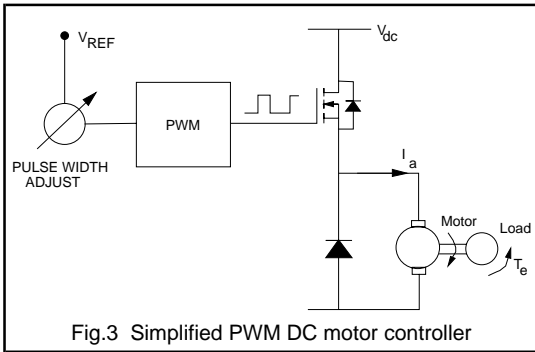
Fig.3 Simplified PWM DC motor controller

PWM motor control

The PWM method of current control will be considered by examining the conditions at motor start-up for a simple arrangement, shown in Fig.3, where the duty cycle is controlled using the DC control voltage, V_{REF}. At start-up the duty cycle is adjusted to be long enough to give sufficient motor starting torque. At zero rotational velocity ($\omega=0$) the back emf, E_a, is zero and so the full DC voltage appears across the series R_a/L_a impedance. The initial motor current is determined according to the equation:

$$L_a \cdot \frac{d i_a}{dt} + R_a \cdot i_a = V_{dc} \qquad (2)$$

If the duty cycle ratio, controlled using V_{REF}, is given by δ, then the duration of the 'ON' pulse is simply given by δT. During this interval the rise of motor current prior to armature rotation is shown by Equation 3.

$$i_a = \frac{V_{dc}}{R_a} \cdot \left(1 - e^{-t/\tau_a}\right) \qquad (3)$$

The current in the motor windings rises exponentially at a rate governed mainly by average supply voltage and motor inductance. If the pulse width is close to the time constant of the motor then the current at the end of the first pulse will reach nearly 60% of its maximum value, $I_{max} = V_{dc}/R_a$. This is shown as I_1 in Fig.4. For the remainder of the PWM cycle switch S1 is off and motor current decays through the diode at a rate dependant upon the external circuit constants and internal motor leakage currents, according to the equation:

$$i_a = I_1 \cdot e^{-(t-\delta T)/\tau_a} \qquad (4)$$

The motor current at the end of the period, T, remains at a level I_2, which is then the starting current for the next cycle, as shown in Fig.4. As the switching sequence repeats, sufficient current begins to flow to give an accelerating torque and thus cause armature rotation. As soon as rotation begins, back emf is generated which subtracts from the supply voltage. The motor equation then becomes:

$$L_a \cdot \frac{d i_a}{dt} + R_a \cdot i_a = V_{dc} - E_a \qquad (5)$$

The current drawn from the supply will consequently be less than that drawn at start-up due to the effect of the motor back emf term, E_a. For a given PWM duty cycle ratio, δ, the motor reaches a quiescent speed governed by the load torque and damping friction. Maximum motor torque is required at start-up in order to accelerate the motor and load inertias to the desired speed. The current required at start-up is therefore also a maximum. At the end of the starting ramp the controller duty cycle is reduced because less current is then needed to maintain the motor speed at its steady state value.
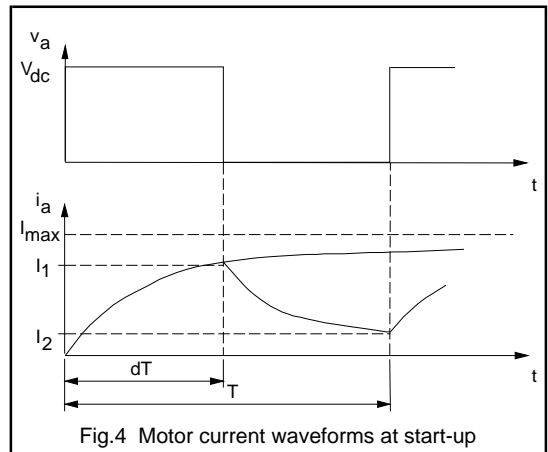
Fig.4 Motor current waveforms at start-up

Fig.5 Motor current waveform, τ_a << T
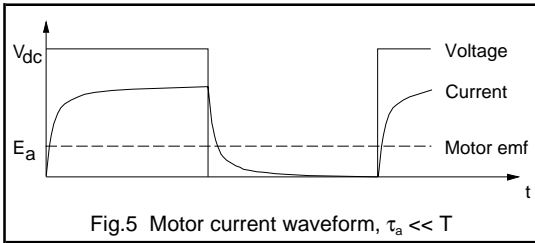
For a low inductance motor where the electrical time constant is much less than the duty cycle then the motor current waveform will closely follow the applied voltage waveform, as shown in Fig.5. An approximate expression for the average motor current is given by:

$$I_{ave} = \delta . \frac{(V_{dc} - E_a)}{R_a}$$ (6)

In summary, the principle control variable in the PWM motor control system is 'duty cycle', δ. Motor torque and velocity can be tightly controlled by controlling the PWM duty cycle and motor current.

The switched mode controller

For the remaining portion of the paper integrated switched-mode control will be considered with specific reference to the NE/SE5560 controller IC. This device incorporates control and protection functions for SMPS and DC motor control applications including internal temperature compensation, internal reference voltages, a sawtooth waveform generator, PWM amplifier and output stage. Protection circuitry includes cycle-by-cycle current limiting, soft start capability, overcurrent protection, voltage protection and feedback loop protection circuits. In the following sections some of the features of the controller will be examined and its use in a number of motor drive designs will be presented.
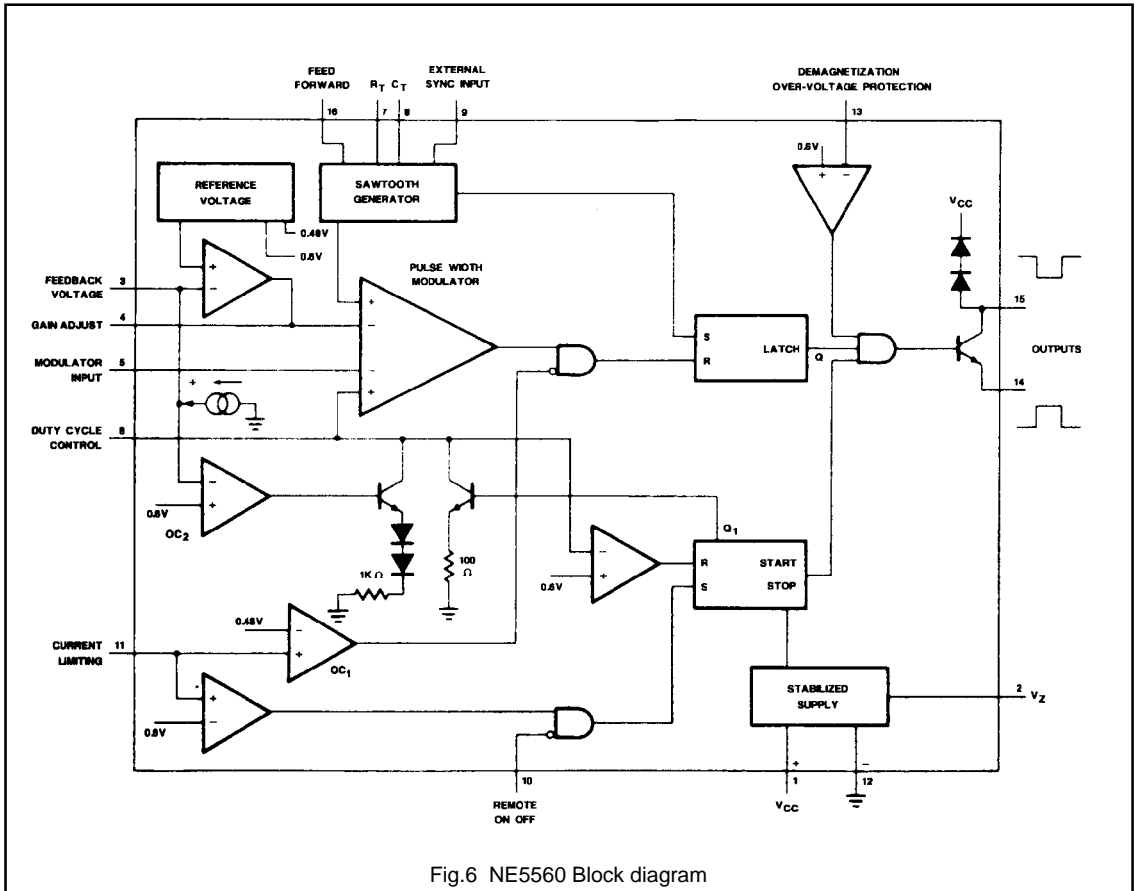
Fig.6 NE5560 Block diagram
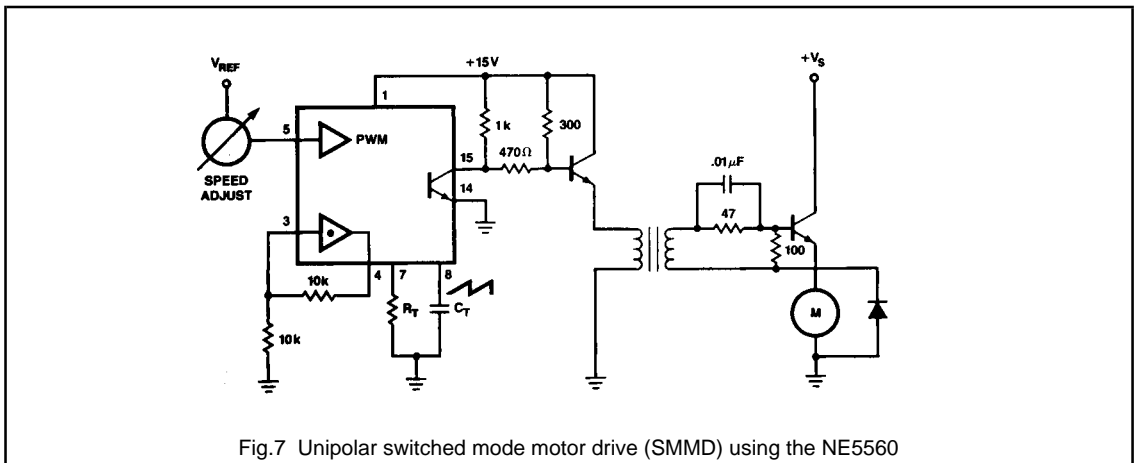
Fig.7 Unipolar switched mode motor drive (SMMD) using the NE5560

The device (see Fig.6) contains an internal voltage reference which is connected to the non-inverting input of the error amplifier. The feedback signal is obtained from either a tachogenerator (TGF - tachogenerator feedback) or from a signal proportional to the armature voltage less the winding iR voltage drop (AVF - armature voltage feedback). This feedback signal must be scaled to centre about the internal voltage reference level. The error amplifier output, in addition to being available for gain adjustment and op amp compensation, is connected internally to the pulse-width modulator. Frequency may be fixed at any value from 50Hz to 100kHz and duty cycle

adjusted at any point from 0 to 98%. Automatic shut-down of the output stage occurs at low supply threshold voltage. The error amplifier has 60dB of open loop gain, is stable for closed loop gains above 40dB and can also can be compensated for unity gain. The single ended switching output is from either the emitter or collector of the output stage. The device has protective features such as high speed overcurrent sense which works on a cycle-by-cycle basis to limit duty cycle, plus an additional second level of slow start shutdown. It is this input which can be adapted to act as a motor torque limit detector.

a) Unipolar drive   b) Bipolar drive
Fig.8 Constant speed servo configurations
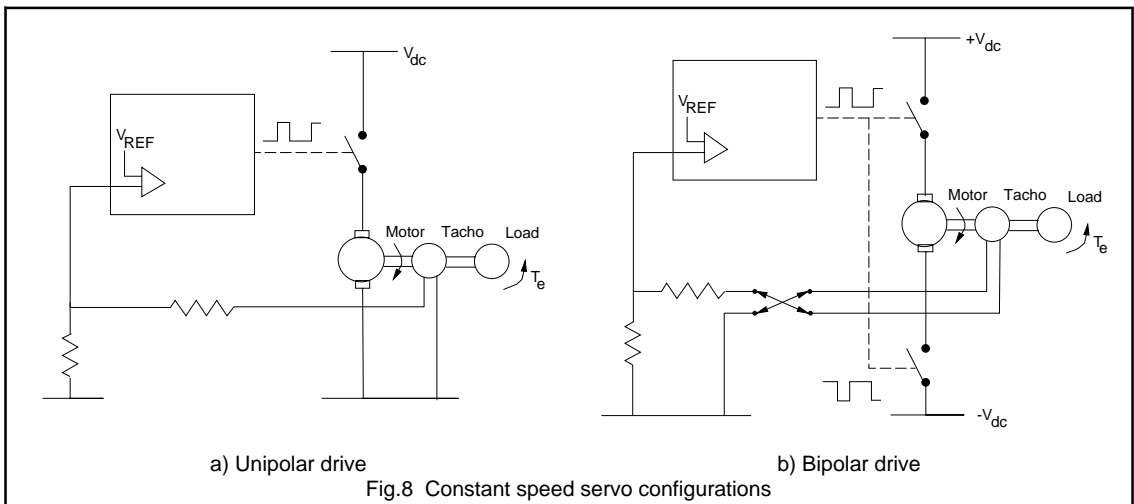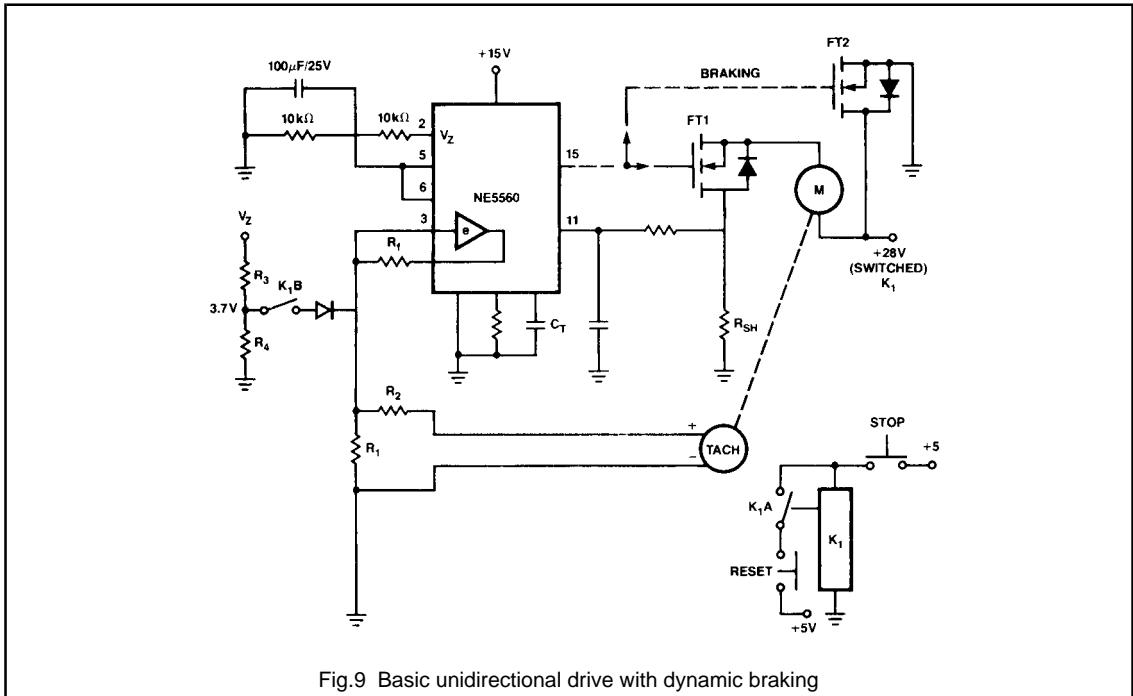
Fig.9 Basic unidirectional drive with dynamic braking

Open loop PWM control using the NE5560

For a given application the switched-mode controller frequency should be set to allow the best dynamic response considering the starting current requirement and motor electrical time constant, as discussed previously. The main drive transistors or MOSFETs must be capable of carrying the peak motor current requirement which occurs at start-up. Device protection using snubber networks and transient suppression networks will depend on the choice of switching device, system ratings and the application requirements. Power MOSFETs provide an excellent solution to many DC drive designs since very low drive power is required and they are self-protected from reverse transients by an internal intrinsic diode. PowerMOS devices may be parallelled for added power handling capability.

Figure 7 shows a simple unipolar drive capable of driving a low voltage motor supplied from an external DC voltage and PWM controlled using the NE5560.

Constant velocity servo

Figure 8 shows in block form the general circuit used to obtain a constant speed switched mode motor drive (SMMD) servo. Figure 8(a) shows a unipolar drive using DC tachometer feedback to the PWM error amplifier. Figure 8(b) shows a bidirectional drive in a half-bridge

configuration. In this case the duty cycle controls the direction of motor rotation in addition to the motor speed. A 50% duty cycle corresponds to the standstill condition. If the average duty cycle is greater than 50% (CW command) then the motor accelerates clockwise, and vice-versa for CCW rotation when the duty cycle is less than 50%. This circuit configuration can be used for both velocity and position servo-designs. The reversing switch allows the tachogenerator output to match the polarity of the PWM reference, which is always positive.

The unipolar drive circuit in Fig.9 uses the NE5560 to develop a SMMD with constant speed control suitable for a small DC motor. The switching device is a single Philips BUK456-100A Power MOSFET capable of over 30 A, with a voltage rating of 100V V_{DS} and $R_{DS(ON)}$=0.057Ω. The PWM drive from the NE5560 is applied to the gate at a nominal 10kHz, although much higher frequencies are possible. The peak gate to source voltage, V_{GS}, is 15V to ensure minimum $R_{DS(ON)}$ and hence minimum loss in the PowerMOS switch.

A sense resistor is placed in the source lead to monitor motor drive current on a cycle-by-cycle basis. The value of this resistor is set to develop the error amplifier threshold voltage at the desired maximum current. The NE5560 then automatically limits the duty cycle, should this threshold be exceeded. This is therefore used as an auto torque limit feature in addition to simply protecting the switching device.

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A slow start network (Pins 2,5,6) gradually ramps up the duty cycle at power on. Fixed braking duty cycle control is achieved by forcing the input error amplifier during braking conditions. The over-current circuit is still active during braking.

SMMD Position servo with μP control

By coupling the switched mode motor drive in a bidirectional configuration as shown in Fig.10, and then sensing linear position with a potentiometer or LVDT connected to a lead screw, for instance, the position feedback loop can be closed to give a position servo. The input to control position of the mechanical stage may be fed as a DC offset to a summing amplifier whose output is fed to Pin 5 of the NE5560, as shown. Forward lead-lag compensation may be combined with the summing amplifier function to achieve a stable response. A velocity loop may be closed through

the error amplifier at Pin 3. The controller may easily be interfaced to a microprocessor by means of a unipolar D/A converter working in the 1 to 6V output range as an input to Pin 5.

Conclusions

The switched-mode motor drive, SMMD, using small, easily available, monolithic integrated control devices designed for switched-mode power applications may easily be adapted to perform a number of useful and efficient torque, velocity and position control operations. The ready availability of good controller ICs, easily compatible with the Philips range of switching power devices in both bipolar and PowerMOS technologies makes such designs even more effective and easily attainable by the control systems designer.

Fig.10 Microprocessor control of PWM drive with four quadrant control
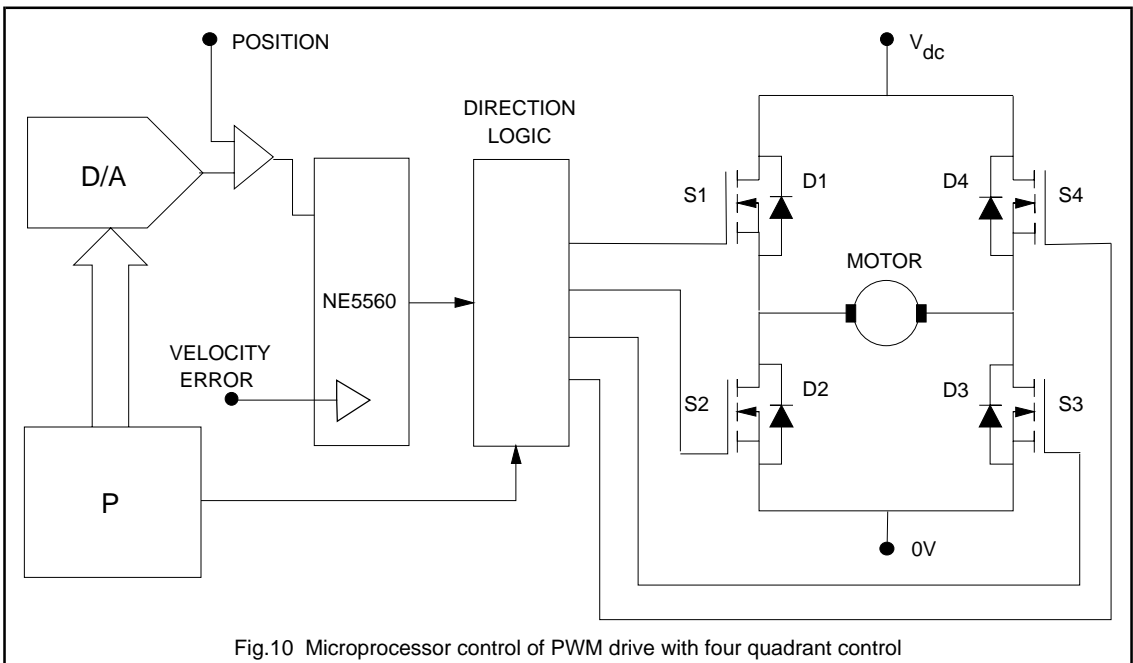
3.2.3 Brushless DC Motor Systems

In recent years the number of drive systems available to designers has increased considerably. The advent and increasing use of stepper motors, inverter-fed ac machines, switched reluctance motors and brushless machines have all addressed particular applications and in some cases these application areas overlap. The correct choice of a drive system for a particular application depends not only upon the speed and torque requirements but also on performance, response, complexity and cost constraints. The brushless DC motor (BDCM) system is emerging as one of the most useful drive options for a wide range of applications ranging from small, low power fans and disc drives, through medium size domestic appliance motors and up to larger industrial and aviational robotic and servo drives.

This section will review the theory and operation of brushless DC motors and describe some of the considerations to be made when designing BDCM drive systems using PowerMOS devices as the main inverter switches.

Background

The principal advantage of a conventional DC machine compared to an AC machine is the ease with which a DC motor can be controlled to give variable speed operation, including direction reversal and regenerative braking capability. The main disadvantage of a DC machine is that the carbon brushes of a DC motor generate dust and also require maintenance and eventual replacement. The RFI generated by the brushgear of a DC motor can be quite large and, in certain environments, the sparks themselves can be unwelcome or hazardous. The brushless DC motor was developed to achieve the performance of a conventional DC machine without the problems associated with its brushes.

The principal advantages of the BDCM system are:

• Long life and high reliability
• High efficiency
• Operation at high speeds and over a wide speed range
• Peak torque capability from standstill up to high speeds
• Simple rugged rotor construction
• Operation in vacuum or in explosive or hazardous environments
• Elimination of RFI due to brush commutation

DC motor configurations

In a conventional DC motor the field energy is provided by either a permanent magnet or a field winding. Both of these arrangements involve quite large, bulky arrangements for the field. In the case of wound field DC motors this is due to large number of turns needed to generate the required electromagnetic field in the airgap of the machine. In the case of permanent magnet DC machines the low energy density of traditional permanent magnet materials means that large magnets are required in order to give reasonable airgap fluxes and avoid demagnetisation. If either of these two options are used with the field excitation on the rotor of the machine then the inertia and weight of the rotor make the machine impractical in terms of its size and dynamic response.

A conventional DC machine has a large number of armature coils on the rotor. Each coil is connected to one segment of a commutator ring. The brushes, mounted on the stator, connect successive commutator segments, and hence armature coils, to the external DC circuit as the motor moves forward. This is necessary to maintain maximum motor torque at all times. The brush/commutator assembly is, in effect, a rotating mechanical changeover switch which controls the direction and flow of current into the armature windings.

In a BDCM the switching of current to the armature coils is carried out statically and electronically rather than mechanically. The power switches are arranged in an inverter bridge configuration in order to achieve bidirectional current flow in the armature coils, i.e. two power switches per coil. It is not possible to have a large number of armature coils, as is the case for a conventional DC motor because this would require a large number of switching devices and hence be difficult to control and expensive. An acceptable compromise is to have only three armature coils and hence six power switches. Reducing the number of armature coils means that the motor is more prone to developing ripple torque in addition to the required DC torque. This problem can be eliminated by good design of the motor. The armature of a three coil brushless DC machine in fact looks similar to the stator of a three phase AC machine and the term 'phase' is more commonly used to describe these three separate coils.

The development of brushless DC machines has made possible by developments in two other technologies: namely those of permanent magnet materials and power semiconductor switches.

Permanent magnet materials
Traditional permanent magnet materials, such as AlNiCo magnets and ferrite magnets, are limited either by their low remanence giving rise to a low airgap flux density in electrical machines, or by their susceptibility to demagnetisation in the presence of high electric fields. However in recent years several new permanent magnet materials have been developed which have much higher

Fig.1 DC motor configurations
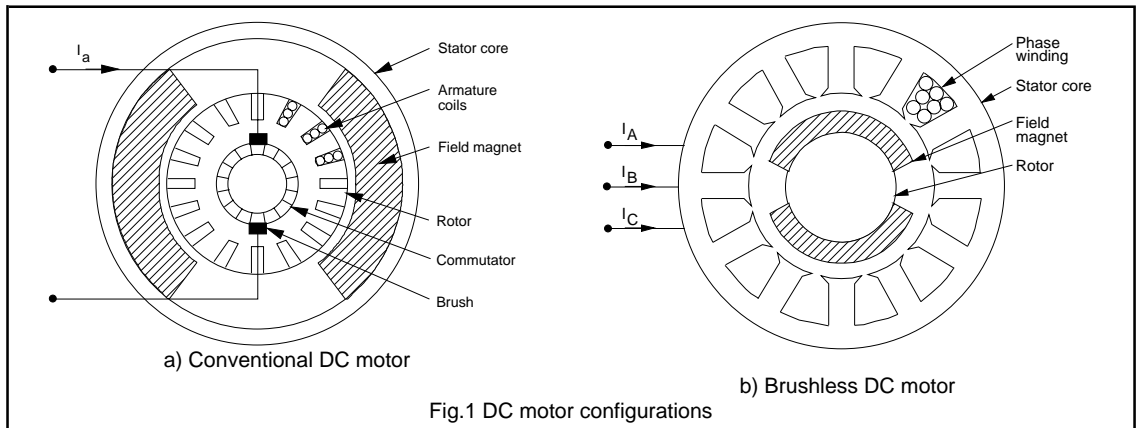
remanent flux densities, and hence airgap flux densities, and high coercivities, making them resistant to demagnetisation under normal operating conditions. Amongst these materials, called 'rare earth' magnets, Samarium Cobalt ($SmCo_5$ and Sm_2Co_{17}) and Neodymium-Iron-Boron (Nd-Fe-B) are the most common. These materials, although still quite expensive, give vastly superior performance as the field excitation for a brushless machine.

Due to the increased energy density of rare earth magnets the amount of magnet material required by the application is greatly reduced. The magnet volume using rare earths is small enough that it is feasible to have the permanent magnet field on the rotor of the machine instead of on the stator. The gives a low inertia, high torque motor capable of high performance operation. This resulting motor design, with the armature on the stator and the field on the rotor and shown in Fig.1, can be considered as a conventional DC motor turned 'inside out.'

Power electronic switches

For the 'inside out' BDCM is it still necessary to switch the armature current into successive armature coils as the rotor advances. As the coils are now on the stator of the machine the need for a commutator and brushgear assembly has disappeared. The development of high voltage and high current power switches, initially thyristors, bipolar power transistors and Darlingtons, but more recently MOSFETs, FREDFETs, SensorFETs and IGBTs, has meant that motors of quite large powers can be controlled electronically, giving a feasible BDCM system. The question of appropriate device selection for brushless DC drives will be considered later.

System description (Fig.2)

DC power supply

The fixed DC voltage is derived from either a battery supply, low voltage power supply or from a rectified mains input. The input voltage may be 12V or 24V as used in many automotive applications, 12V-48V for applications such as disc drives or tape drives, or 150V-550V for single-phase or three-phase mains-fed applications such as domestic appliances or industrial servo drives or machine tools.

Inverter

The inverter bridge is the main power conversion stage and it is the switching sequence of the power devices which controls the direction, speed and torque delivered by the motor. The power switches can be either bipolar devices or, more commonly, PowerMOS devices. Mixed device inverters, for example systems using pnp Darlingtons as the high side power switches and MOSFETs as the low side switches, are also possible. The freewheel diodes in each inverter leg may be internal to the main power switches as in the case of FREDFETs or may be separate discrete devices in the case of standard MOSFETs or IGBTs. Detailed considerations of inverter design, gate drive design and layout have been considered in separate articles.

The inverter switching speed may be in the range 3kHz to 20kHz and above. For many applications operation at ultrasonic switching speeds (>15-20kHz) is required in order to reduce system noise and vibration, reduce the amplitude of the switching frequency currents and to eliminate switching harmonic pulsations in the motor. Because of the high switching speed capability of PowerMOS devices they are often the most suitable device for BDCM inverters.

Fig.2 BDCM system
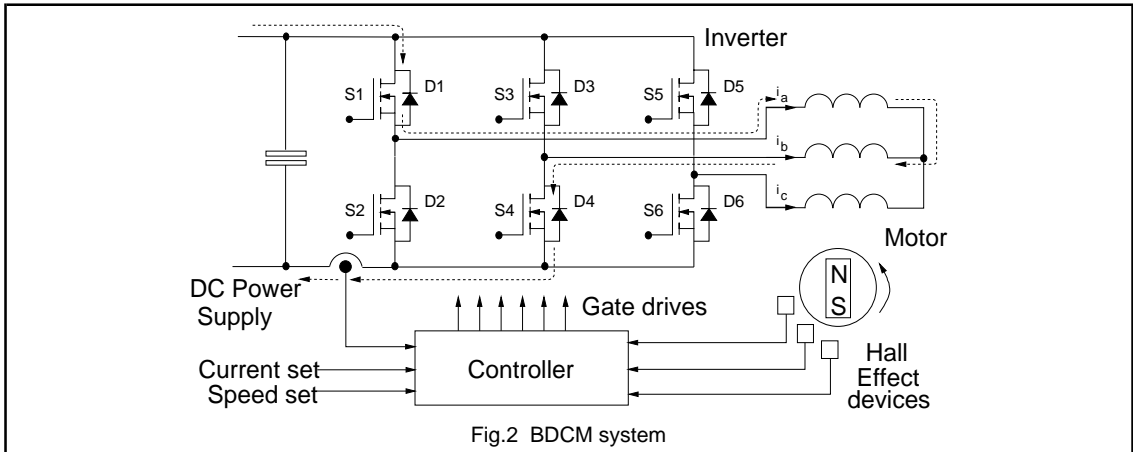
The first choice for the inverter devices might appear to be one with an N-channel MOSFET for the bottom device in each inverter leg and a P-channel device in the top half of each leg. The disadvantage of P-channel devices is that they require around three times more silicon area than equivalent N-channel MOSFETs to achieve the same value of $R_{DS(ON)}$. This makes P-channel devices uncompetitively expensive for many applications. However, using N-channel devices for both the top and bottom switches in an inverter leg means that some sort of floating drive is required for the upper device. Transformer coupled or optically coupled gate driver stages are required, or alternatively, circuits such as the bootstrap circuit shown in Fig.3 can be used to provide the drive for the top device.

In the circuit of Fig.3 the bootstrap capacitor is charged up via the diode D every time the bottom MOSFET is on. When this device turns off the capacitor remains charged up to the gate supply voltage as D is now reverse biassed. When a turn-on pulse is applied for the upper MOSFET the bootstrap capacitor provides the necessary gate source voltage to turn the device on.

Motor
A two pole BDCM with the field magnets mounted on the surface of the rotor and with a conventional stator assembly was shown in Fig.1. Machines having higher numbers of poles are often used depending upon the application requirements for motor size, rotor speed and inverter frequency. Alternative motor designs, such as disc motors or interior magnet rotor machines, are also used for some applications. The motor phases are usually connected in a star configuration as shown in Fig.2. Rotor position sensors are required in order to control the switching sequence of the inverter devices. The usual arrangement has three Hall effect sensors, separated by either 60˚ or 120˚, mounted on the stator surface close to the airgap of the machine. As

the rotor advances the switching signals from these Hall Effect latches are decoded into rotor position information in order to determine the inverter firing pattern.

In order to minimise torque ripple the emf induced in each motor phase winding must be constant during all instants in time when that phase is conducting current. Any variation in a motor phase emf whilst it is energised results in a corresponding variation in the torque developed by that phase. The so-called 'trapezoidal emf' motor, shown in Fig.4, has a constant induced emf for 120˚ and so is a practical motor design which gives optimum performance in a BDCM system.

Controller
The inverter is controlled in order to limit the device currents, and hence control the motor torque, and to set the direction and speed of rotation of the motor. The average ouput torque is determined by the average current in each phase when energised. As the motor current is equal to the DC link current (Fig.2) then the output torque is proportional to the DC input current, as in a conventional DC motor. The motor speed is synchronous with the applied voltage waveforms and so is controlled by setting the frequency of the inverter switching sequence.

Rotor position feedback signal are derived from the Hall effect devices as discussed earlier or from opto-transducers with a slotted disc arrangement mounted on the rotor shaft. It is also possible to sense rotor position by monitoring the emfs in the motor phase windings but this is somewhat more complex. In some applications the Hall effect sensor outputs can be used to provide a signal which is proportional to the motor speed. This signal can be used in a closed loop controller if required.
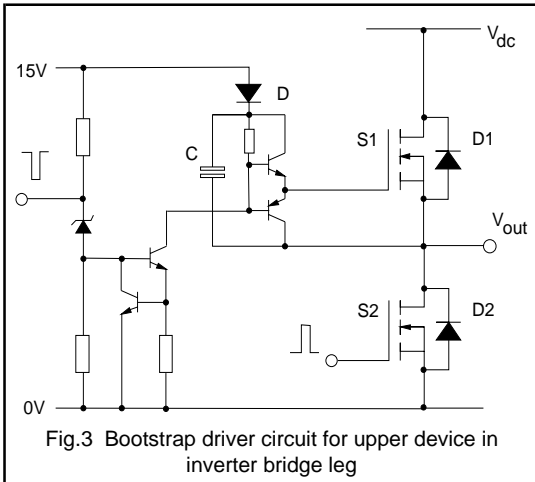
Fig.3 Bootstrap driver circuit for upper device in inverter bridge leg
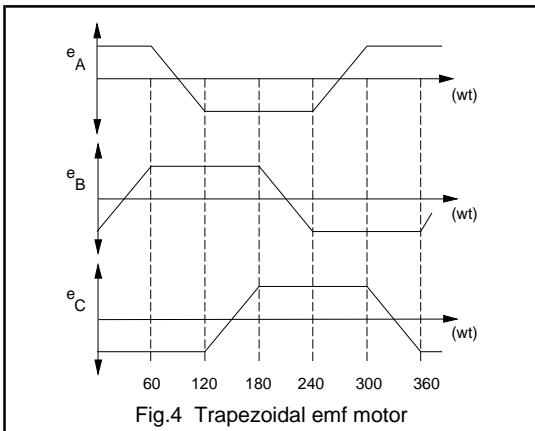
Fig.4 Trapezoidal emf motor
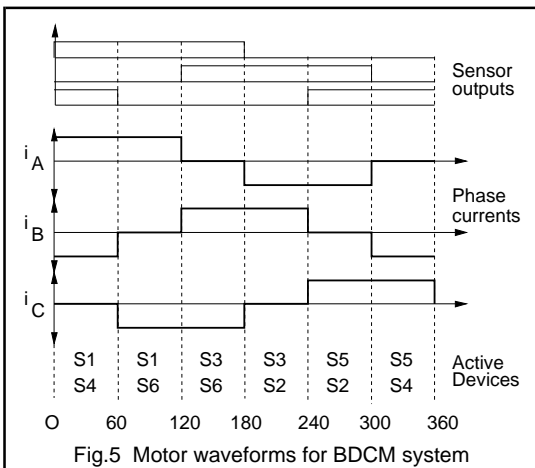
Fig.5 Motor waveforms for BDCM system

The controller also requires a current feedback signal. Usually this is taken from the DC link of the inverter as shown in the Fig.2. The current is controlled using either PWM techniques or hysteresis type of control. A current reference command is compared with the current feedback signal and then used to determine the switching signal to the main power devices. Additional controller functions include undervoltage protection, thermal protection and current ripple limit controls, error amplifier inputs for incorporation in closed loop servos and microprocessor compatible inputs.

Several IC manufacturers offer dedicated ICs providing all the functions for PWM control of brushless DC motors. The Philips version of the NE5570 CMOS controller is one such device which can be used for three phase BDCM systems using a serial data input command from a microprocessor controller. This device contains the PWM comparator and oscillator, dynamic current loop controller and output pre-drivers suitable for a MOSFET power stage. Its operation is described more fully in Philips Application Note AN1281.

Brushless DC motor operation

The operation of a BDCM system can be explained with reference to Fig.5. At any instant in time the rotor position is known by the output states of the three airgap mounted Hall effect devices. The output state of one Hall effect device switches for every 60° of rotation, thus defining six conduction zones as shown in the figure. The switching of the inverter devices is arranged to give symmetrical 120° intervals of positive and negative constant current in each motor phase winding. The position of the sensors and controller logic ensures that the applied currents are in phase with the motor emfs in order to give maximum motor torque at all times.

Referring to Figures 2 and 5, during the first 60° conduction zone switches S1 and S4 are on and the current flows through the 'A' and 'B' phase windings. The 'C' phase is inactive during this interval. At the end of this 60° conduction zone one of the Hall effect devices changes state and so switch S4 turns off and S6 turns on. The switching sequence continues as the motor advances. At any instant in time two motor phases are energised and one motor phase is off. The motor phase current waveforms are described as being 'quasi-square' in shape. The motor windings are energised for two thirds of the total time and the maximum switch duty cycle ratio is one third.

The other function of the controller is to maintain the motor phase currents at their desired constant value for each 120° interval that a particular phase is energised. The precise method of current limiting depends upon the controller algorithm. In order to limit the current to its desired value either one or both of the conducting devices are switched off thus allowing the motor current to freewheel through the

bridge leg diodes. The current is limited by controlling the switch duty cycle to ensure that device current ratings and the motor current rating are not exceeded, especially during start-up conditions or low speed operation. The amount of current ripple is controlled by the switching frequency of a PWM waveform or by the width of a hysteresis band.

Power Semiconductor switches for Brushless DC motors

Philips Semiconductors produce a range of power semiconductor devices suitable for use in BDCM systems. The include transistors, MOSFETs, FREDFETs, Logic Level MOSFETs (L²FETs) and IGBTs. These devices are available in a variety of current and voltage ratings and a range of packages, to suit individual applications.

FREDFETs
For higher voltage applications the FREDFET is an appropriate device for the inverter switches in a brushless DC drive. The FREDFET is a PowerMOS device where the characteristics of the MOSFET intrinsic diode have been upgraded to those of a discrete fast recovery diode. Thus the FREDFET is ideally suited to bridge circuits such as that shown in Fig.2 where the recovery properties of the bridge diodes significantly affect the switching performance of the circuit. Fig.6 shows a conventional MOSFET inverter bridge circuit, where the MOSFETs intrinsic diode is disabled by a series Schottky diode. A discrete antiparallel FRED carries the motor freewheeling current. Using the FREDFET reduces the component count and circuit layout complexity considerably.

MOSFET inverter leg   FREDFET inverter leg
Fig.6 MOSFET and FREDFET half bridge legs
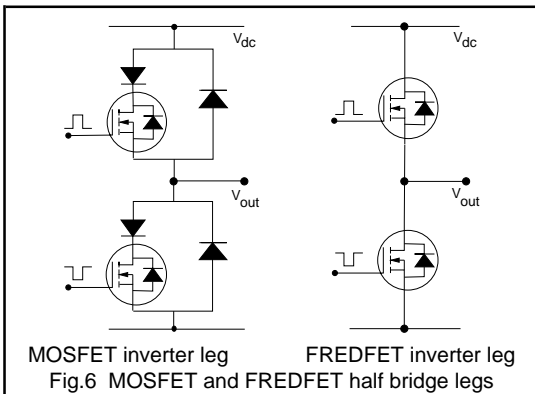
L²FETs
For many lower voltage applications logic level FETs (L²FETs) can be used to interface the power circuit with standard TTL or CMOS drive circuits without the need for level shifting stages. L²FETs require gate source voltage of only 5V to be fully turned on and typically have $V_{GS(th)} = $ 1-2V. Using Philips L²FETs in BDCM applications such as

tape or disc drives where the MOSFETs are driven directly by a controller IC produces an efficient overall design with the minimum of gate drive components.

IGBTs
IGBTs are especially suited to higher power applications where the conduction losses of a MOSFET begin to become prohibitive. The IGBT is a power transistor which uses a combination of both bipolar and MOS technologies to give a device which has low on-state losses and is easy to drive. The IGBT is finding applications in mains-fed domestic and industrial drive markets. By careful design of the device characteristics the switching losses of an IGBT can be minimised without adversely affecting the conduction losses of the device too severely. Operation of BDCM inverters is possible at switching speeds of up to 20kHz using IGBTs.

Device selection

The first selection criterion for an inverter device is the voltage rating. Philips PowerMOS devices have excellent avalanche ruggedness capability and so are able to survive transient overvoltages which may occur in the inverter circuit. This gives the circuit designer the freedom to choose appropriately rated devices for the application without suffering from the extra device conduction losses which occur when using higher voltage grade devices. In noisy environments or where sustained overvoltages occur then some external protection circuitry will usually be required.

For low voltage and automotive applications 60V devices may be adequate. For mains-fed applications then the DC link voltage is fixed by the external mains supply. A 240V supply will, depending on the DC link filtering arrangement, give a link voltage of around 330V. Using 450V or 500V MOSFETs will allow sufficient margin for transient overvoltages to be well within the device capability.

The current rating of a device is determined by the worst case conditions that the device will experience. These will occur during start-up, overload or stall conditions and should be limited by the BDCM controller. Short circuit protection must be provided by using appropriate fusing or overcurrent trip circuitry.

In addition to the normal motor currents the inverter devices will experience additional currents due to diode reverse recovery effects. The magnitude of these overcurrents will depend on the properties of the freewheel diodes and on the switching rates used in the circuit. Turn-on overcurrents can often be greater than twice the normal load current. The peak to average current capability of MOSFETs is very good (typically 3 to 4) and so they are able to carry overcurrents for short periods of time without damage. For high power applications PowerMOS devices can easily be

parallelled to give the required current ratings providing the circuit is suitably arranged in order to ensure good current sharing under both dynamic and static conditions.

Conclusions

The brushless DC motor has already become an important drive configuration for many applications across a wide range of powers and speeds. The ease of control and excellent performance of the brushless DC motors will ensure that the number of applications using them will continue to grow for the foreseeable future. The Philips range of PowerMOS devices which includes MOSFETs, FREDFETs, L^{2}FETs and IGBTs are particularly suited for use in inverter circuits for motor controllers due to their low loss characteristics, excellent switching performance and ruggedness.

Stepper Motor Control

3.3.1 Stepper Motor Control

A stepper motor converts digital information into proportional mechanical movement; it is an electro-mechanical device whose spindle rotates in discrete steps when operated from a source that provides programmed current reversals. After the appearance of the stepper motor in applications traditionally employing digital control, the advantages of precise and rapid positioning of objects using stepper motor drive systems became more obvious and this, in turn, led to a greater variety of applications. These now include:

•   paper and magnetic tape drives,
•   camera iris control and film transport,
•   co-ordinate plotters, printers, chart recorders and variable speed chart drives,
•   medical equipment,
•   fuel control, valve control and variable speed pumps,
•   meters, card readers, production line pulse counters
•   automatic weighing and labelling systems,
•   digital to analogue converters and remote position indicating equipment.

All of these applications have one thing in common - controlled motion. Wherever controlled movement and/or positioning is necessary, the stepper motor can be used to give a fast, flexible and accurate system.

From a mechanical viewpoint, the stepper motor has simple positional control, reliability and precision. Previously, simple, mechanically operated switches often provided adequate control for many positioning systems but increased performance requirements have forced the need for a better drive systems. The advantages of stepper motor systems have been gained at the expense of controller simplicity. The combination of fast controller ICs, low cost, high power, high efficiency switches, particularly MOSFETs, and the ease of use of stepper motors has lead to their current widespread use.

The full benefit of a stepper motor can only be realised if it is correctly driven. It requires a dc supply, an electronic switch and a source of control pulses (digital information). The appropriate dc supply is directed into the motor via a power electronic switching network. In effect, the motor moves through one step for each control pulse applied to the power stage electronic switches. The angle of the step depends upon the type of motor and can be from as little as 1.8˚ to as much as 15˚. Consequently, if 24 pulses are fed to the switching network, the shaft of a motor with a 15˚ step-angle will complete one revolution. The time taken for this action is entirely a function of the rate at which control pulses are applied. These may be generated by an oscillator with adjustable frequency or from a dedicated controller IC.

Principles of operation

Stepper motors can be divided into three principle types:

• permanent magnet stepper motors
• variable reluctance stepper motors
• hybrid stepper motors.
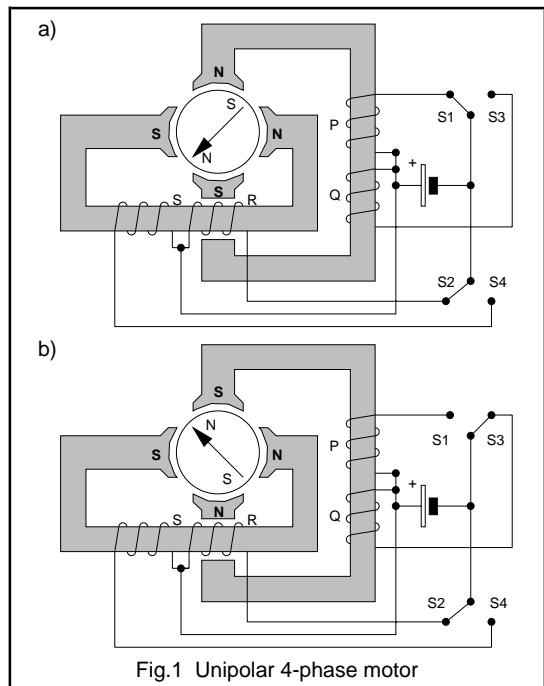
Fig.1 Unipolar 4-phase motor

Permanent magnet stepper motors

The step angle of a permanent magnet stepper motor depends upon the relationship between the number of magnetic poles on its stator assembly and the number of magnetic poles on its rotor. Since the latter is a cylindrical permanent magnet, the poles are fixed, and their number is limited, due to the characteristics of the magnetic material. Enlarging the magnet diameter to provide for a larger number of rotor poles results in a drastic increase in the rotor inertia. This reduces the starting capabilities of such a motor beyond practical use. With a permanent magnet rotor, only relatively large step angles can be obtained. However, the operating step angle can be reduced by using more than one stator stack along the length of the machine and then by offsetting the separate stacks.
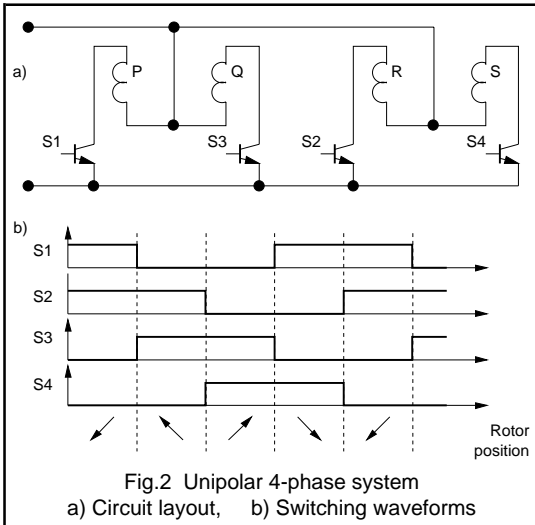
Fig.2 Unipolar 4-phase system
a) Circuit layout,   b) Switching waveforms

The stator assembly comprises two or more stators, each having a coil through which current is passed to form a magnetic field. By reversing the direction of current flowing in a coil the north and south poles developed by the coils can be transposed. Reversing the current flow through successive stator coils creates a rotating magnetic field which the permanent-magnet rotor follows. Speed of rotation is thus governed by the rate at which the stator coils (and hence the electromagnetic poles) are switched and the direction of rotation by the actual switching sequence.

There are two methods by which the current flow through stator coils can be reversed and this has led to two classes of stepper motor: those designed for unipolar drive and those for bipolar drive. For ease of description, illustrations in this section which give a diagrammatic representation of a permanent magnet stepper motor show only a 2-pole rotor although it could have as many as 24: the operating principles, however, are the same.

Motors for Unipolar drive

Each stator coil of a motor designed for unipolar drive is provided with a centre-tap which is connected to one side of the supply. The direction of current flowing through a coil is then determined by the end to which the other supply line is connected via a switching device. Switching between the coil halves results in the magnetic poles of the relevant stator being reversed.

Figure 1(a) shows a 4-phase stepper motor in which phases P and R are energised. The north poles at P and R cause the rotor to align in the position indicated. If switch S1 is turned off and S3 turned on, so that phases Q and R are now energised, then the stator field is repositioned and so the conditions illustrated in Fig.1(b) are obtained, ie. the rotor has moved through 90˚ to align with the stator field.

From this it can be seen that by altering the switching sequence for switches S1, S2, S3 and S4 the rotor can be made to advance in either direction.

Figure 2(a) shows the drive configuration for a unipolar 4-phase motor. The switching sequence of the power switches is shown in Fig.2(b). Two motor phases are energised at any one time thus giving the rotation of the stator field and required stepping motion.
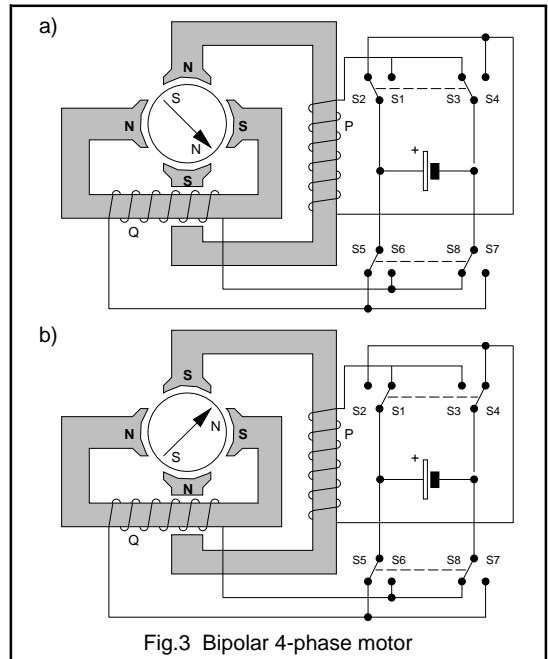
Fig.3 Bipolar 4-phase motor

Motors for Bipolar drive

The stator coils of a motor designed for bipolar drive have no centre-tap. Instead of using alternate coil-halves to produce a reversal of current-flow through the stator windings, the current is now reversed through the entire coil by switching both supply lines. Operation of a motor with bipolar drive is identical to that of one with unipolar drive, and is shown in Fig.3. Here, when the polarity of current in phase P is reversed using switches S1 to S4 the stator field realigns and the rotor moves accordingly. Figure 4(a) shows the drive configuration for a bipolar 4-phase motor. The devices are always switched as pairs, i.e. S1 and S4, S2 and S3. The switching waveforms for this configuration are shown in Fig.4(b).

The advantages of using motors with bipolar drive are shown in Fig.5. This compares the performance of a unipolar motor with its bipolar equivalent. Unipolar motors

Fig.4 Bipolar 4-phase system
a) Circuit layout,   b) Switching waveforms

bobbin so that 2-stator motors have two coils and 4-stator motors four coils. Unipolar motors require only a simple drive circuit - only four power transistors instead of eight. Moreover, the switching time requirements are less severe for unipolar drives. For a bipolar drive, care must be taken with switching times to ensure that two opposing transistors are not switched on at the same time, thus shorting out the supply. Properly operated, bipolar windings give optimum motor performance at low to medium stepping rates.

Variable reluctance stepper motors

In a variable reluctance stepper motor the motion is achieved by using the force of attraction between a magnetised component (the stator pole excited by a controlled current) and a passive steel component (the rotor pole). As successive stator poles are energised different rotor poles are attracted towards the nearest active pole, thus giving the required stepping motion. Figure 6 shows the simplest variable reluctance motor configuration having six stator poles and four rotor poles. The rotor is simply a shaped steel shaft. The stator winding is arranged so that one stator phase winding is on each stator pole.

Figure 6(a) shows the condition when the 'A' phase of the motor is energised and rotor pole 1 is aligned with the energised winding. If stator phase 'A' is switched off and phase 'B' is switched on then rotor pole 2 (which is the nearest rotor pole to any 'B' phase pole) experiences an attractive force due to the energised 'B' phase. The rotor advances to the position shown in Fig.6(b).

develop less torque at low stepping rates than their bipolar counter-parts, although at higher stepping rates the torque developed by both types of motor is nearly the same.

The 4-phase unipolar motor shown in Fig.1 has two coils per phase which must be wound on one bobbin for each stator (bifilar winding), ie. four coils in total. Because the two coils occupy the same space as a single coil in equivalent bipolar types, the wire is thinner and coil resistance higher. Bipolar motors have only one coil per

Fig.5 Torque vs. stepping rate characteristic
A) Unipolar motor   B) Bipolar motor

If, subsequentally, phase 'C' is energised then rotor pole 1 will align with the 'C' phase, as shown in Fig.6(c). The step angle of a variable reluctance motor can be reduced by having more than one set of offset rotor poles which are built up along the stack length of the machine. Different offset rotor poles align with the stator poles at each step position.

Fig.6 Variable reluctance motor
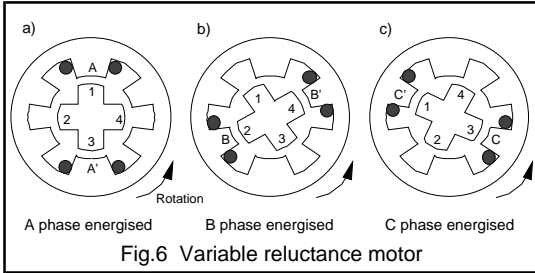
Hybrid stepper motors

The usual configuration for a hybrid stepper motor operates using the torque production methods found in both permanent magnet and variable reluctance motors. This gives a higher performance system with a low volume, and hence a low rotor inertia, and small step angles. The rotor of a hybrid stepper motor consists of an axially aligned magnet and a pair of toothed discs, one at each end of the rotor stack. The general layout is shown in Fig.7. The teeth of the discs are misaligned with respect to each other with the result that as the stator phase windings are energised different teeth align with the stator poles, in a similar way to those in a variable reluctance motor. The addition of the permanent magnet on the rotor introduces a polarity in the way that the rotor teeth align with the stator poles. Again multi-stack motors are used to reduce the step length further. Alternative hybrid stepper motor configurations have the magnets on the stator, but operate in a broadly similar manner.

Fig.7 Hybrid stepper motor, cross sectional view
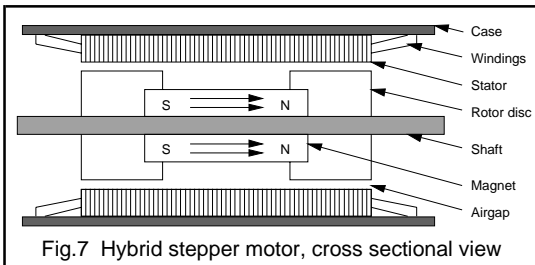
Stepper motor systems

Proper selection of the right stepper motor for a specific application calls for a thorough understanding of the characteristics of the motor and its drive circuitry. Figure 8

shows schematically the four constituent parts of a stepper motor system together with the most important aspects of each. These will be briefly considered below.

Fig.8 Stepper motor system block diagram
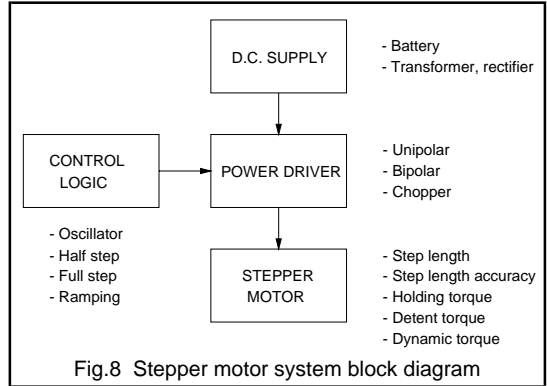
The stepper motor

Typical standard step motor angles are shown below:

Step angle	Steps per revolution
0.9˚	400
1.8˚	200
3.6˚	100
3.75˚	96
7.5˚	48
15.0˚	24

The no load step angle accuracy is specified for each type of motor For example, a motor having a step angle of 7.5˚ and will typically position to within 20' (i.e. 5%) whether the motor is made to move for 1 step or 1000 steps. The step angle error is non-cumulative and averages to zero every four steps, i.e. 360˚. Every four steps the rotor returns to the same position with respect to magnetic polarity and flux paths. For this reason, when very accurate positioning is required, it is advisable to divide the required movement into multiples of four steps. This is known as the 4-step mode of operation.

Torque
Three torques are used to define stepper motor operation:

Holding torque
At standstill, when energised, a certain amount of torque is required to deflect a motor by one step. This is known as the holding torque. When a torque is applied that exceeds the holding torque the motor will rotate continuously. The holding torque is normally higher than the working torque and acts as a strong brake in holding a load in position.

Detent torque

Due to their permanent magnets, hybrid stepper motors and permanent magnet stepper motors have a braking torque even when the stator windings are unenergised. This is referred to as the detent torque.

Working (dynamic) torque
The dynamic characteristics of a stepper motor are described by the curves of torque versus stepping rate. Typical curves were shown in Fig.5. The pull-in curve shows the load a motor can start and stop without losing steps when operated at a constant stepping rate. The pull-out curve shows the torque available when the motor is gradually accelerated to and decelerated from its required working speed. The area between the two curves is known as the slew range. The characteristic curves are used to define the correct motor selection for any particular application.

Overshoot
After executing each single step the rotor tends to overshoot and oscillate about its final position as shown in Fig.9(a). This is normal behaviour for any pulsed dynamic system. The actual response depends on the load and on the power input provided by the drive. The response can be modified by increasing the frictional load or by adding mechanical damping. However, mechanical dampers such as friction discs or fluid flywheels add to system cost and complexity and so it is usually better to damp electronically.

Fig.9 Dynamic step response
a) Single step undamped response
b) Electronically damped response
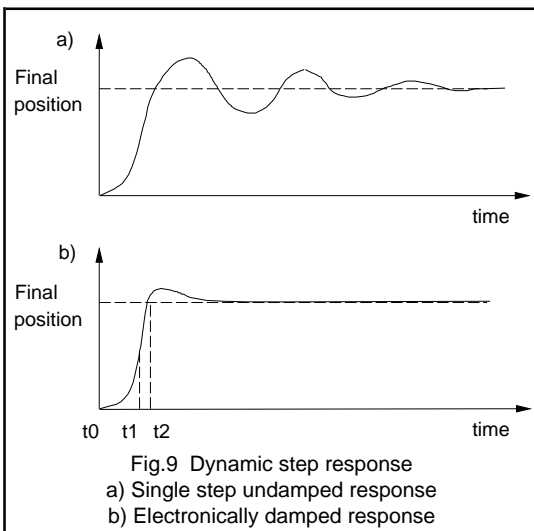
Two methods of electronic damping are commonly used - the simplest being to delay the final pulse in an incremental pulse train such that the effective length of the final step is reduced. Alternatively, every pulse, or just the final pulse in a train, can be modified into three stages, as shown in Fig.9(b). Using this method of damping a forward pulse is applied at time t_0, a reverse pulse is applied at t_1 in order

to slow the rotor down and then finally a second forward pulse is applied at t_2 which ensures the rotor comes to rest at the desired position. The accelerating torque which is developed from this final pulse is less than that for a full step and so the shaft overshoot is significantly reduced.

Multiple stepping
There are often several alternatives available in order to make a desired incremental movement. For example, a rotation of 90° can be reached in 6 steps of a 15° motor, 12 steps of 7.5° motor or in 50 steps of a 1.8° motor. Generally, a movement executed in a large number of small steps will result in less overshoot, be stiffer and more accurate than one executed in smaller number of large steps. Also there is more opportunity to control the velocity by starting slowly, accelerating to full speed and then decelerating to a standstill with minimum oscillation about the final position if small step lengths are used.

Fig.10 Controlled acceleration and deceleration profiles
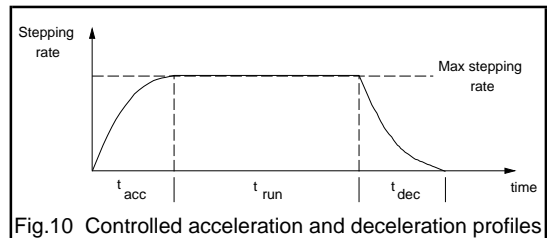
A voltage controlled oscillator and charging capacitor are usually used for acceleration (or ramp) control of the motor. The RC time constant of the ramp controller is used to give different ramp rates. Figure 10 shows a typical curve of step rate against time for an incremental movement with equal acceleration and deceleration times.

Resonance
A stepper motor operated at no-load over its entire operating frequency range will exhibit resonance points that are either audible or can be detected by vibration sensors. If any are objectionable then these drive frequencies should be avoided, a softer drive used, or alternatively extra inertia or external damping added.

Drive methods

The normal drive method is the 4-step sequence mentioned above. However, other methods can be used depending on the coil configuration and the logic pattern in which the coils are switched:

Wave drive
Energising only one winding at a time is called wave excitation and produces the same position increment as the 4-step sequence. Figure 11 shows the stepping sequence for the bipolar 4-phase motor, which was discussed earlier and shown in Fig.4. Since only one winding is energised,

holding torque and working torque are reduced by 30%. This can, within limits, be compensated by increasing supply voltage. The advantage of this form of drive is higher efficiency, but at the cost of reduced step accuracy.

Half-step mode
It is also possible to step a motor in a half-step sequence, thus producing half steps, for example 3.75˚ steps from a 7.5˚ motor. A possible drawback for some applications is that the holding torque is alternately strong and weak on successive motor steps. This is because on 'full' steps only one phase winding is energised whilst on the 'half' steps two stator windings are energised. Also, because current and flux paths differ on alternate steps, accuracy will be worse than when full stepping. The switching sequence for a 4-phase bipolar drive is shown in Fig.12.

Fig.11 Wave drive switching for 4-phase bipolar stepper motor

Fig.12 Half stepping switching for 4-phase bipolar stepper motor
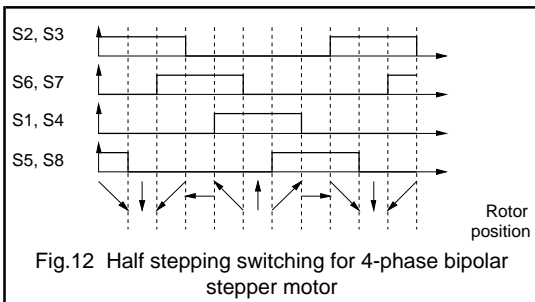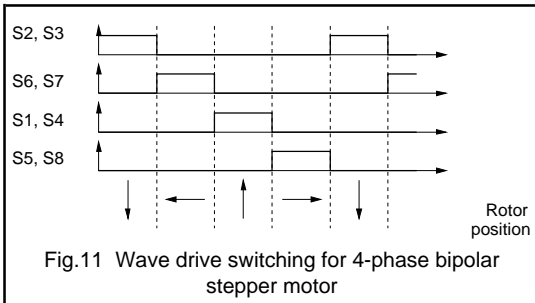
Supply considerations

When a motor is operated at a fixed rated voltage its torque output decreases as step rate rises. This is because the increasing back EMF and the rise time of the coil current limits the power actually delivered to the motor. The effect is governed by the motor time constant (L/R). Because of their higher winding resistance unipolar motors have a better L/R ratio than their bipolar equivalents. The effect can be compensated by either increasing the power supply voltage to maintain constant current as stepping rate increases, or by increasing supply voltage by a fixed amount and adding series resistors to the circuit.

Adding series resistors to the drive circuit can improve the motor performance at high stepping rates by reducing the L/R ratio. Adding a series resistor three times the winding resistance would give a modified ratio of L/4R. Supply voltage would then have to be increased to four times the motor rated voltage to maintain rated current. The addition of the extra resistance greatly reduces the drive efficiency. If the increased power consumption is objectionable some other drive method such as a bi-level voltage supply or a chopper supply should be used.

Bi-level drive
With a bi-level drive the motor is operated below rated voltage at zero step rate (holding) and above rated voltage when stepping. It is most efficient for fixed stepping rates. The high voltage may be turned on by current sensing resistors or, as in the circuit of Fig.13, by means of the inductively generated turn-off current spikes. At zero step rate the windings are energised from the low voltage. As the windings are switched in the 4-step sequence, diodes D1, D2, D3 and D4 turn on the high voltage supply transistors S1 and S2.

Fig.13 Unipolar bi-level drive
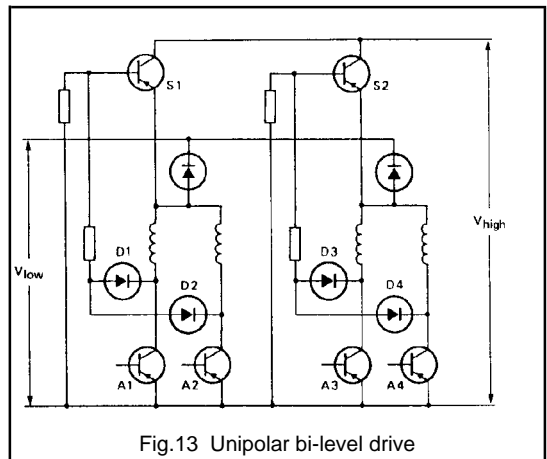
Chopper drive
A chopper drive maintains current at an average level by switching the supply on until an upper current level is reached and then switching it off until a lower level is reached. A chopper drive is best suited to fast acceleration and variable frequency applications. It is more efficient than an analogue constant current regulated supply. In the chopper circuit shown in Fig.14, V+ would be typically 5 to 10 times the motor rated voltage.

Spike suppression

When windings are turned-off, high voltage spikes are induced which could damage the drive circuit if not suppressed. They are usually suppressed by a diode across each winding. A disadvantage is that torque output

is reduced unless the voltage across the transistors is allowed to build up to about twice the supply voltage. The higher this voltage the faster the induced fields and currents collapse and performance is, therefore, better. For this reason a zener diode or series resistor is usually added as in Fig.15.
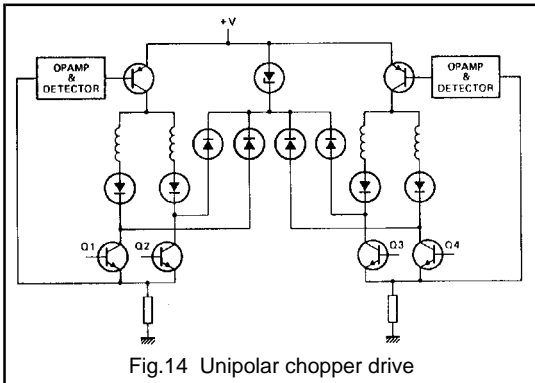
Fig.14 Unipolar chopper drive
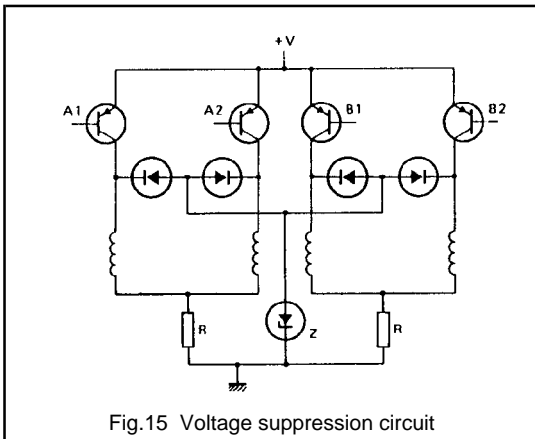
Fig.15 Voltage suppression circuit

Performance limitations

At standstill or low step rates, increasing the supply voltage produces proportionally higher torque until the motor magnetically saturates.   Near saturation the motor becomes less efficient so that increased power in unjustifiable. The maximum speed of a stepper motor is limited by inductance and eddy current losses. At a certain step rate the heating effect of these losses limits any further attempt to get more speed or torque out of a motor by driving it harder.

Terminology

Detent Torque: The maximum torque that can be applied to the spindle of an unexcited motor without causing continuous rotation.   *Unit:* Nm.

Deviation: The change in spindle position from the unloaded holding position when a certain torque is applied to the spindle of an excited motor.   *Unit:* degrees.

Holding Torque: The maximum steady torque that can be externally applied to the spindle of an excited motor without causing continuous rotation.   *Unit:* Nm.

Maximum Pull-In Rate (Speed): The maximum switching rate (speed) at which an unloaded motor can start without losing steps.   *Unit:* steps/s (revs/min).

Maximum Pull Out Rate (Speed): The maximum switching rate (speed) which the unloaded motor can follow without losing steps.   *Unit:* steps/s (revs/min).

Maximum Working Torque: The maximum torque that can be obtained from the motor: *Unit:* Nm.

Overshoot: The maximum amplitude of the oscillation around the final holding position of the rotor after cessation of the switching pulses   *Unit:* degrees.

Permanent Overshoot: The number of steps the rotor moves after cessation of the applied switching pulses.   *Unit:* steps.

Phase: Each winding connected across the supply voltage.

Pull In Rate (Speed): The maximum switching rate (speed) at which a frictionally loaded motor can start without losing steps.   *Unit:* steps/s (revs/min).

Pull In Torque: The maximum switching rate (speed) which a frictionally loaded motor can follow without losing steps.   *Unit:* steps/s (revs/min).

Pull Out Torque: The maximum torque that can be applied to a motor spindle when running at the pull out rate.   *Unit:* Nm.

Start Range: The range of switching rates within which a motor can start without losing steps.

Step Angle: The nominal angle that the motor spindle must turn through between adjacent steps.   *Unit:* degrees.

Stepping Rate: The number of step positions passed by a fixed point on the rotor per second.   *Unit:* steps/s.

Slew Range: The range of switching rates within which a motor can run unidirectionally and follow the switching rate (within a certain maximum acceleration) without losing steps, but cannot start, stop or reverse.

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Preface

This book was prepared by the Power Semiconductor Applications Laboratory of the Philips Semiconductors product division, Hazel Grove. The book is intended as a guide to using power semiconductors both efficiently and reliably in power conversion applications. It is made up of eight main chapters each of which contains a number of application notes aimed at making it easier to select and use power semiconductors.

CHAPTER 1 forms an introduction to power semiconductors concentrating particularly on the two major power transistor technologies, Power MOSFETs and High Voltage Bipolar Transistors.

CHAPTER 2 is devoted to Switched Mode Power Supplies. It begins with a basic description of the most commonly used topologies and discusses the major issues surrounding the use of power semiconductors including rectifiers. Specific design examples are given as well as a look at designing the magnetic components. The end of this chapter describes resonant power supply technology.

CHAPTER 3 describes motion control in terms of ac, dc and stepper motor operation and control. This chapter looks only at transistor controls, phase control using thyristors and triacs is discussed separately in chapter 6.

CHAPTER 4 looks at television and monitor applications. A description of the operation of horizontal deflection circuits is given followed by transistor selection guides for both deflection and power supply applications. Deflection and power supply circuit examples are also given based on circuits designed by the Product Concept and Application Laboratories (Eindhoven).

CHAPTER 5 concentrates on automotive electronics looking in detail at the requirements for the electronic switches taking into consideration the harsh environment in which they must operate.

CHAPTER 6 reviews thyristor and triac applications from the basics of device technology and operation to the simple design rules which should be followed to achieve maximum reliability. Specific examples are given in this chapter for a number of the common applications.

CHAPTER 7 looks at the thermal considerations for power semiconductors in terms of power dissipation and junction temperature limits. Part of this chapter is devoted to worked examples showing how junction temperatures can be calculated to ensure the limits are not exceeded. Heatsink requirements and designs are also discussed in the second half of this chapter.

CHAPTER 8 is an introduction to the use of high voltage bipolar transistors in electronic lighting ballasts. Many of the possible topologies are described.

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