1.i datasheet dei dispositivi delle unità funzionali (ALU 74181, registro 74198) implementate nel simulatore

datasheet ALU 14181:

-4 bit-ALU e Generatore di Funzioni (i.e. forme d'onda impulsive) Texas Instruments SN74x181/SN54x181 - https://www.ti.com/lit/ds/symlink/sn54s181.pdf?ts=1743147429951&ref_url=https%253A%252F%252Fwww.google.com%252F (fonte: ti.com)

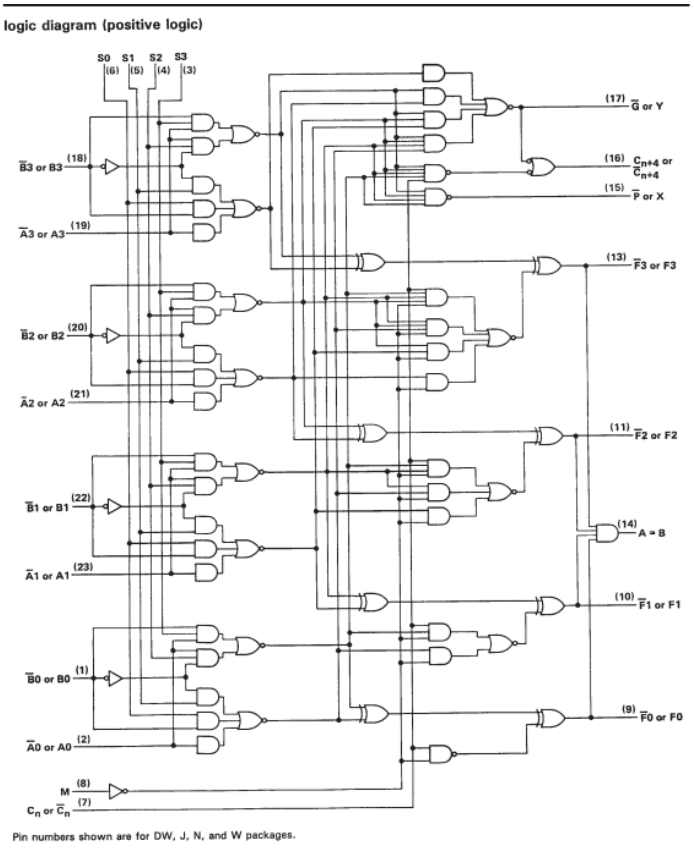
-uP Zilog Z80 - http://www.z80.info/zip/z80.pdf (fonte: z80.info)

datasheet Registri 74198:

-https://www.alldatasheet.com/datasheet-pdf/pdf/84885/TI/SN54198.html

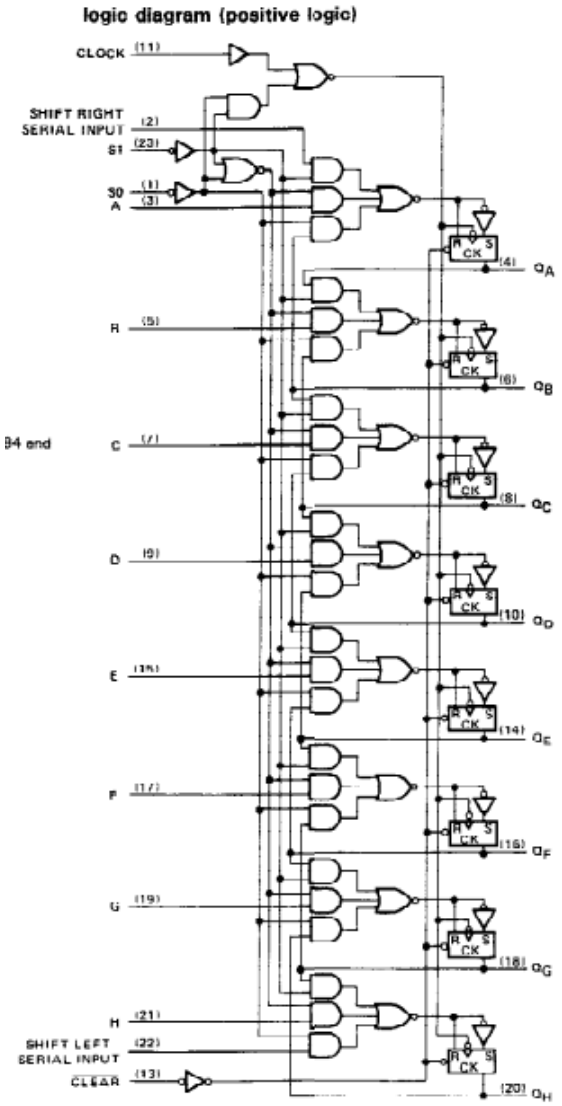
2.gli schemi dei circuiti logici delle unità funzionali implementate nel simulatore

-schema logico alu:

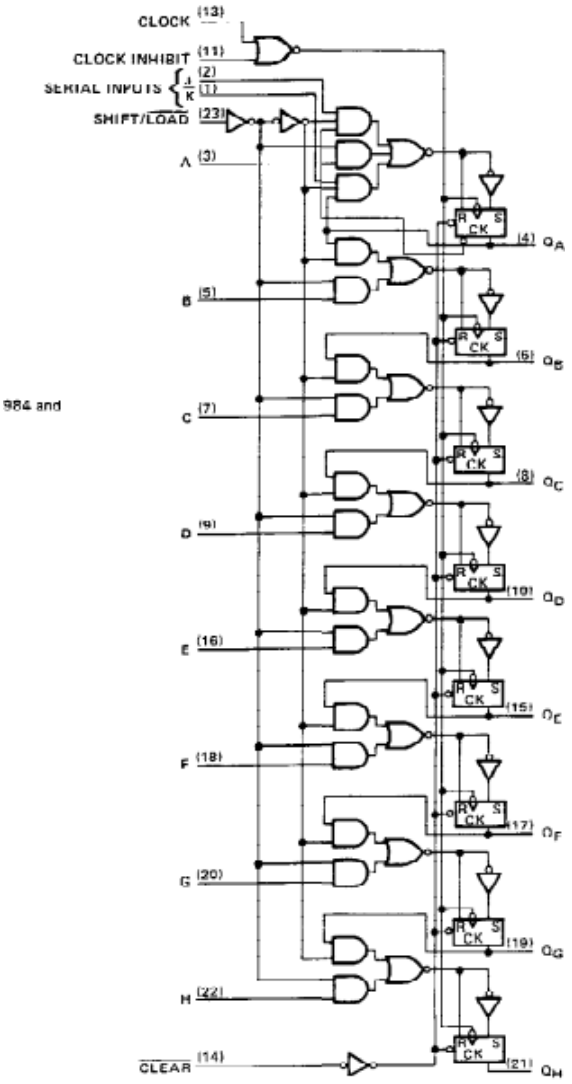


Schemi logici registri:

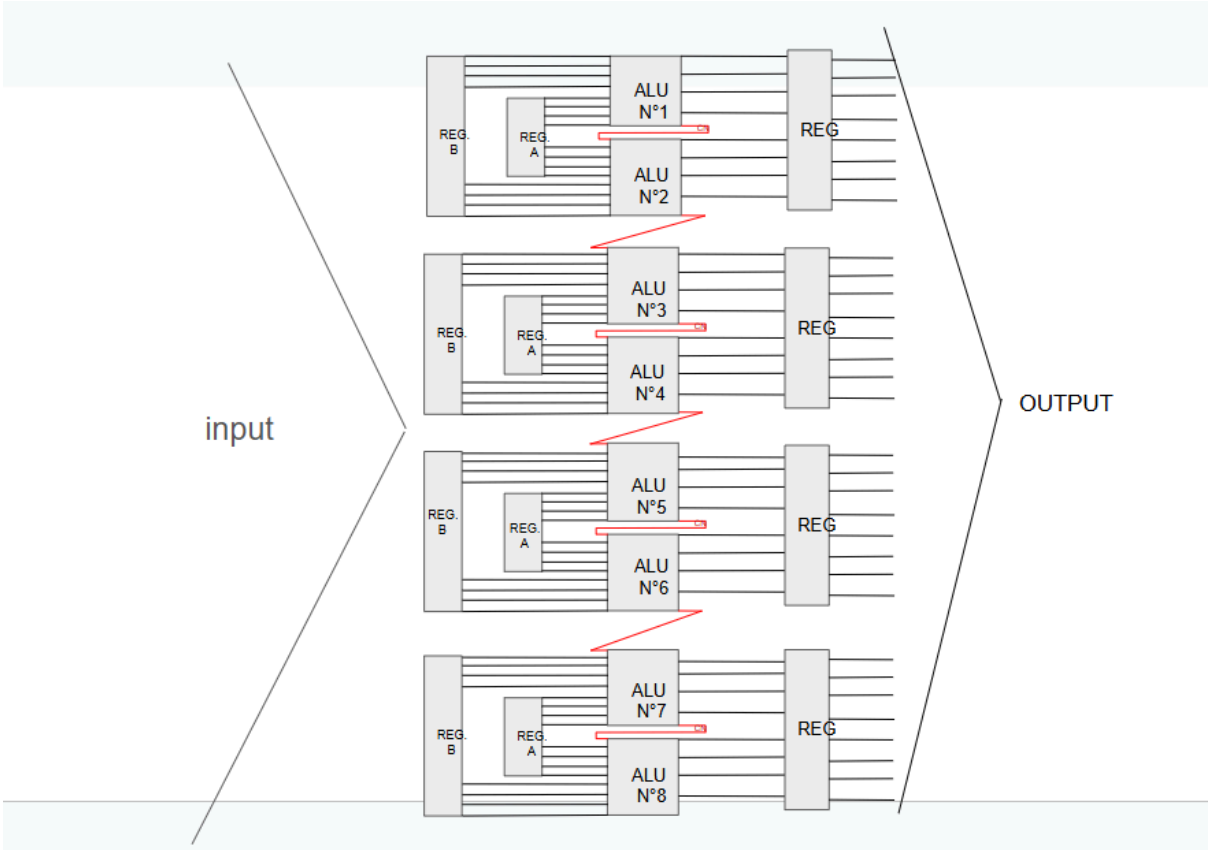
stato mem



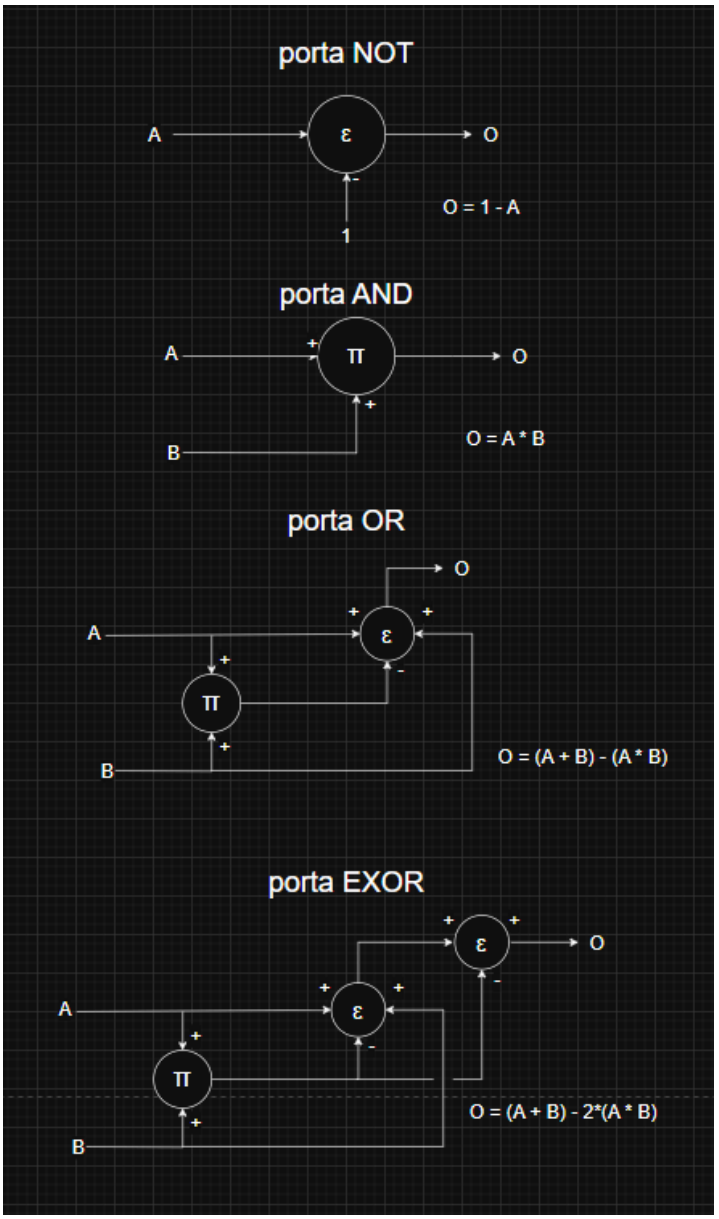
stato init



3.lo schema logico globale del simulatore



4.gli schemi a blocchi orientati degli analoghi algebrici impiegati nella sintesi computazionale delle unità funzionali minime (NOT, AND, OR, EXOR) del simulatore



5.le tavole di stato delle unità funzionali elementari del simulatore (NOT, AND, OR, EXOR, ALU 74181, registro 74198, flip-flop SR)

porte logiche:

porta NOT

A	O
0	1
1	0

porta AND

A	B	O
0	0	0
0	1	0
1	0	0
1	1	1

porta OR

A	B	O
0	0	0
0	1	1
1	0	1
1	1	1

porta EXOR

A	B	O
0	0	0
0	1	1
1	0	1
1	1	0

flip flop SR:

MEM = processo di memorizzazione

US = valori che rendono instabile la memoria

Latch S-R a porte NOR

A	B	O	On
0	0	MEM	MEM
0	1	0	1
1	0	1	0
1	1	US	US

Latch S-R a porte NAND

A	B	O	On
0	0	US	US
0	1	1	0
1	0	0	1
1	1	MEM	MEM

ALU 74181:

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A‡	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

‡Each bit is shifted to the next more significant position.

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \overline{AB}$	F = A PLUS $A\overline{B}$	F = A PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS $A\overline{B}$	F = (A + B) PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

†Each bit is shifted to the next more significant position.

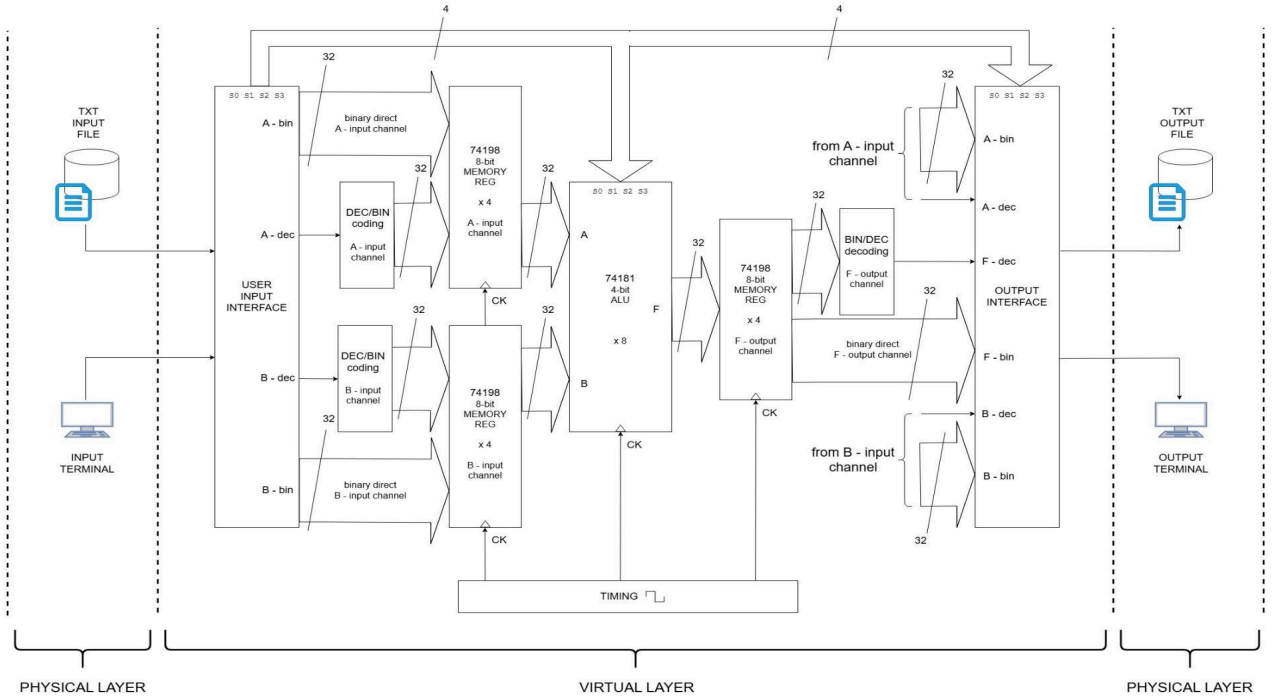
Registri 74198:

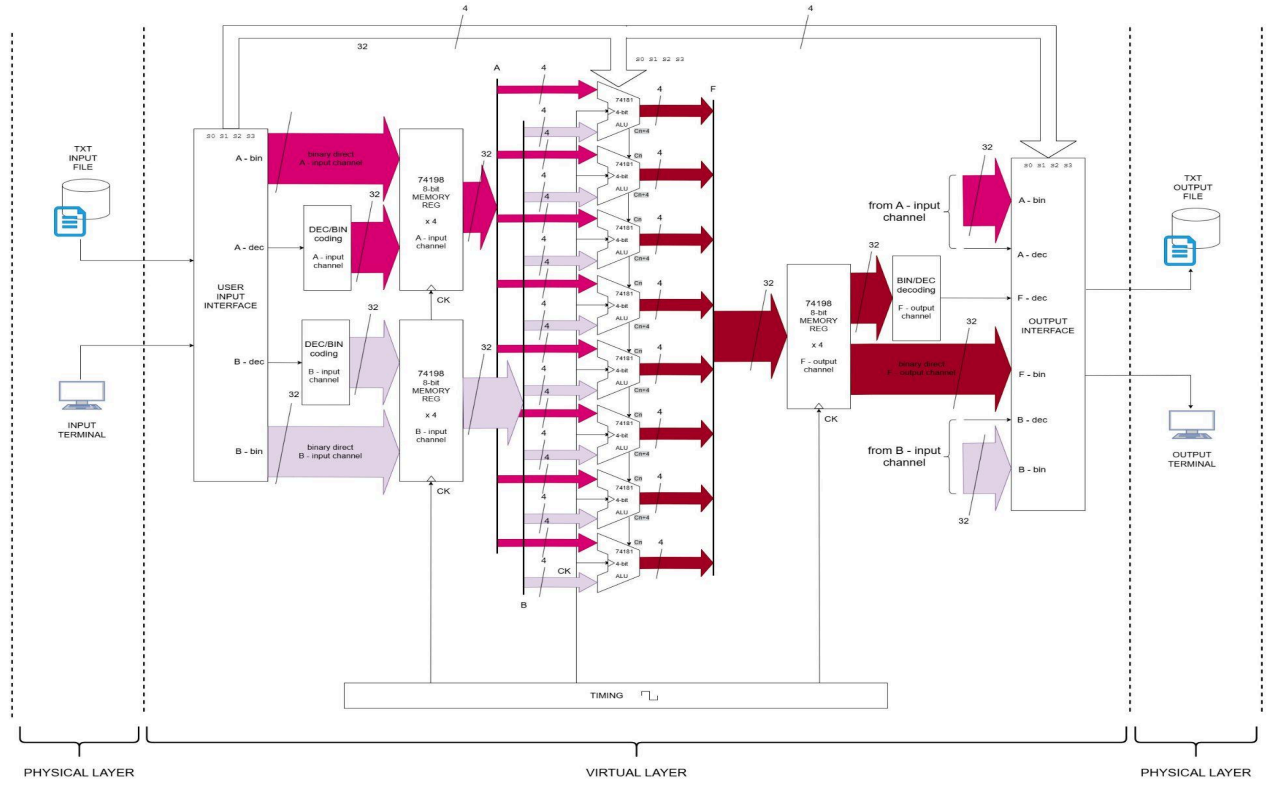
'199

FUNCTION TABLE

INPUTS							OUTPUTS			
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK INHIBIT	CLOCK	SERIAL J	SERIAL $\overline{K}$	PARALLEL A . . . H	Q_A	Q_B	Q_C . . .	Q_H
L	X	X	X	X	X	X	L	L	L	L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}
H	L	L	↑	X	X	a . . . h	a	b	c	h
H	H	L	↑	L	H	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}	Q_{H0}

6.gli schemi analitici delle architetture organizzative (es. lo schema dell'impianto modulare del codice sorgente, lo schema organizzativo delle librerie di funzioni, lo schema globale di associazione rete logica-moduli sorgente, etc.)





7.gli schemi dei processi esecutivi coinvolti (es. i diagrammi di flusso del kernel e delle funzioni accessorie invocabili)

- Non presenti

8.i codici sorgente del kernel e delle funzioni accessorie

- vedere sotto sezione

9.diagrammi e grafici analitici (es. risultati dei benchmark test applicati all'analisi delle performance del simulatore, etc.)

- Non presenti

Infine come richiesto ecco le firme dei membri del gruppo:

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Rescigno Marie:
Gatti Simone: