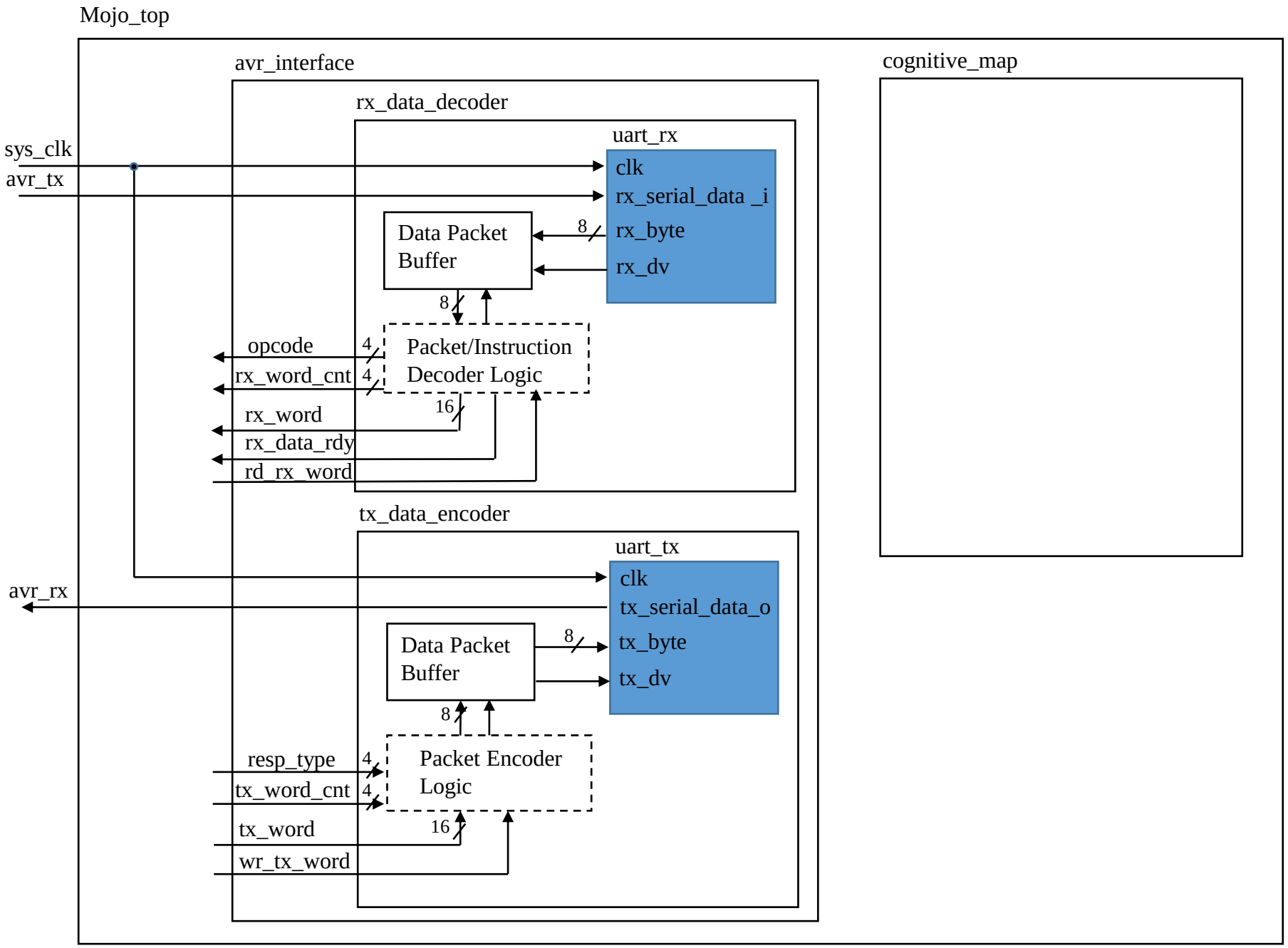
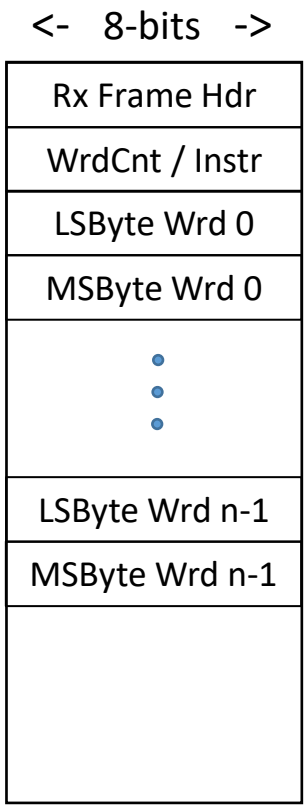
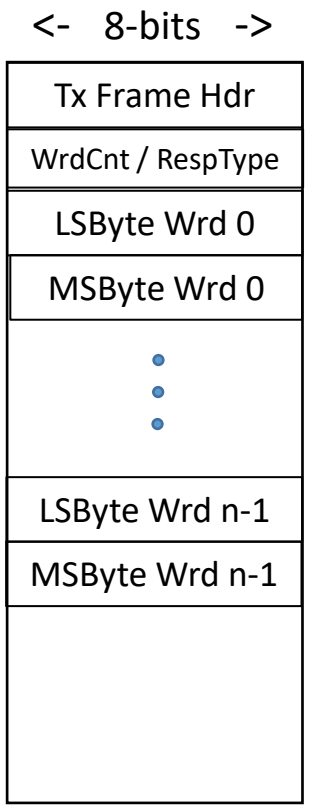

Mojo_top
avr_interface
cognitive_map
rx_data_decoder
uart_rx
sys_clk
avr_tx
clk
rx_serial_data _i
rx_byte
rx_dv
8
Data Packet
Buffer
8
opcode
4
rx_word_cnt
4
Packet/Instruction
Decoder Logic
16
rx_word
rx_data_rdy
rd_rx_word
tx_data_encoder
uart_tx
avr_rx
clk
tx_serial_data_o
tx_byte
tx_dv
8
Data Packet
Buffer
8
resp_type
4
tx_word_cnt
4
Packet Encoder
Logic
16
tx_word
wr_tx_word

Avr Tx -> FPGA Rx Data Packet

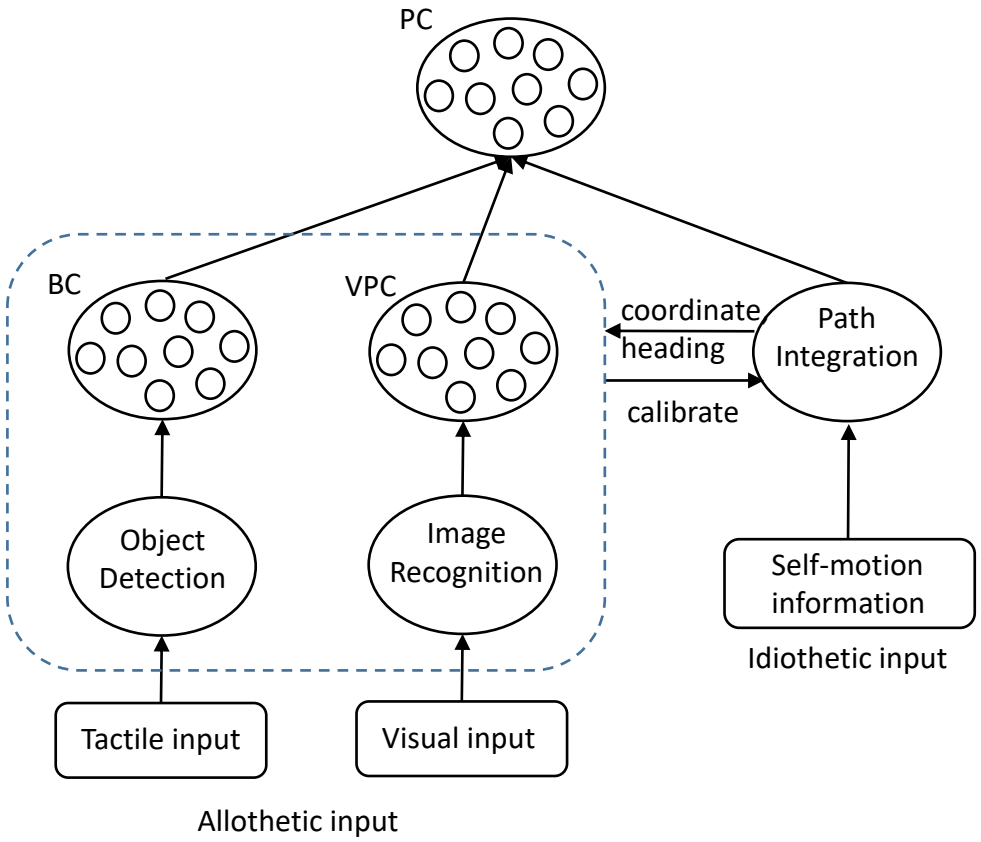


FPGA Tx Data Packet -> Avr Rx

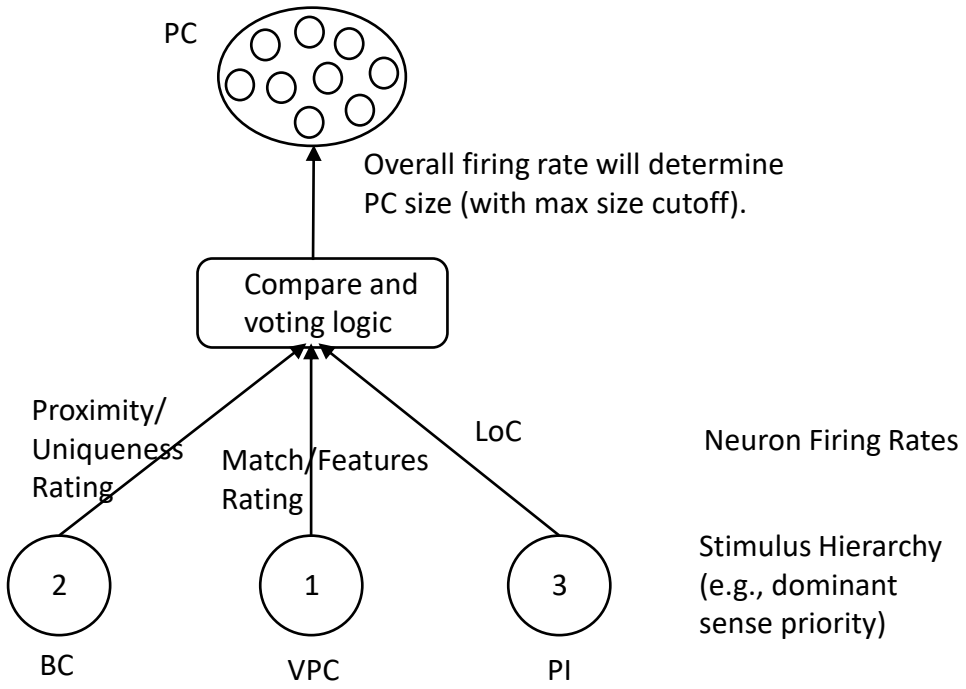


Cognitive Map Module Opcodes

Opcode	Operation	Description	Data Sent	Data Returned
4’h0	Comm. Test Loop			
4’h1	BC placement			

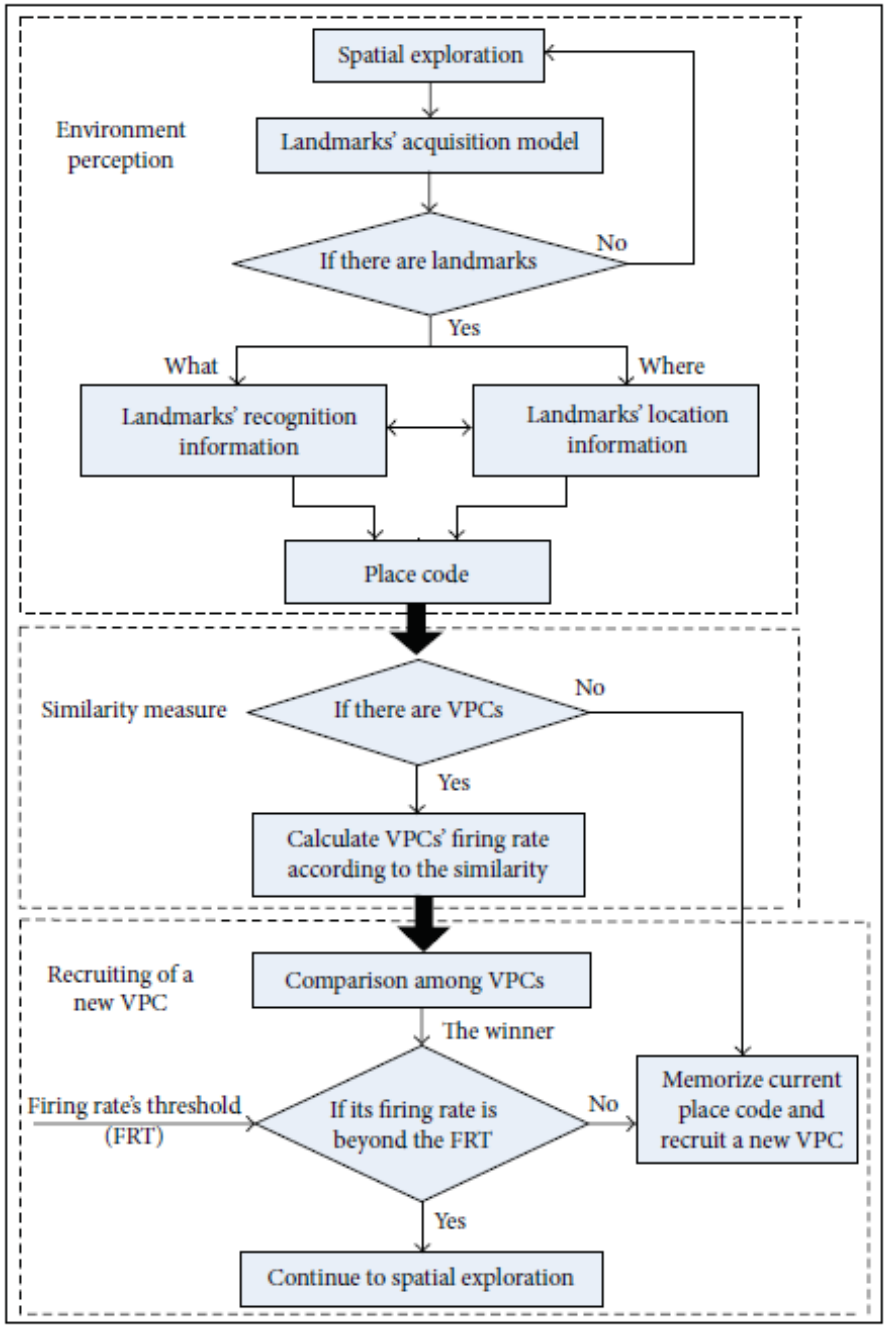


(My) Thesis proposed model of the PC firing field sources. The cognitive map located in the FPGA will possess BCs, VPCs and PCs



(My) Thesis proposed model of the PC firing field sources. The cognitive map located in the FPGA will possess BCs, VPCs and PCs

A VPCs generation model [18]:



Boundary Cell Logic as implemented in the FPGA.