5	**Sequential Logic Circuit Design:** sequential circuits Introduction difference between combinational circuits and sequential circuits flip- flop: SR, JK, D, T preset & clear master and slave flip flops their truth tables and excitation tables conversion from one type to another type of flip flop application of flip-flops: bounce elimination switch registers counters Registers: buffer register; shift register Counters: asynchronous counter synchronous counter ring counters BCD counter johnson counter modulus of the counter	**10**	**10**

UNIT 5

SEQUENTIAL LOGIC CIRCUITS

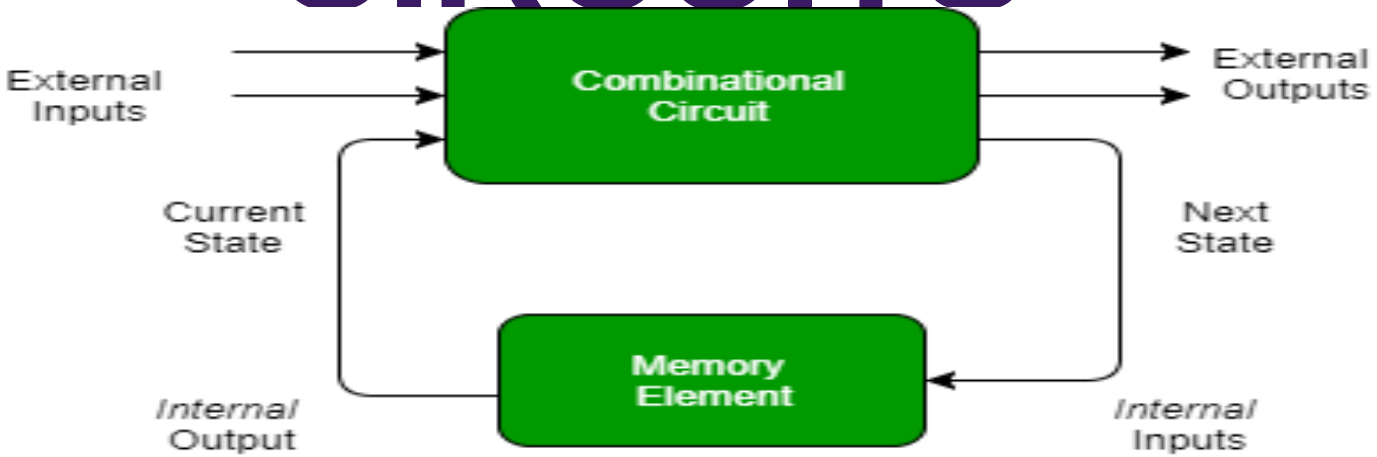


Figure: Sequential Circuit

Introduction

- The digital systems in general are classified into two namely:

1. Combinational logic circuits
2. Sequential logic circuits.

Combinational circuits :

- Till now we have discussed only the combinational circuits
- The output of a combinational circuit at any instant of time, depends only on the levels present at input terminals. It does not depend on the past status of inputs.
- The combinational circuits do not use any memory. Therefore the previous states of input does not have any effect on the present value of the cintil

Sequential Circuits :

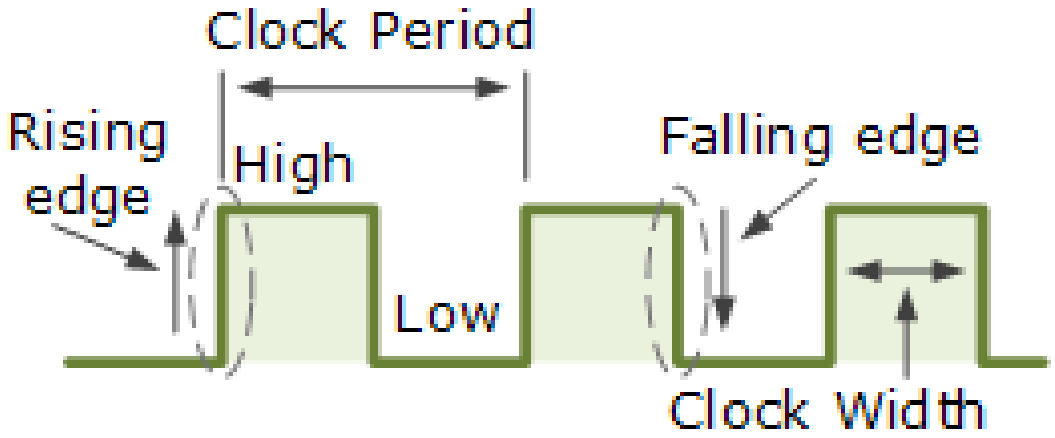
- In the sequential circuit, the timing parameter also needs to be taken into consideration.
- The output of a sequential circuit depends on the present time inputs, the previous output (past) and the sequence in which the inputs are applied.
- In order to provide the previous input, a memory element is required as shown in the figure.

Comparison

A type of digital circuit where the output is only a pure function of the present input	A type of digital circuit whose output depends not only on the present value of its input signals but also on the sequence of past inputs
Output depends on the present input	Output depends on the present input and past outputs
There is no memory unit	There is a memory unit to store immediate results
There is no clock	There is a clock
Ex: Half adder, full adder, multiplexer, de-multiplexer, encoder, and, decoder	Ex: flip flop and registers

Clock Signal

- The clock signal is a timing signal.
- Every sequential signal will have this timing signal applied as an input signal.
- Clock is a rectangular signal as shown in fig.with a duty cycle equal to 50%.means its ON time is equal to its OFF time.
- The clock signal repeats itself after every T seconds.

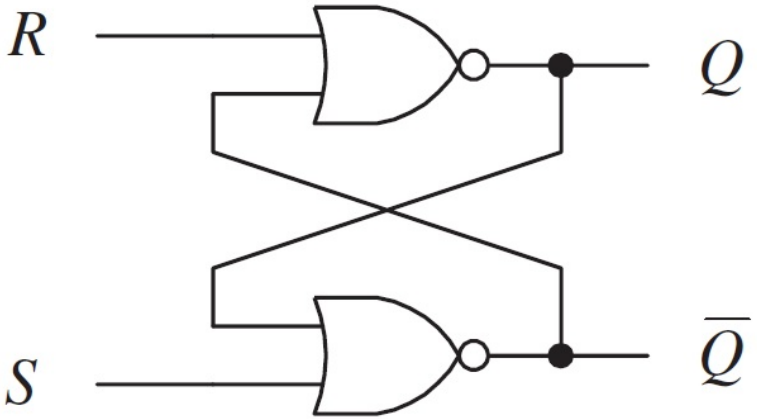


Flip-Flops

- A flip-flop is **a device which stores a single bit (binary digit) of data**; one of its two states represents a "one" and the other represents a "zero".
- Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics.

S-R Flip Flop

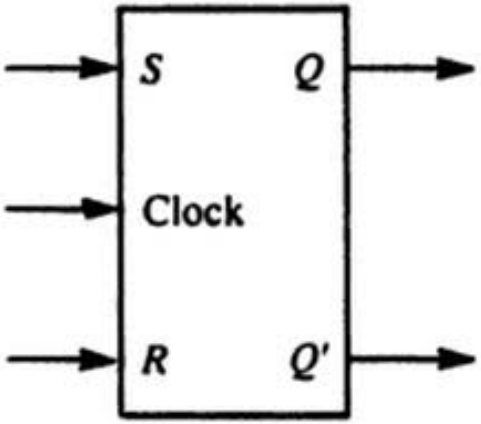
The SR flip flop is a 1-bit memory bistable device having two inputs, i.e., SET and RESET. The SET input 'S' set the device or produce the output 1, and the RESET input 'R' reset the device or produce the output 0. ... The SR flip flop stands for "**Set-Reset**" **flip flop**.

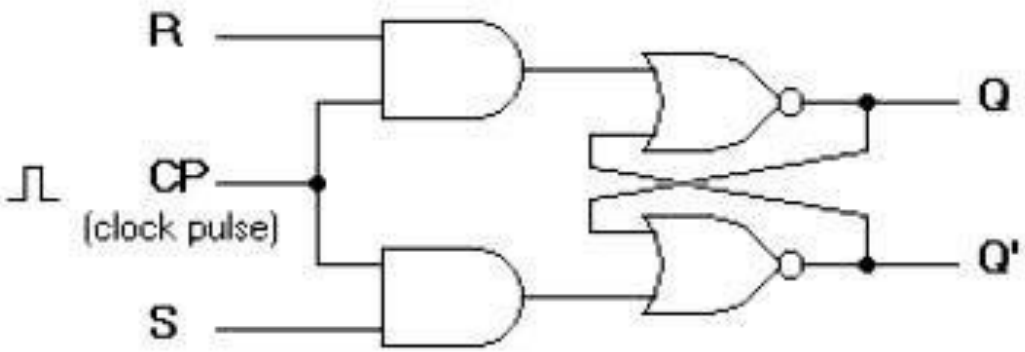


S	R	Q+1
0	0	Q
0	1	0
1	0	1
1	1	x

S	R	Q	Q+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

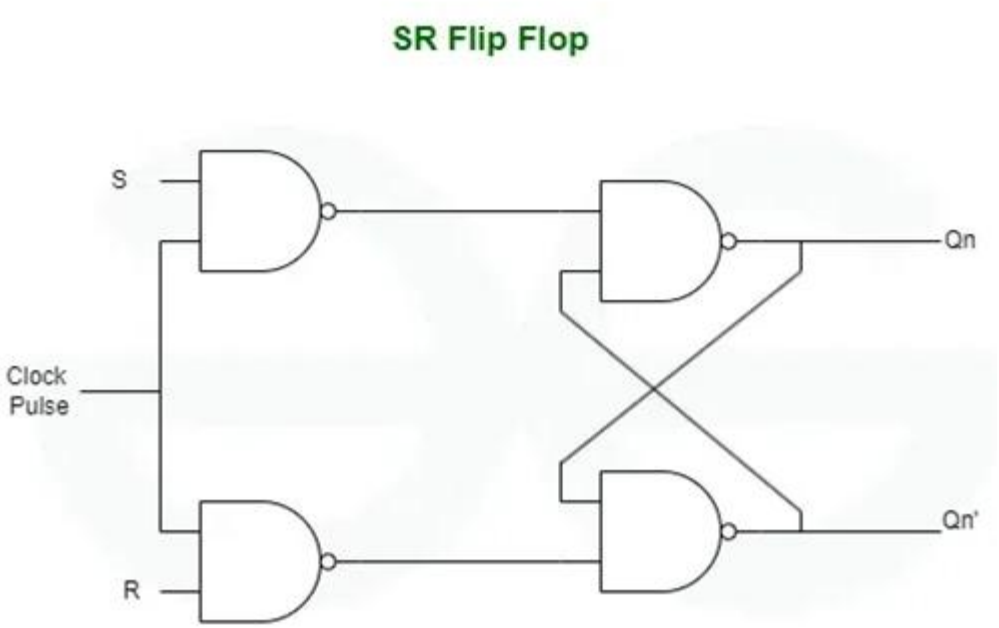
Clocked SR Flip flops using AND and NOR





(a) Logic diagram

Clocked SR Flip flops using NAND

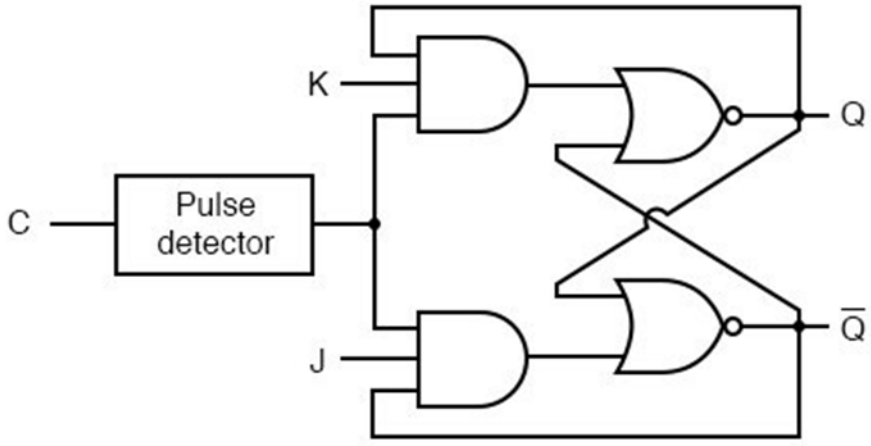


S	R	Qn+1	State
0	0	Qn	Hold
0	1	0	Reset
1	0	1	Set
1	1	X	Invalid

S	R	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Invalid
1	1	1	Invalid

- For S=R=0 the latch output does not change.
- For S=0,R=1 is called as the “Reset” condition as Q=0 and Q=1
- For S=1,R=0 is called as the “Set” condition as Q=1 and Q=0
- S=R=1 is the prohibited state. The output is unpredictable. This condition should therefore be avoided.

Edge Triggered (Clocked) JK Flip flops



Clock	J	K	Q+1
↑	0	0	Q
↑	0	1	0
↑	1	0	1
↑	1	1	$\overline{Q}$

A **JK flip-flop** is a type of flip-flop or bistable multivibrator, which is a fundamental building block in digital electronics used for memory and control applications.

A JK flip-flop is typically edge-triggered, meaning its state changes occur on a clock signal transition (rising or falling edge).

It is an improvement over the SR flip-flop, avoiding the invalid state when both inputs are high.

Key Points:

Inputs: It has two inputs: **J** (Set) and **K** (Reset).

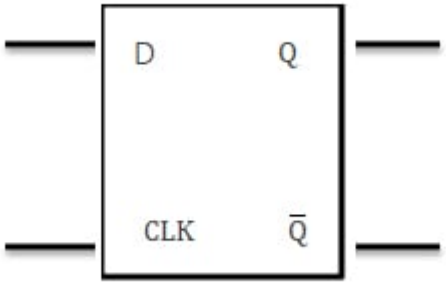
Outputs: Two outputs, **Q** (normal) and **Q'** (complement).

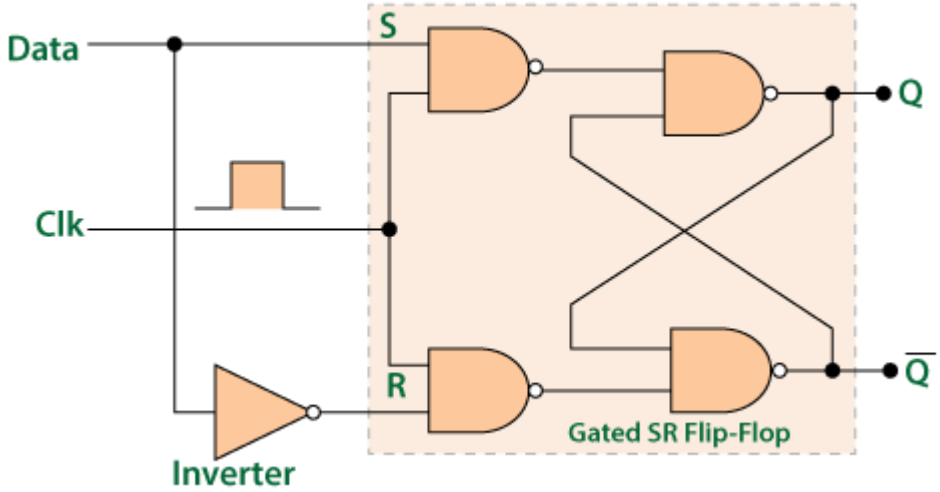
Operation:

- When **J = 0, K = 0**: No change in the output (Q holds its state).
- When **J = 0, K = 1**: Q is reset to 0.
- When **J = 1, K = 0**: Q is set to 1.

  When **J = 1, K = 1**: The output toggles (Q flips to its opposite state).

D Flip-Flop





Q	D	Q+1
0	0	0
0	1	1
1	0	0
1	1	1

A **D flip-flop** (Data or Delay flip-flop) is a type of flip-flop used in digital electronics for storing a single bit of data.

Key Points:

Inputs: It has one main input **D** (Data) and a **Clock** input.

Outputs: Two outputs, **Q** (normal) and **Q'** (complement).

Operation:

- On the clock's active edge (rising or falling), the value of **D** is transferred to the output **Q**.
- The output **Q** remains stable until the next clock edge.

Function: It acts as a latch that stores the value of **D** at the clock edge.

Applications:

- Data storage
- Shift registers
- Synchronizing signals in digital circuits

Simplified Behavior:

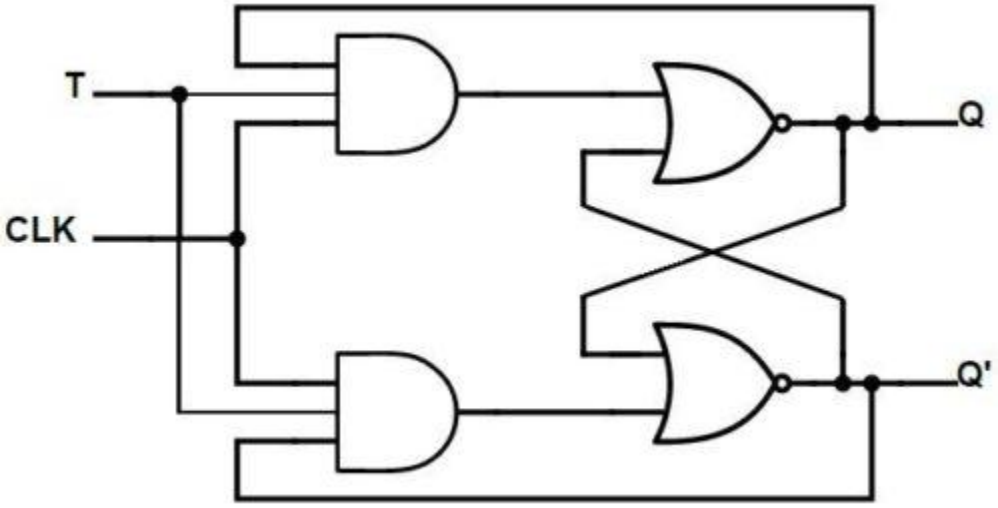
D = 0 → Q = 0

D = 1 → Q = 1

T Flip-Flop

- T stands for Toggle. So it is called as Toggle flip flop
- T flip flop has only one Input Terminal.
- T flip flop can be obtained from JK Flip flop simply by combining J and K terminal together.

T Flip-Flop



h Table

CLK	T	Q+1
0	X	0
↑	0	Q Present state
↑	1	$\overline{Q}$ Toggle

Q	T	Q+1	
0	0	0	If T =0 ,present state(Q) will occur
0	1	1 TOGGLE	If T =1 ,opposite of present state (Q) will occur
1	0	1	If T =0 ,present state(Q) will occur
1	1	0 TOGGLE	If T =1 ,opposite of present state (Q) will occur

A **T flip-flop** (Toggle flip-flop) is a type of flip-flop that toggles its state when triggered.

Key Points:

Inputs: It has one input **T** (Toggle) and a **Clock** signal.

Outputs: Two outputs, **Q** (normal) and **Q'** (complement).

Operation:

- **T = 0**: No change in the output (Q holds its state).
- **T = 1**: The output **Q** toggles to its opposite state on the clock's active edge.

Function: It is derived from the JK flip-flop by tying the **J** and **K** inputs together (T = J = K).

Applications:

- Counters (e.g., binary counters)
- Frequency division
- Toggle switches in digital systems

Simplified Behavior:

T = 0 → Q = Q (No change)

T = 1 → Q = Q' (Toggles state)

Registers

Registers in digital circuits are essential components used for data storage and transfer. They consist of a group of flip-flops, with each flip-flop storing one bit of data.

Definition: A register is a collection of flip-flops, where each flip-flop stores one bit of information. Registers are used to hold binary data for processing and temporary storage in digital systems.

Size: The number of flip-flops in a register determines its size. For example, an 8-bit register has 8 flip-flops, allowing it to store 8 bits of data.

Types of Registers:

1) **Buffer Registers**: Temporarily hold data during transfer between components.
2) **Shift Registers**: Transfer data serially (bit by bit) either left or right.
3) **Counter Registers**: Increment or decrement stored data, often used in counters.

Buffer Register

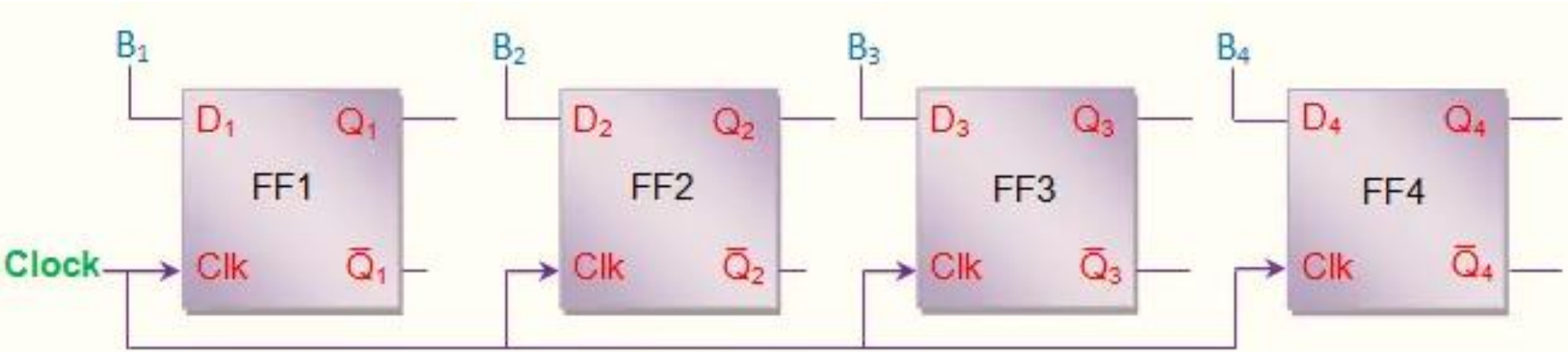
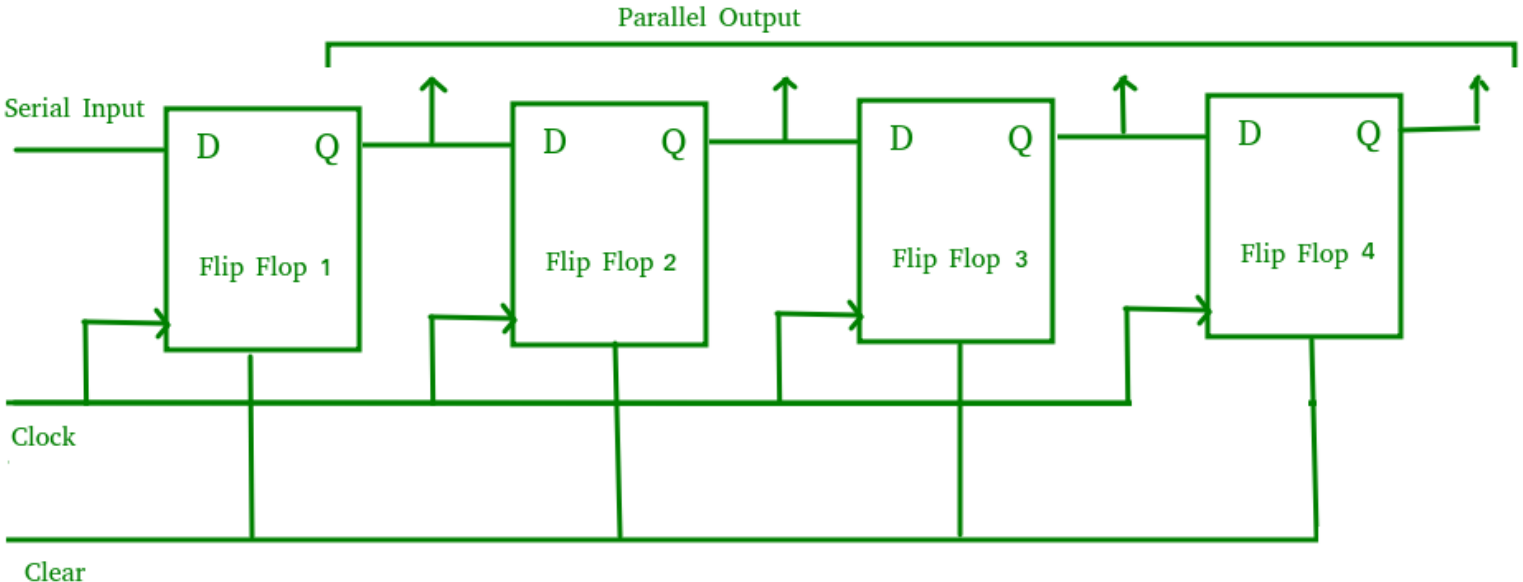


Figure 1 **4-bit Buffer Register**

Shift Register

- A shift register is a digital circuit that moves stored bits by connecting multiple flip-flops in series.
- **Types of Shift Registers**
- Serial-in/serial-out.
- Parallel-in/serial-out.
- Serial-in/parallel-out.
- Universal parallel-in/parallel-out.
- Ring counter.



Counter

- A Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter a counter increases count for every rising edge of clock. Not only counting, a counter can follow the certain sequence based on our design like any random sequence 0,1,3,2… .They can also be designed with the help of flip flops. They are used as frequency dividers where the frequency of given pulse waveform is divided. Counters are sequential circuit that count the number of pulses can be either in binary code or BCD form. The main properties of a counter are timing , sequencing , and counting. Counter works in two modes
- Up counter
- Down counter

Counter Classification

Counters are broadly divided into two categories

- Asynchronous counter
- Synchronous counter

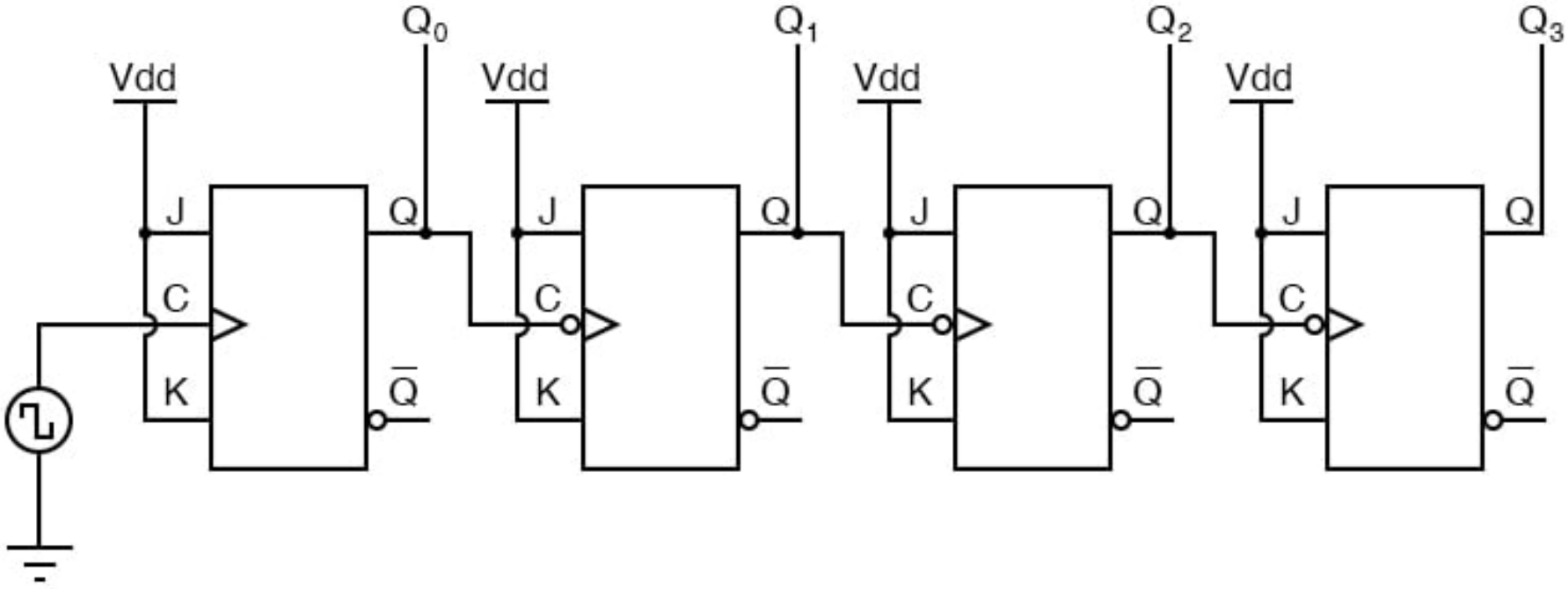
1. **Asynchronous Counter**

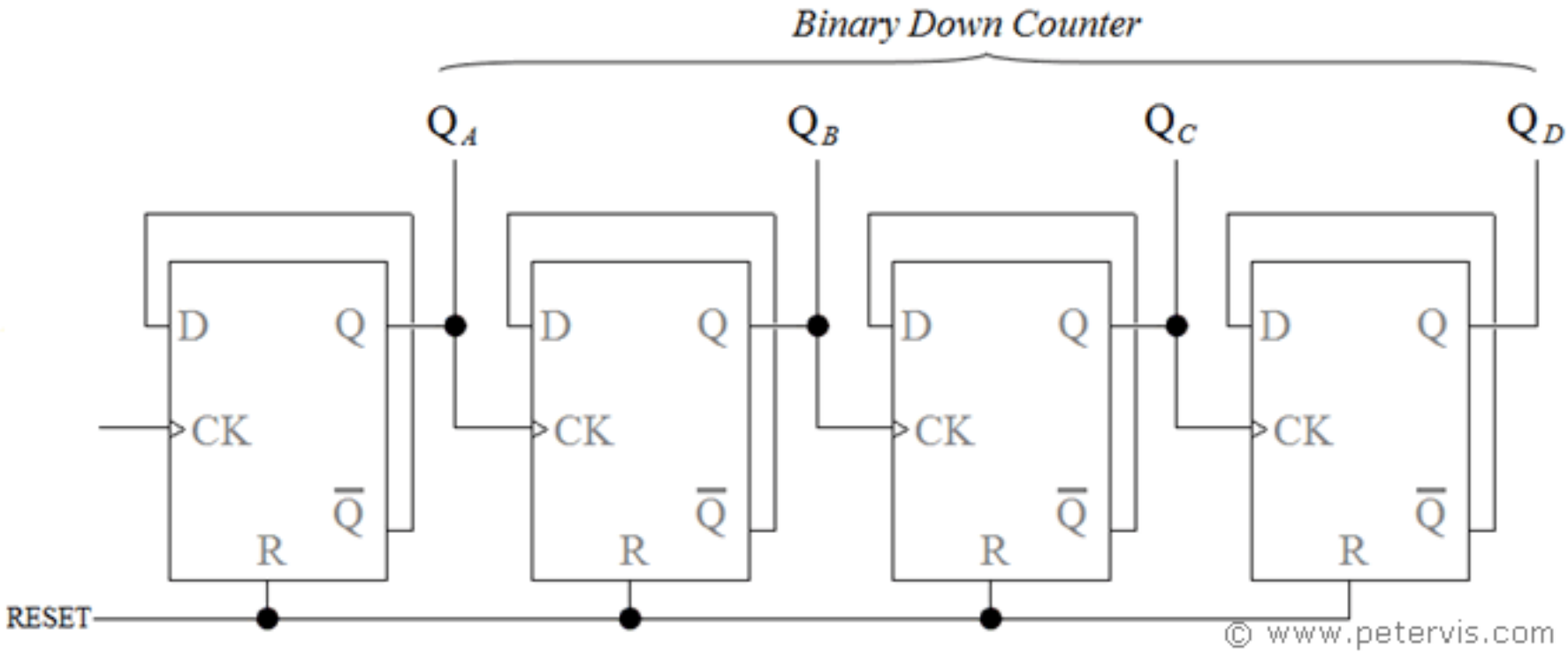
In asynchronous counter we don’t use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops.

Synchronous Counter

Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop. It is also called as parallel counter.

A four-bit “up” counter




Binary Down Counter
Q_A
Q_B
Q_C
Q_D
D
Q
CK
$\overline{Q}$
R
RESET
© www.petervis.com

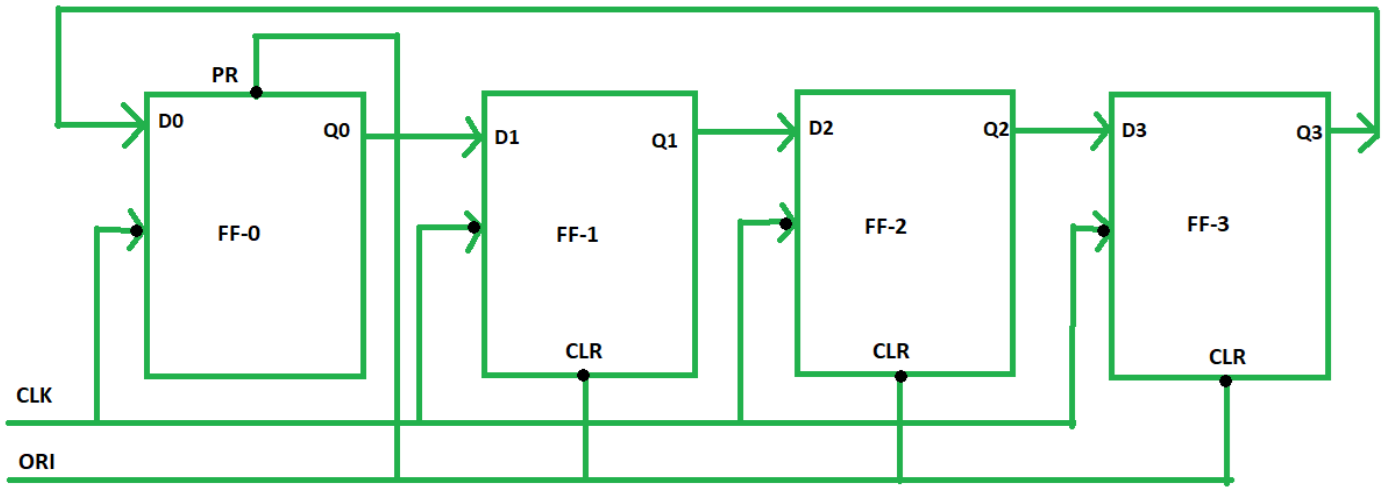
- An up/down counter (UDC) in digital circuits counts upward from a starting value and downward from an initial value. The direction of counting is determined by the control input or by using separate "up" and "down" clocks.

Ring Counter

A ring counter is a typical application of the Shift register. The ring counter is almost the same as the shift counter. The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring counter but in the case of the shift register it is taken as output. Except for this, all the other things are the same.

```
No. of states in Ring counter = No. of flip-flop used
```

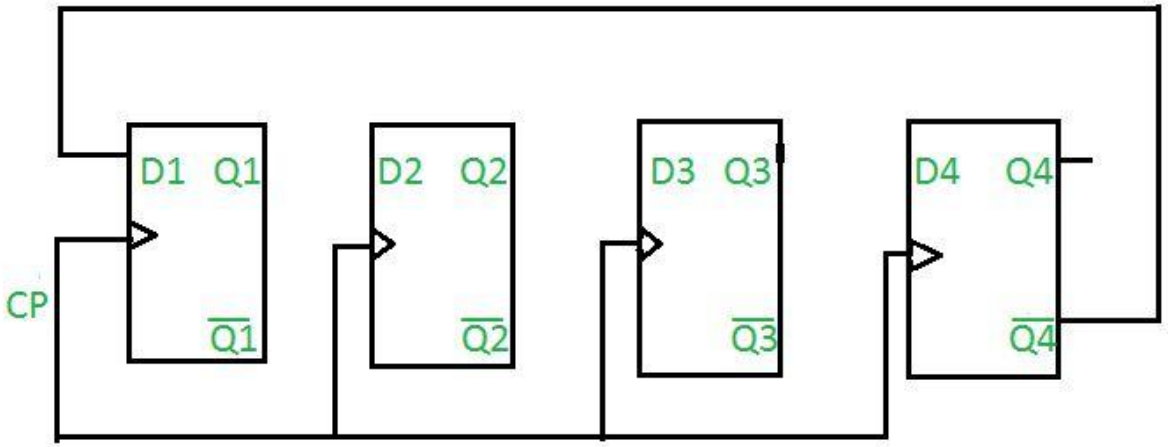
So, for designing a 4-bit Ring counter we need 4 flip-flops.



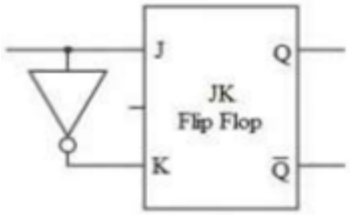
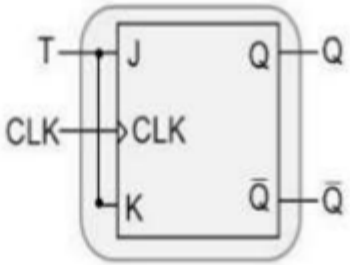
Ring Counter

Johnson Counter

- A Johnson counter is a type of a synchronous counter with a special counting pattern. It operates by the complemented output of the last flip flop feed back into the input of the first flip flop.



ıte between D FF and T FF.	4M

		4M
ıt is transferred after a delay	When T=1, output toggles	
Used in shift registers	Used in counters, frequency dividers	
D Qn+1 0 0	T Qn+1 0 Qn	

Practice Question

Combinational, Sequential circuit difference

Draw SR, JK, D, T ff and its excitation table

Register

Buffer and Shift Registers.(Diagrams and Difference)

Counters

Synhronous and asynchronous counter.

UP, DOWN, RING, JOHNSONS (Diagrams and 3 4 points to remember)