# Memory Management Techniques

## Types

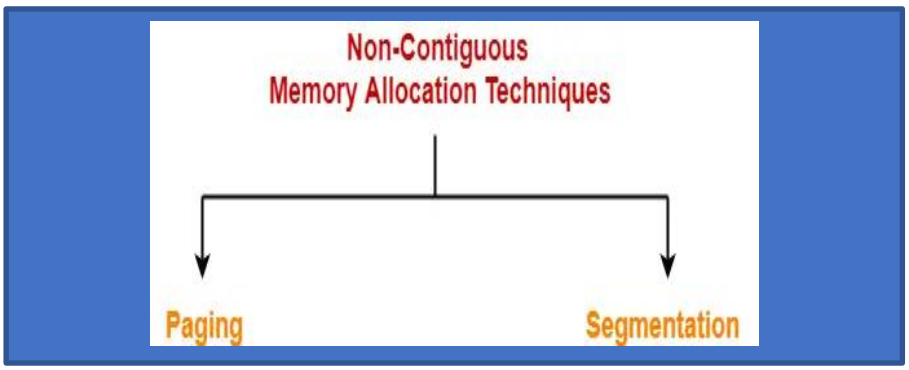
: There are two types of Memory Management Techniques

1)Contiguous 2) Non-Contiguous

**Contiguous :** Contiguous memory allocation means assigning continuous blocks of memory to the process

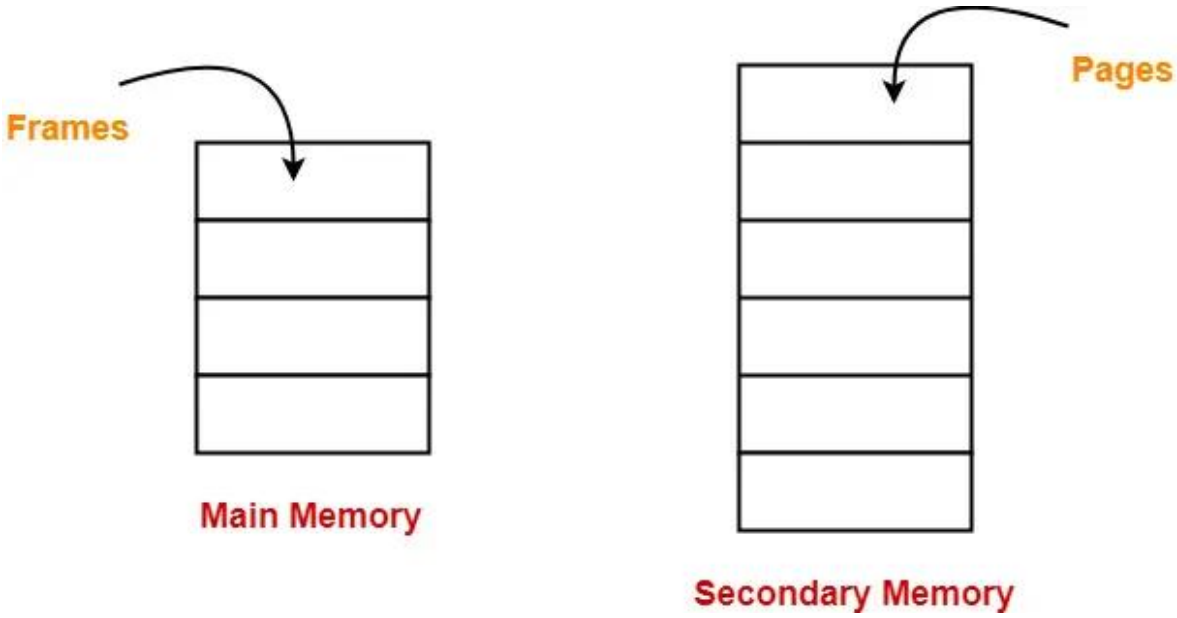
## Non-Contiguous Memory Allocation

- Non-contiguous memory allocation is a memory allocation technique.
- It allows to store parts of a single process in a non-contiguous fashion.
- Thus, different parts of the same process can be stored at different places in the main memory.




## Paging-

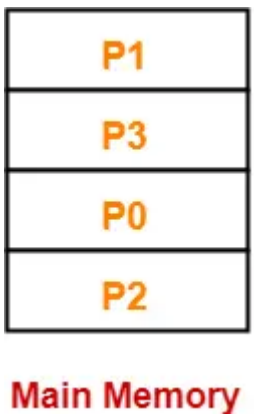
- Paging is a fixed size partitioning scheme.
- In paging, secondary memory and main memory are divided into equal fixed size partitions(blocks).
- The partitions of secondary memory are called as **pages**.
- The partitions of main memory are called as **frames**.




- Each process is divided into parts where size of each part is same as page size.
- The size of the last part may be less than the page size.
- The pages of process are stored in the frames of main memory depending upon their availability.

## Example-

- Consider a process is divided into 4 pages $P_0$, $P_1$, $P_2$and $P_3$.
- Depending upon the availability, these pages may be stored in the main memory frames in a non-contiguous fashion as shown-




## Translating Logical Address into Physical Address-

1. When CPU needs some instruction to execute , it request for that, but CPU doesnot know where it is located in main memory, so it will generate the logical address.

2.Therefore there is a need to map the logical address to physical address , this mapping is done with the help of MMU(Memory Management Unit).

3. CPU always generates a logical address.
4. A physical address is needed to access the main memory.

For this mapping , Every process needs to maintain page table. Page table contains the information of Page No with its respective frame number. Page number acts like an index.

Consider A process size = 4B
Page size =2 B

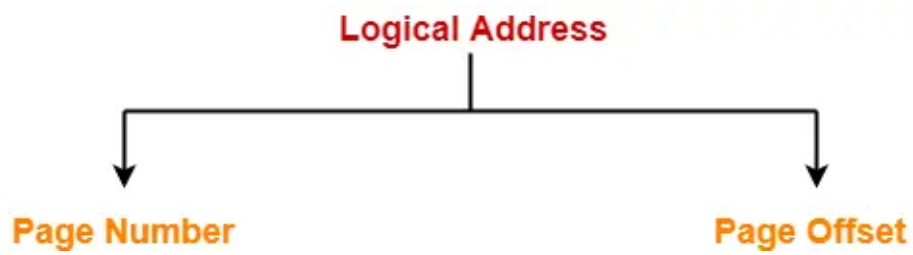
| • **Page No.** | • **Frame No.** |
|---|---|
| • **0** | • **F2** |
| • **1** | • **F4** |
| • | |

Following steps are followed to translate logical address into physical address-

## Step-01:

CPU generates a logical address consisting of two parts-

1. Page Number
2. Page Offset




- Page Number specifies the specific page of the process from which CPU wants to read the data.
- Page Offset specifies the specific word on the page that CPU wants to read.

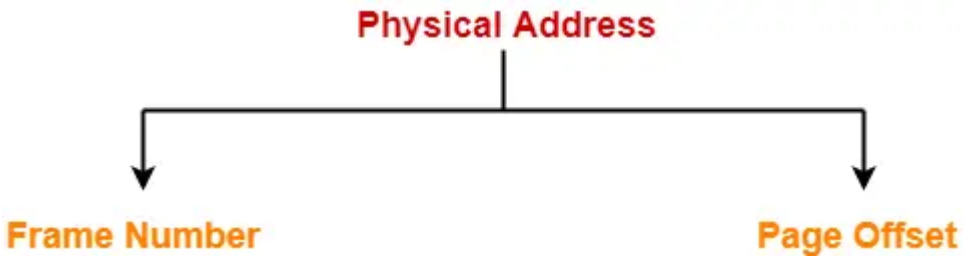
## Step-02:

For the page number generated by the CPU,

- **Page Table**provides the corresponding frame number (base address of the frame) where that page is stored in the main memory.

## Step-03:

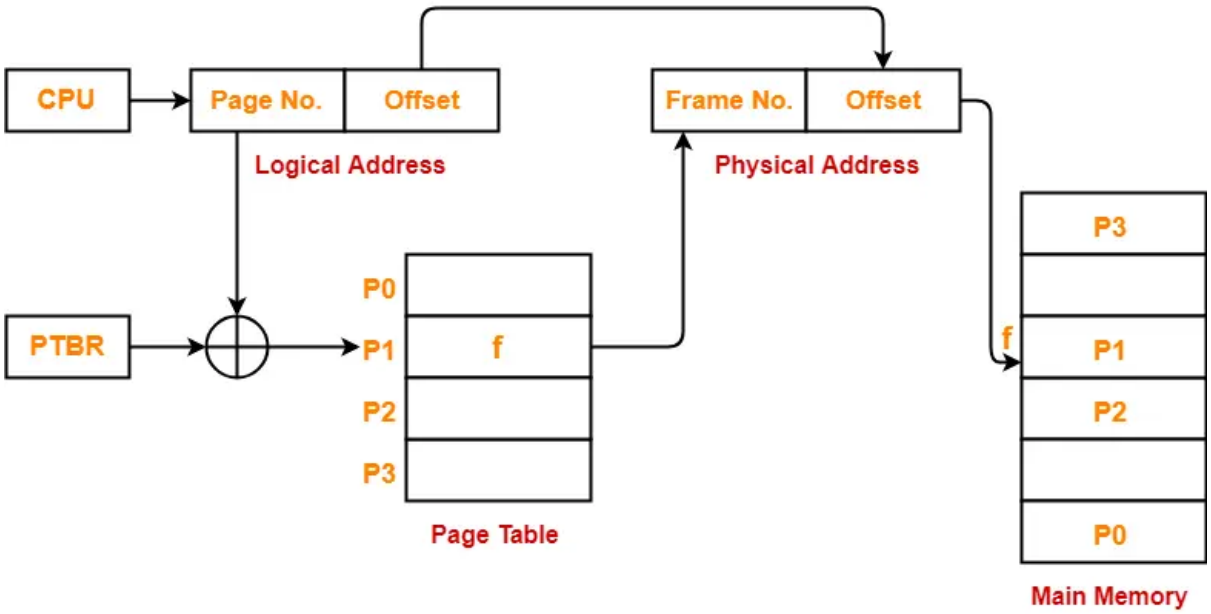
- The frame number combined with the page offset forms the required physical address.




- Frame number specifies the specific frame where the required page is stored.
- Page Offset specifies the specific word that has to be read from that page.

## Diagram-

The following diagram illustrates the above steps of translating logical address into physical address-




Translating Logical Address into Physical Address

## Advantages-

The advantages of paging are-

- It allows to store parts of a single process in a non-contiguous fashion.
- It solves the problem of external fragmentation.

## Disadvantages-

The disadvantages of paging are-

- It suffers from internal fragmentation.
- There is an overhead of maintaining a page table for each process.

**(Note: In class , It is explained how to generate physical address with example, refer that example here, it is expected to writ it here)**

### Translation Look aside Buffer(TLB):

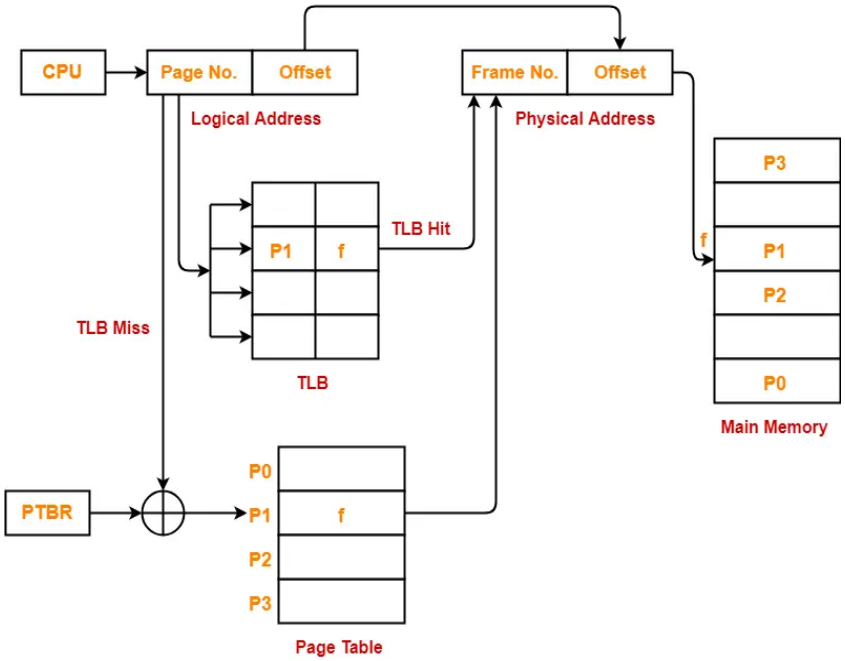
1.Every process needs to maintain page table.

2.In earlier architecture the page table was maintained by registers which was capable to maintain only few entries.

3.As the Size of RAM increases, it is possible to store more no. Of processes in the RAM which need more space to store page table and hence registerw werenot capable to store large entries of page table.

4. Hence , Page table get stored in the main memory, in this approach there are two memory access to the main memory , one access is for page table and another one is for accessing the particular page.

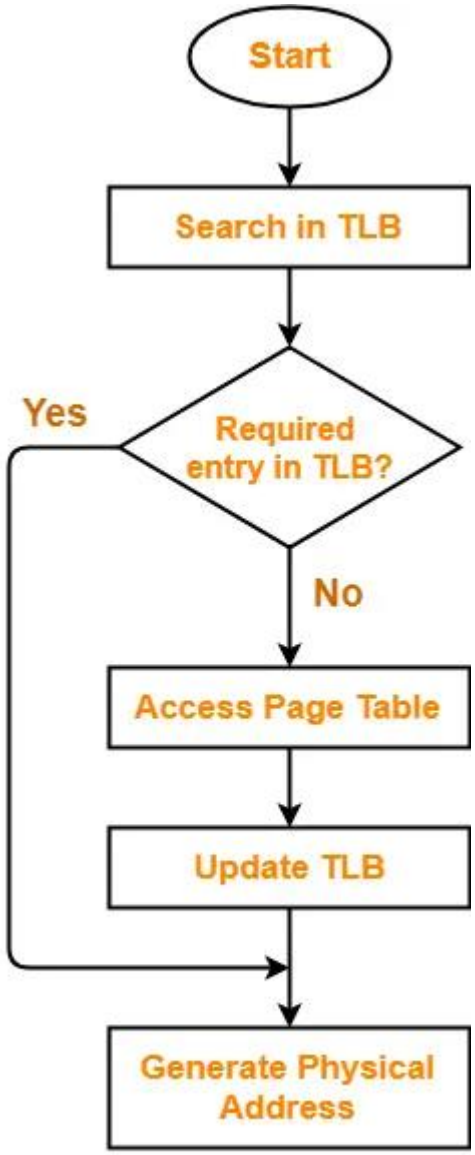
5.To overcome this overhead, cache storage is allocate to store some entries of pages from page table called as TLB (**Translation Look aside buffer**) and rest of the page entries are maintained in page table in main memory itself.




Translating Logical Address into Physical Address

# Flowchart-

The following flowchart illustrates the above steps of translating logical address into physical address-




Flowchart

**Point-01:**

- Unlike page table, there exists only one TLB in the system.
- So, whenever context switching occurs, the entire content of TLB is flushed and deleted.
- TLB is then again updated with the currently running process.

**Point-02:**

When a new process gets scheduled-

- Initially, TLB is empty. So, TLB misses are frequent.
- With every access from the page table, TLB is updated.
- After some time, TLB hits increases and TLB misses reduces.

**Point-03:**

- The time taken to update TLB after getting the frame number from the page table is negligible.
- Also, TLB is updated in parallel while fetching the word from the main memory.

## Advantages-

The advantages of using TLB are-

- TLB reduces the effective access time.
- Only one memory access is required when TLB hit occurs.

## Disadvantages-

A major disadvantage of using TLB is-

- After some time of running the process, when TLB hits increases and process starts to run smoothly, a context switching occurs.
- The entire content of the TLB is flushed.
- Then, TLB is again updated with the currently running process.This happens again and again.

Other disadvantages are-

- TLB can hold the data of only one process at a time.
- When context switches occur frequently, the performance of TLB degrades due to low hit ratio.
- As it is a special hardware, it involves additional cost.

# Segmentation:

Like Paging, Segmentation is another non-contiguous memory allocation technique.

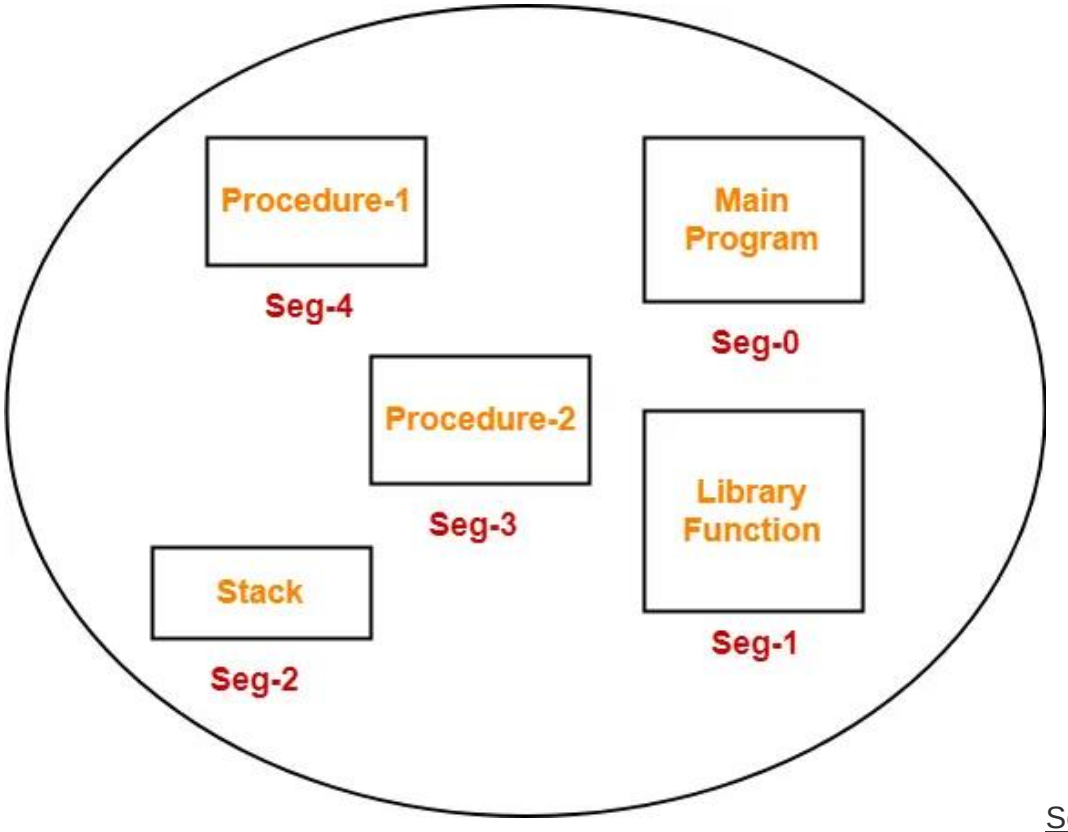
- In segmentation, process is not divided blindly into fixed size pages.
- Rather, the process is divided into modules for better visualization.

# Segmentation is a variable size partitioning scheme.

- In segmentation, secondary memory and main memory are divided into partitions of unequal size.
- The size of partitions depend on the length of modules.
- The partitions of secondary memory are called as **segments**.

## Example-

Consider a program is divided into 5 segments as-




Segment Table-

- Segment table is a table that stores the information about each segment of the process.
- It has two columns.
- First columnstores the size or length of the segment.
- Second column stores the base address or starting address of the segment in the main memory.
- Segment table is stored as a separate segment in the main memory.
- Segment table base register (STBR) stores the base address of the segment table.

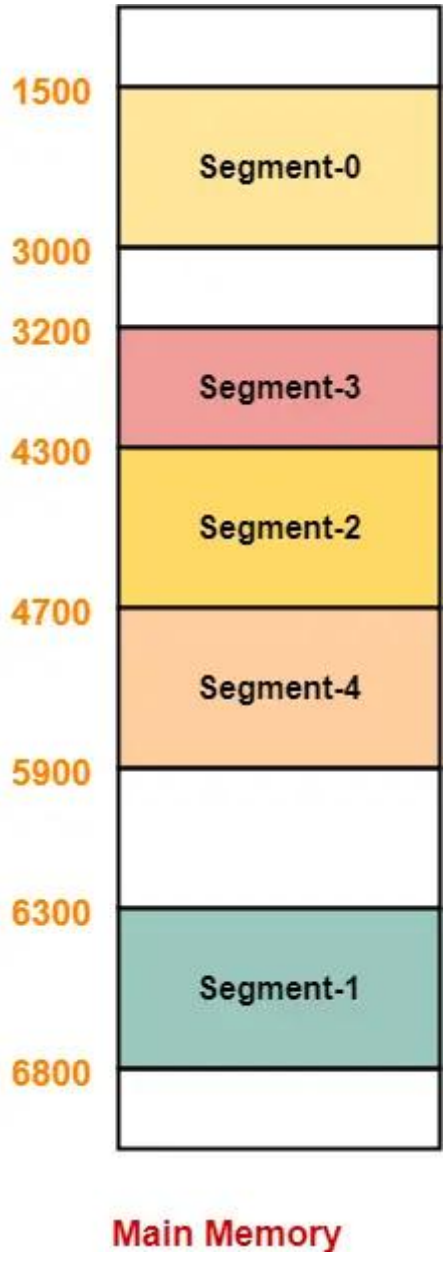
Consider the following segment table

| | Limit | Base |
|---|---|---|
| Seg-0 | 1500 | 1500 |
| Seg-1 | 500 | 6300 |
| Seg-2 | 400 | 4300 |
| Seg-3 | 1100 | 3200 |
| Seg-4 | 1200 | 4700 |

Segment Table

- in above Limit indicates the length or size of the segment.
- Base indicates the base address or starting address of the segment in the main memory.

In accordance to the above segment table, the segments are stored in the main memory as-




## Translating Logical Address into Physical Address in

# Segmentation

- CPU always generates a logical address.
- A physical address is needed to access the main memory.

Following steps are followed to translate logical address into physical address-

# Step-01:

CPU generates a logical address consisting of two parts-

1. Segment Number
2. Segment Offset

Segment Numberspecifies the specific segment of the process from which CPU wants to read the data. Segment Offset specifies the specific word in the segment that CPU wants to read.

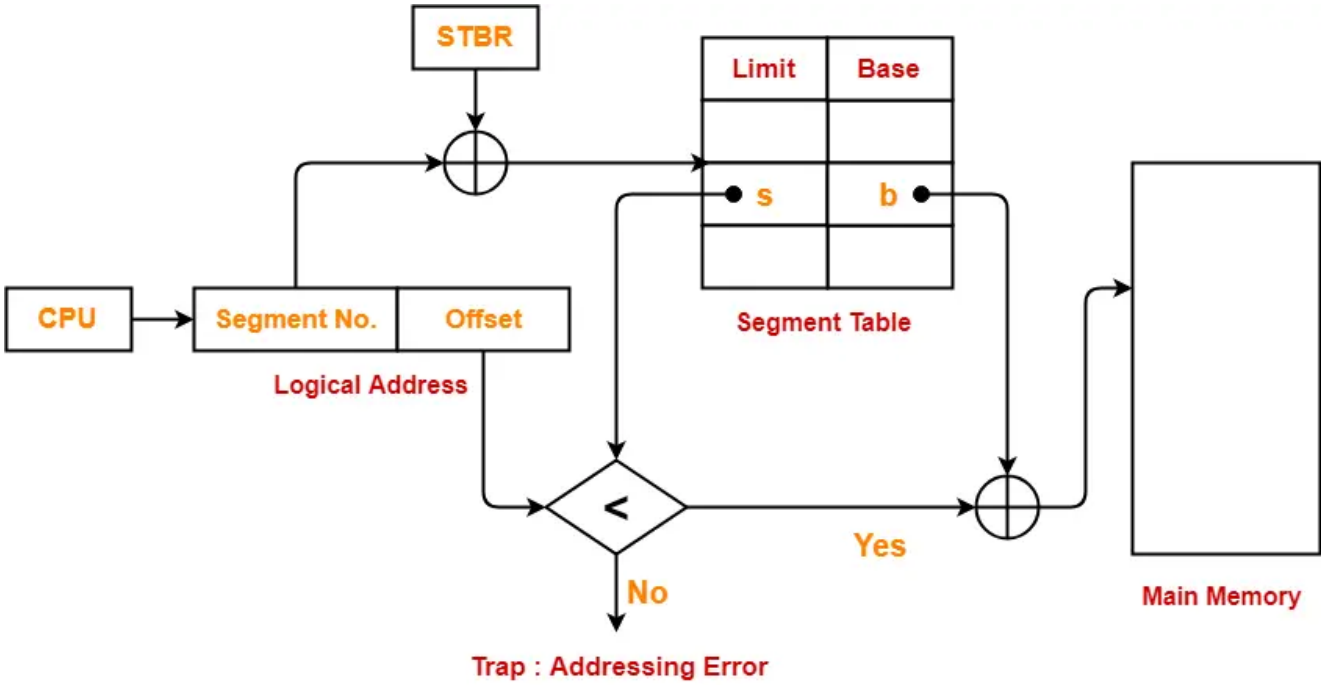
# Step-02:

For the generated segment number, corresponding entry is located in the segment table.

- Then, segment offset is compared with the limit (size) of the segment.

# Diagram-

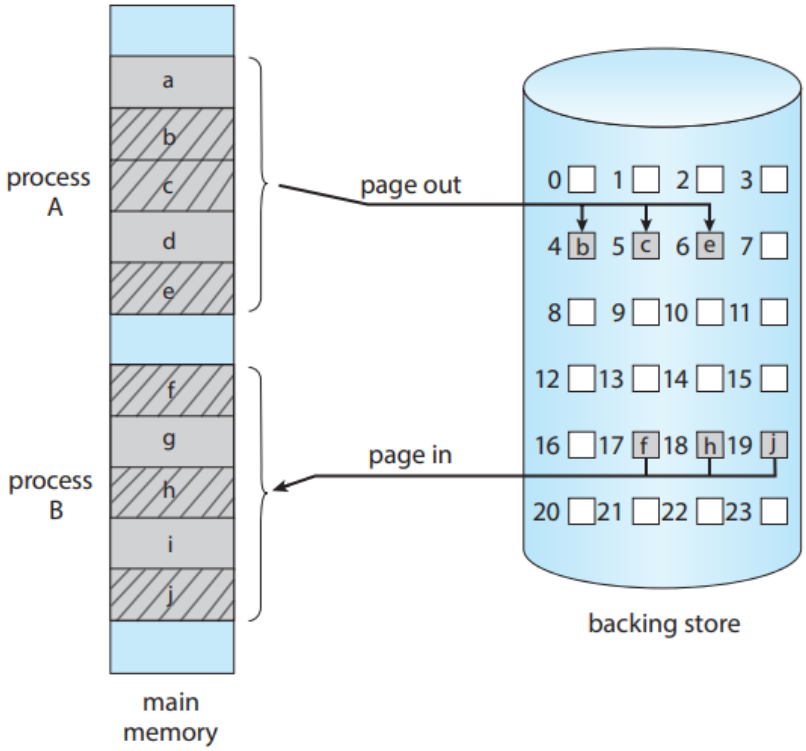
The following diagram illustrates the above steps of translating logical address into physical address-




Translating Logical Address into Physical Address

## Virtual Memory

1. Virtual Memory is a storage allocation scheme in which secondary memory can be addressed as though it were part of the main memory.
2. provides user an illusion of having a very big main memory.
3. whenever some pages needs to be loaded in the main memory for the execution and the memory is not available for those many pages, then in that case, instead of stopping the pages from entering in the main memory, the OS search for the RAM area that are least used in the recent times or that are not referenced and copy that into the secondary memory to make the space for the new pages in the main memory.
4. This procedure happens automatically with the help of MMU (Memory Management Unit), therefore it makes the computer feel like it is having the unlimited RAM.




## Demand Paging

Demand Paging is a popular method of virtual memory management. In demand paging, the pages of a process which are least used, get stored in the secondary memory.A page is copied to the main memory when its demand is made or page fault occurs.

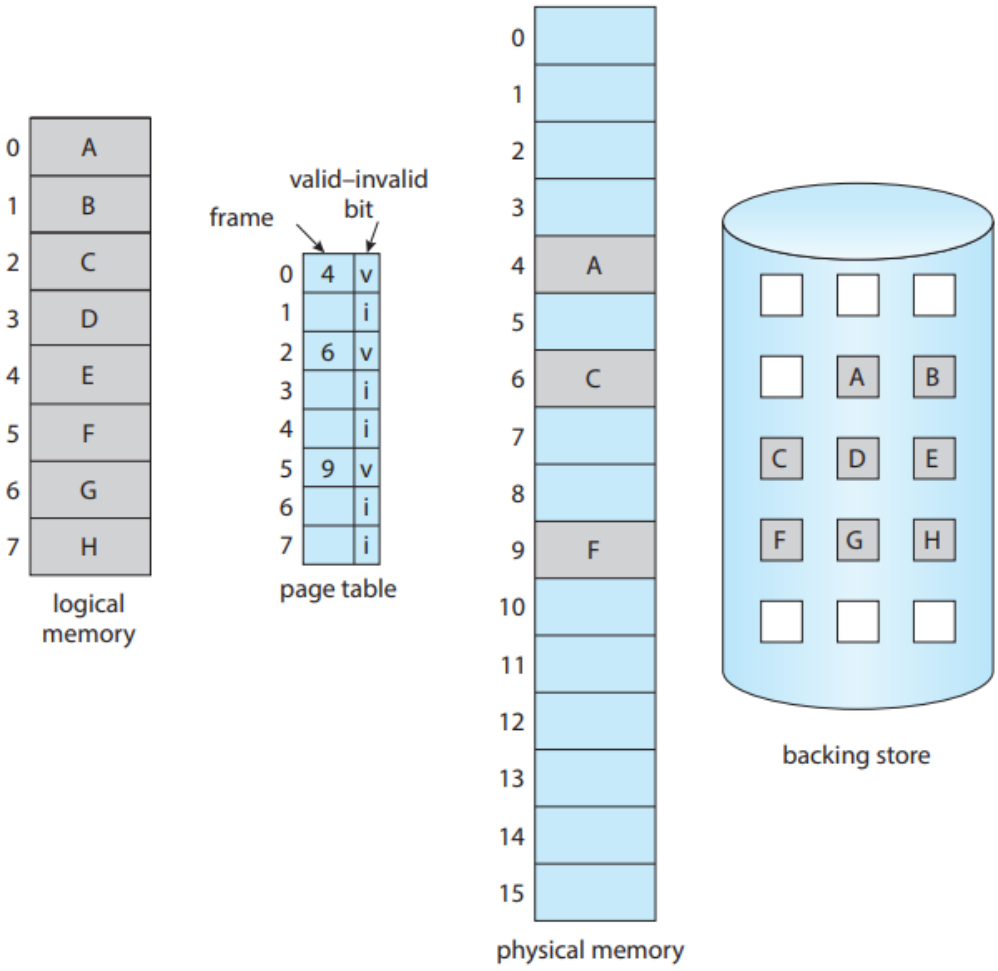
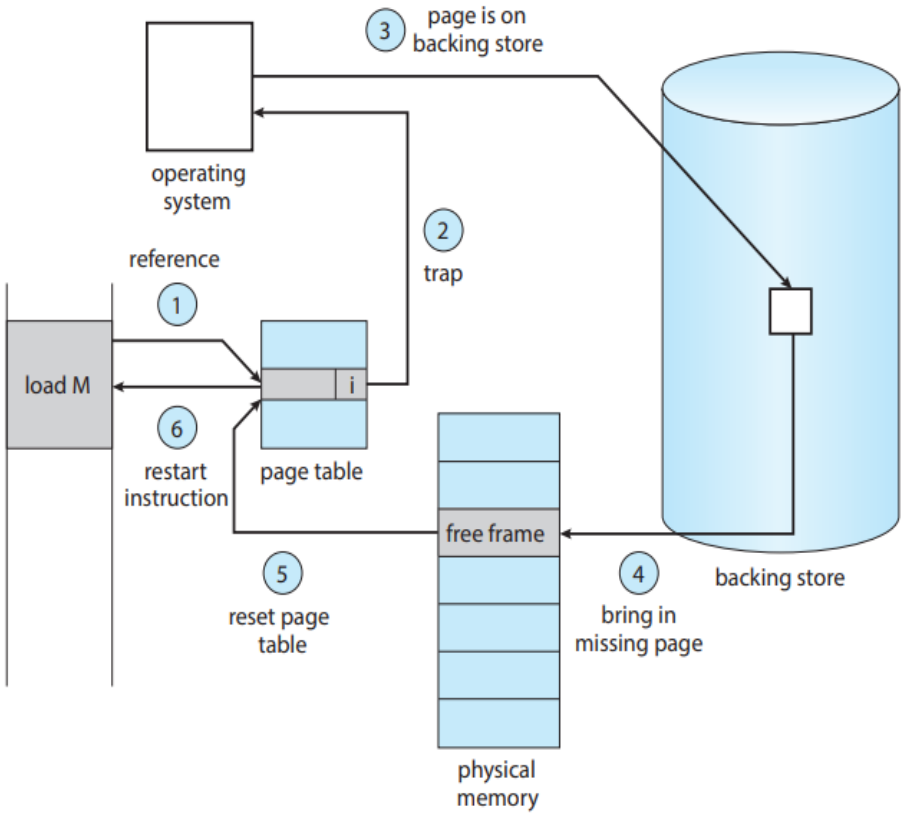



Fig. Page table when some pages are not in main memory




## Advantages of Virtual Memory

1. The degree of Multiprogramming will be increased.
2. User can run large application with less real RAM.
3. There is no need to buy more memory RAMs.

## Disadvantages of Virtual Memory

1. The system becomes slower since swapping takes time.
2. It takes more time in switching between applications.
3. The user will have the lesser hard disk space for its use.

# Page Replacement

Page replacement is a mechanism of freeing up a frame that can be allocated to the process requesting it.

*Numericals on Page Replacement has been practiced in class.