EXPERIMENT NO: 10

Aim: - Implementation and Verification De-Multiplexer using Logic Gates.

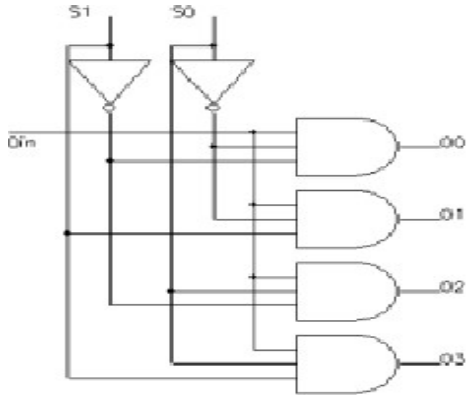
APPARATUS REQUIRED: Digital Trainer kit, IC 7447, IC 74139 and connecting Connector.

THEORY:

DEMULTIPLEXER: Demultiplexer means generally one into many. A demultiplexer is a logic circuit with one input and many outputs. By applying control signals, we can steer the input signal to one of the output lines. The circuit. has one input signal, m control signal and n output signals. Where $2^n = m$. It functions as an electronic switch to route an incoming data signal to one of several outputs.

LOGIC DIAGRAM:

1:4 Demux



PROCEDURE:

1) Connect the circuit as shown in figure.
2) Apply Vcc & ground signal to every IC.
3) Observe the input & output according to the truth table.

Truth table for Demux

Output select Lines		Output selected
S_1	S_0	
0	0	O_0
0	1	O_1
1	0	O_2
1	1	O_3

RESULT: De-multiplexer have been studied and verified.

EXPERIMENT NO: 3

Aim: Verification of State Tables of Rs, J-k, T and D Flip-Flops using NAND & NOR Gates

APPARATUS REQUIRED: IC' S 7400, 7402 Digital Trainer & Connecting leads.

THEORY:

- **RS FLIP-FLOP:** There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. When I/Ps R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

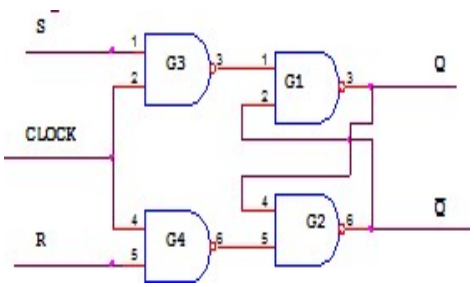
- **JK FLIP-FLOP**: For counting, the JK flip-flop is the ideal element to use. The variables J and K are called control I/Ps because they determine what the flip-flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disabled and Q retains its last value.

- **D FLIP –FLOP**: This kind of flip flop prevents the value of D from reaching the Q output until clock pulses occur. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

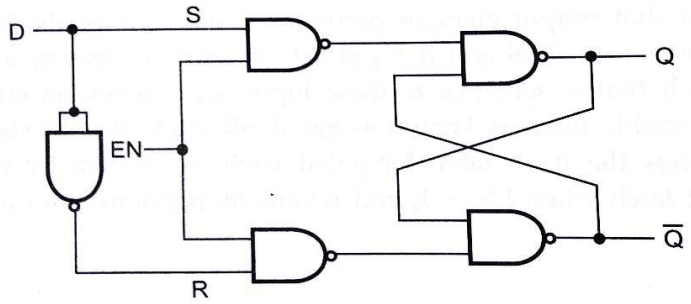
- **T FLIP-FLOP**: The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

CIRCUIT DIAGRAM:

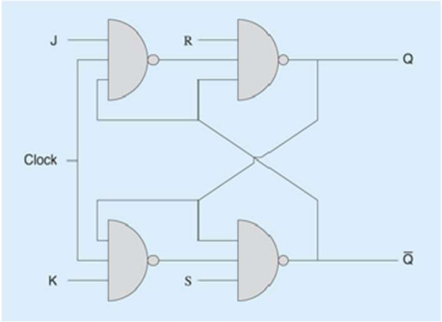
SR Flip Flop



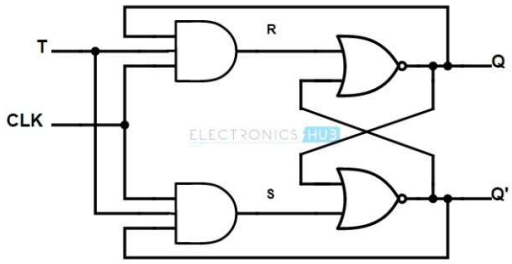
D Flip Flop



JK Flip Flop



T Flip Flop



PROCEDURE:

1. Connect the circuit as shown in figure.
2. Apply Vcc & ground signal to every IC.
3. Observe the input & output according to the truth table.

TRUTH TABLE:
SR FLIP FLOP:

CLOCK	S	R	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	?

D FLIPFLOP:

INPUT	OUTPUT
0	0
1	1

JK FLIPFLOP

CLOCK	S	R	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	Qn’

T FLIPFLOP

CLOCK	S	R	Q_{n+1}
1	0	1	NO CHANGE
1	1	0	Qn’

RESULT: Truth table is verified on digital trainer.