

# SIYANG CHEN

Sun Yat-sen University ◊ Microelectronic Science and Engineering  
School of Electronics and Information Technology  
Phone: (+86) 157-6788-9072 ◊ Email: chensy298@mail2.sysu.edu.cn

## EDUCATION

<b>Sun Yat-sen University (SYSU)</b> B.E. in Microelectronics Science and Engineering <b>Rank: 5/104 (Top 5%), GPA: 4.0/4.0 (4.12/5.0)</b> , Average Score: 91.2, CET-6: 621 Outstanding academic performance in Engineering Circuit Analysis, Digital Circuits and Logical Design, Analog Circuits, High Frequency Circuits, Semiconductor Device Physics, Hardware Description Language and FPGA Design, ... (Top 5 in core courses)	Sep 2022 - Jul 2026(expected)
---	-------------------------------

## RESEARCH EXPERIENCE

<b>Cell Generator: Automated Custom Design of Digital Standard Cells</b> <b>(Principal Investigator)</b> <i>Supervisors: Prof. Xiangyu Meng</i>	Sep 2024 - Jan 2025 SYSU
· Objective: Develop an EDA tool to enable user-defined standard cell dimensions for resolving the limited diversity in standard cell libraries and optimizing circuit performance · Methodology: Identification + Modification. Identify transistors in the provided layout and modify the width of specified transistors based on input information · Outcome: Successfully developed an EDA tool to achieve automated generation of standard cell layouts for all logic gates and D flip-flops · Contributions: Designed data structures, developed transistor identification modules, and optimized code for layout replication	

### Transformer-Based Automatic Inductor Layout Generation

<b>(Principal Investigator)</b> <i>Supervisors: Prof. Xiangyu Meng</i>	Dec 2023 - Dec 2024 SYSU
· Objective: Streamline inductor layout iteration by predicting metal block movement(annotated with labels) using deep learning · Methodology: Modeled metal blocks as text sequences and trained a Transformer on annotated inductor layout datasets · Outcome: The model achieves prediction of labels for any metal block in the inductor layout, average accuracy: 97% · Contributions: Designed the embedding layer of model, alongside comprehensive coding of the entire model architecture	

## AWARDS

<b>National Scholarship</b>	2024 - 2025
<b>Zhentai Donation Scholarship</b>	2022 - 2023
Sun Yat-sen University Scholarship*3	2022 - 2025
First Prize, National IC Innovation Competition (South China Division)	Jul 2025

## SKILLS

<b>Software Languages</b>	Python, C, C++
<b>Hardware Languages</b>	Verilog
<b>Frameworks</b>	Xilinx Vivado, PyTorch, LaTeX