1-1. Example: Use a button to control one LED light

Use the given FPGA development board to implement a circuit that uses a button to control one LED light:

- When the button is pressed, the light is on.
- When the button is not pressed, the light is off.

Requirements:

1. Follow "How to build a new project in Quartus II.pdf", "How to write and add RTL codes in project.pdf", "How to write the testbench code.pdf", "How to plan pins.pdf", and "How to download designs.pdf" to build the required circuit and finish the simulation.
2. You do NOT need to include this example in your report.

1-2. Example: 2-to-1 Multiplexer

Use the given FPGA development board to implement a 2-to-1 multiplexer. This multiplexer contains

- 2 buttons as 2 individual inputs;
- 1 button as the selection input;
- 1 LED as the output.

Requirements:

1. Write the Verilog codes to build the required circuit.
2. Do the simulation to verify whether your designs and codes satisfy the required functions.
3. Test your designs in the development board.
4. You do NOT need to include this example in your report.

1-3. Example: 3-8 Line Decoder

Use the given FPGA development board to implement a 3-8 line decider. This decoder contains

- 3 individual inputs: 3 inputs denote 3 bits of the natural binary number.
- 8 outputs: One bit is high, which is determined by the input binary number. Other bits are low. The lowest bit denotes 0.

You do NOT need to test your designs in the development board.

Requirements:

1. Write the Verilog codes to build the required circuit.
2. Do the simulation to verify whether your designs and codes satisfy the required functions.
3. You do NOT need to test your designs in the development board.
4. You do NOT need to include this example in your report.

1-4. Example: Half Adder

Use the given FPGA development board to implement a half adder. This half adder contains

- 2 buttons as 2 individual inputs;
- 1 LED as the carry-on bit output;
- 1 LED as the sum bit output

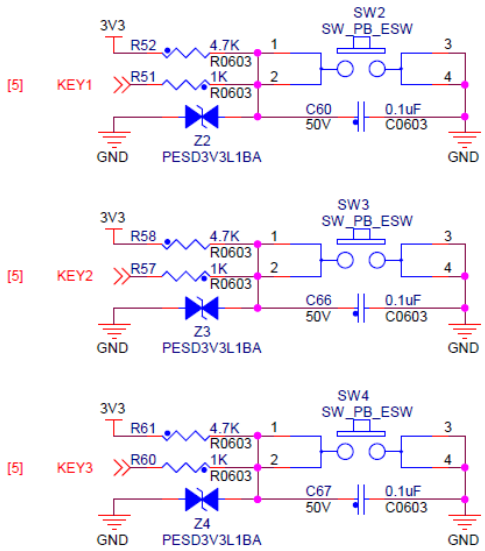
Requirements:

1. Write the Verilog codes to build the required circuit.
2. Do the simulation to verify whether your designs and codes satisfy the required functions.
3. You do NOT need to include this example in your report.

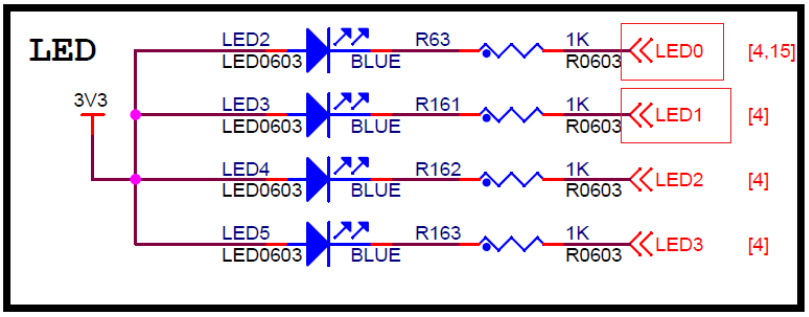
1-5. Full-Adder

Use the given FPGA development board to implement a full adder. This full adder contains

- 3 buttons as 3 individual inputs:
  - Use KEY1 in the development board as the 1st input, which is the addend
  - Use KEY2 in the development board as the 2nd input, which is the augend
  - Use KEY3 in the development board as the 3rd input, which is the carry-on bit from the lower bit



- Use LED1 in the development board as the carry-on bit output.
- Use LED0 in the development board as the sum bit output:



You may refer the page 53 of Review-1.pptx to review what is the full adder.

Requirements:

1. Write the Verilog codes to build the required circuit.
2. Do the simulation to verify whether your designs and codes satisfy the required functions.

3. Test your designs in the development board.

1. You need to include this example in your report. In your report, you need to include:
    a) Introduction:
        i. Introduce the background. For example, you can introduce
            - what is the full adder,
            - the key differences between the half adder and the full adder,
            - …
        ii. Purpose of the experiment
        iii. Brief introduce your designs and key results
        iv. Contributions of your group members
        v. …
    b) Materials and Methods: Show your FPGA solution. You need to show
        i. your designed structure block diagram,
        ii. your designed truth table,
        iii. your designed signal waveforms,
        iv. which devices or resources in this development board you used,
        v. …
    c) Results: Show your simulation and corresponding test results. You need to show
        i. how you build the testbench,
        ii. the testing inputs,
        iii. the expected outputs,
        iv. the actual outputs,
        v. the differences between the expected outputs and the actual outputs,
        vi. the expected values, actual values, and their differences of the important internal variables
        vii. test results in the development board
        viii. …
    d) Discussions. This part is not essential, but you can show:
        i. If you find any bugs or problems that you can not solve in the given time, you can discuss them and show your possible solutions.
        ii. If you find any interesting results, you can discuss them.
        iii. …
    e) Conclusion. You need to
        i. summarize all your designs and simulation results,

ii. summarize the key discussion results if you have,

iii. …

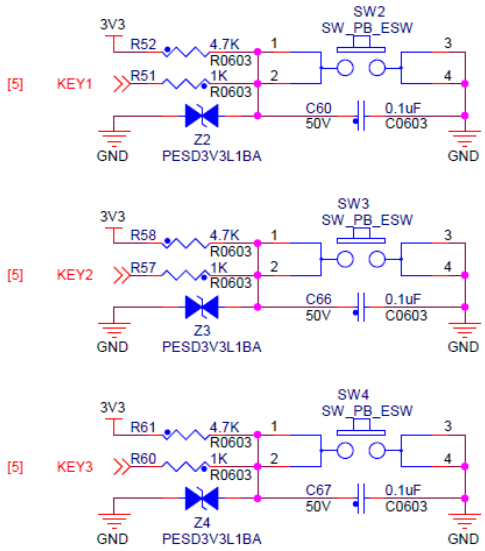
f) References. This is a list of all the sources cited in the report, formatted according to a specific citation style. You need to use the IEEE reference format (http://journals.ieeeauthorcenter.ieee.org/wp-content/uploads/sites/7/IEEE_Reference_Guide.pdf).

g) Appendices. This optional section can include codes, raw data, calculations, additional graphs, and other supplementary material that is relevant but not essential to the main report.

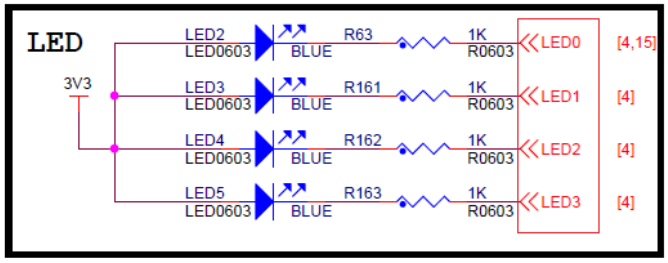
1-6. 2-4 Line Decoder

Use the given FPGA development board to implement a 2-4 line decoder. This decoder contains

- 3 buttons:
  - Use KEY2 as the 1st input of this decoder
  - Use KEY3 as the 2nd input of this decoder
  - Use KEY1 in the development board as the enable input



- Use LED3, LED2, LED1, and LED0 as 4 outputs of this decoder. The LED3 is the highest bit. The LED0 is the lowest bit.



You may refer the page 55 of Review-1.pptx to review what is the 2-4 line decoder

Requirements:

1. Write the Verilog codes to build the required circuit.
2. Do the simulation to verify whether your designs and codes satisfy the required functions.
3. Test your designs in the development board.

2. You need to include this example in your report. In your report, you need to include:
    a) Introduction:
        i. Purpose of the experiment
        ii. Brief introduce your designs and key results
        iii. Contributions of your group members
        iv. …
    b) Materials and Methods: Show your FPGA solution. You need to show
        i. your designed structure block diagram,
        ii. your designed truth table,
        iii. your designed signal waveforms,
        iv. which devices or resources in this development board you used,
        v. …
    c) Results: Show your simulation and corresponding test results. You need to show
        i. how you build the testbench,
        ii. the testing inputs,
        iii. the expected outputs,
        iv. the actual outputs,
        v. the differences between the expected outputs and the actual outputs,
        vi. the expected values, actual values, and their differences of the important internal variables
        vii. test results in the development board
        viii. …
    d) Discussions. This part is not essential, but you can show:
        i. If you find any bugs or problems that you can not solve in the given time, you can discuss them and show your possible solutions.
        ii. If you find any interesting results, you can discuss them.
        iii. …
    e) Conclusion. You need to
        i. summarize all your designs and simulation results,
        ii. summarize the key discussion results if you have,
        iii. …
    f) References. This is a list of all the sources cited in the report, formatted according to a specific citation style. You need to use the IEEE reference format (http://journals.ieeeauthorcenter.ieee.org/wp-

content/uploads/sites/7/IEEE_Reference_Guide.pdf).

g) Appendices. This optional section can include codes, raw data, calculations, additional graphs, and other supplementary material that is relevant but not essential to the main report.

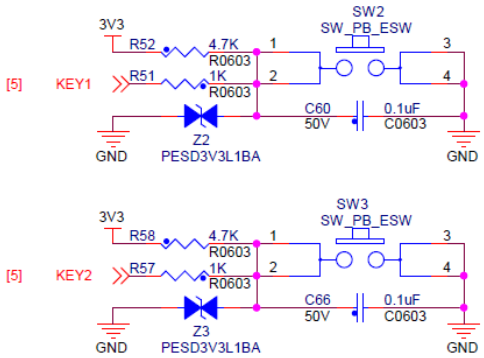
1-7. One-bit Digital Comparator

Use the given FPGA development board to implement a one-bit digital comparator that uses 2 buttons as inputs and 3 LED lights as outputs. Suppose that 2 inputs are A and B, 3 outputs follow:

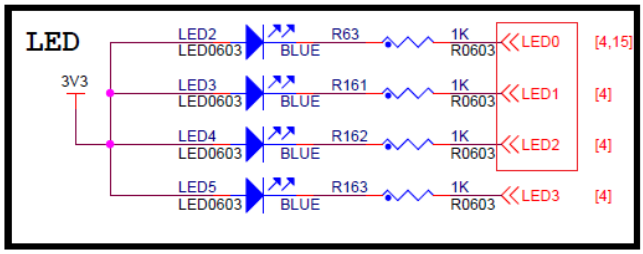
- When A<B, only the 1st output is turned on, and other outputs are turned off.
- When A=B, only the 2nd output is turned on, and other outputs are turned off.
- When A>B, only the 3rd output is turned on, and other outputs are turned off.

You need to

- Use KEY1 in the development board as the input A
- Use KEY2 in the development board as the input B



- Use LED0 in the development board as the 1st output
- Use LED1 in the development board as the 2nd output
- Use LED2 in the development board as the 3rd output



Requirements:

4. Write the Verilog codes to build the required circuit.
5. Do the simulation to verify whether your designs and codes satisfy the required functions.

6. Test your designs in the development board.
3. You need to include this example in your report. In your report, you need to include:
    a) Introduction:
        i. Purpose of the experiment
        ii. Brief introduce your designs and key results
        iii. Contributions of your group members
        iv. …
    b) Materials and Methods: Show your FPGA solution. You need to show
        i. your designed structure block diagram,
        ii. your designed truth table,
        iii. your designed signal waveforms,
        iv. which devices or resources in this development board you used,
        v. …
    c) Results: Show your simulation and corresponding test results. You need to show
        i. how you build the testbench,
        ii. the testing inputs,
        iii. the expected outputs,
        iv. the actual outputs,
        v. the differences between the expected outputs and the actual outputs,
        vi. the expected values, actual values, and their differences of the important internal variables
        vii. test results in the development board
        viii. …
    d) Discussions. This part is not essential, but you can show:
        i. If you find any bugs or problems that you can not solve in the given time, you can discuss them and show your possible solutions.
        ii. If you find any interesting results, you can discuss them.
        iii. …
    e) Conclusion. You need to
        i. summarize all your designs and simulation results,
        ii. summarize the key discussion results if you have,
        iii. …
    f) References. This is a list of all the sources cited in the report, formatted according to a specific citation style. You need to use the IEEE

reference format (http://journals.ieeeauthorcenter.ieee.org/wp-content/uploads/sites/7/IEEE_Reference_Guide.pdf).

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