3-1. Example: Simple Vending Machine

Implement a vending machine. This vending machine sell cokes. You can only put one 1-yuan coin into the Coke machine at a time, and each bottle of Coke sells for 3 yuan, that is, you can make the Coke machine dispense Coke by putting in 3 coins. If you don't have enough coins and want to give up putting in coins, you need to press the reset button, otherwise the money you put in before cannot be returned.
Note: No refund button

Requirements:

1. Write the Verilog codes to build the required circuit.
2. Do the simulation to verify whether your designs and codes satisfy the required functions.
3. You do NOT need to include this example in your report.

3-2. Vending Machine in Lecture Slide

Implement a vending machine. The unit price of the beverage is 2 yuan, and the vending machine can only accept coins of 0.5 yuan and 1 yuan. Consider change and delivery. The coin insertion and delivery process are carried out one by one, and there will be no phenomenon of inserting multiple coins at one time or delivering multiple bottles of beverages at one time. After each round of coin insertion, delivery, and change, the vending machine can enter a new automatic vending state.

Note:

- No refund button
- Refer to pages 39~47 in 5_HDL-2.pptx

Requirements:

1. Write the Verilog codes to build the required circuit.
2. Do the simulation to verify whether your designs and codes satisfy the required functions.
3. You need to include this experiment in your report. In your report, you need to include:
    a) Introduction:
        i. Introduce the background. For example, you can introduce
            - What is the state machine,
            - Importance of the state machine,
            - Real-world applications of the state machine
            - …
        ii. Purpose of the experiment
        iii. Brief introduce your designs and key results
        iv. Contributions of your group members
        v. …
    b) Materials and Methods: Show your FPGA solution. You need to show
        i. Your designed structure block diagram,
        ii. Your designed signal waveforms,
        iii. Your designed state transfer diagram,
        iv. …
    c) Results: Show your simulation results. You need to show
        i. How you build the testbench,
        ii. Testing inputs,

iii. Expected outputs,
iv. Actual outputs,
v. Differences between the expected outputs and the actual outputs,
vi. Expected values, actual values, and their differences of the important internal variables
vii. …

a) Discussions. This part is not essential in this experiment, but you can show:
   i. If you find any bugs or problems that you can not solve in the given time, you can discuss them and show your possible solutions.
   ii. If you find any interesting results, you can discuss them.
   iii. …

d) Conclusion. You need to
   i. Summarize all your designs and simulation results,
   ii. Summarize the key discussions if you have
   iii. …

e) References. This is a list of all the sources cited in the report, formatted according to a specific citation style. You need to use the IEEE reference format (http://journals.ieeeauthorcenter.ieee.org/wp-content/uploads/sites/7/IEEE_Reference_Guide.pdf).

f) Appendices. This optional section can include codes, raw data, calculations, additional graphs, and other supplementary material that is relevant but not essential to the main report.

3-3. Vending Machine with Refund Function

Implement a vending machine. The function of this vending machine is same as the vending machine in the experiment 3-2. But, in this experiment, you need to consider the refund function: When the reset button is pressed, not only does the machine status return to the idle state, but the money entered by the user also needs to be refunded.

Requirements:

1. Write the Verilog codes to build the required circuit.
2. Do the simulation to verify whether your designs and codes satisfy the required functions.
3. You need to include this experiment in your report. In your report, you need to include:
    a) Introduction:
        i. Purpose of the experiment
        ii. Brief introduce your designs and key results
        iii. Contributions of your group members
        iv. …
    b) Materials and Methods: Show your FPGA solution. You need to show
        i. Your designed structure block diagram,
        ii. Your designed signal waveforms,
        iii. Your designed state transfer diagram,
        iv. …
    c) Results: Show your simulation results. You need to show
        i. How you build the testbench,
        ii. Testing inputs,
        iii. Expected outputs,
        iv. Actual outputs,
        v. Differences between the expected outputs and the actual outputs,
        vi. Expected values, actual values, and their differences of the important internal variables
        vii. …
    b) Discussions. This part is not essential in this experiment, but you can show:
        i. If you find any bugs or problems that you can not solve in the given time, you can discuss them and show your possible

solutions.

ii. If you find any interesting results, you can discuss them.

iii. …

d) Conclusion. You need to

i. Summarize all your designs and simulation results,

ii. Summarize the key discussions if you have

iii. …

e) References. This is a list of all the sources cited in the report, formatted according to a specific citation style. You need to use the IEEE reference format (http://journals.ieeeauthorcenter.ieee.org/wp-content/uploads/sites/7/IEEE_Reference_Guide.pdf).

f) Appendices. This optional section can include codes, raw data, calculations, additional graphs, and other supplementary material that is relevant but not essential to the main report.