EIE330 FPGA Based System Design

Report of Laboratory 1

FPGA Lab1: Full adder, Decoder, and Comparator

Source Code of this report can be found at: EIE330-FPGA-Laboratory

by

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This report is a part of the result for EIE330 FPGA Based System Design in U.C.T.M

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Conteúdo

Capítulo I

Abstract

I: I Result

Source Code of this report can be found at the git-hub repository: EIE330-FPGA-Laboratory. And the demonstration video of certain code can be found at the Github release Page or the Youtube video.

All relevant output in this report is shown in the following directory.

- **FPGA Lab1**
  1. 1-0. Report [T][Z]
     (a) Text [T][Z]
     (b) Video [T]
  2. 1-5. Full adder
     (a) Design [Z]
     (b) Coding [Z]
     (c) Test [Z]
  3. 1-6. Decoder
     (a) Design [T]
     (b) Coding [T]
     (c) Test [T]
  4. 1-7. Comparator
     (a) Design [Z]
     (b) Coding [Z]
     (c) Test [Z]

I: II Contribution

And the contribution of each member is labeled with their last name:

1. Pengrui Tang: [T]
2. Xiaoyang Zhen: [Z]

Capítulo II

Full-Adder

II: I Introduction

i Background

The full adder is the basic component in digital circuits to carry out arithmetic operations. Different from the half adder, the full adder handles the addition of three inputs(A, B, and Carry-in) and output the sum and carry-out of them.

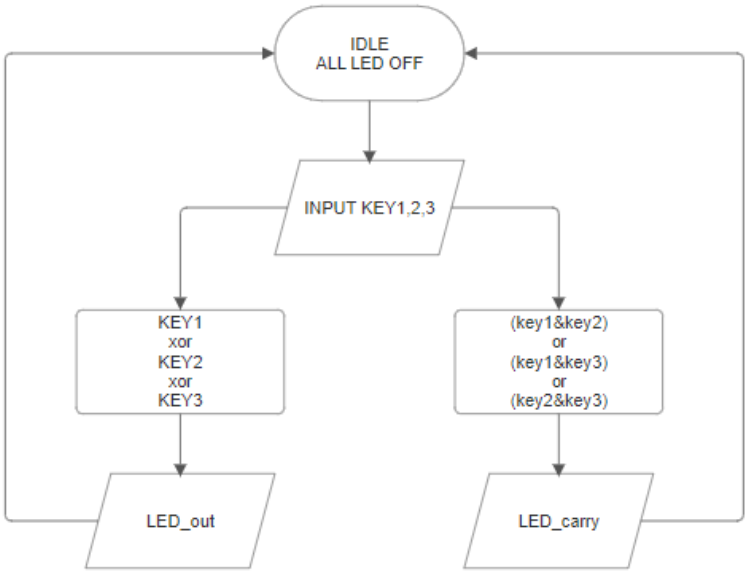
ii Purpose

In this experiment, we want to design a full adder using the FPGA board that can handle three single-bit input additions.

iii Design and Key-results

II: II Materials and Methods

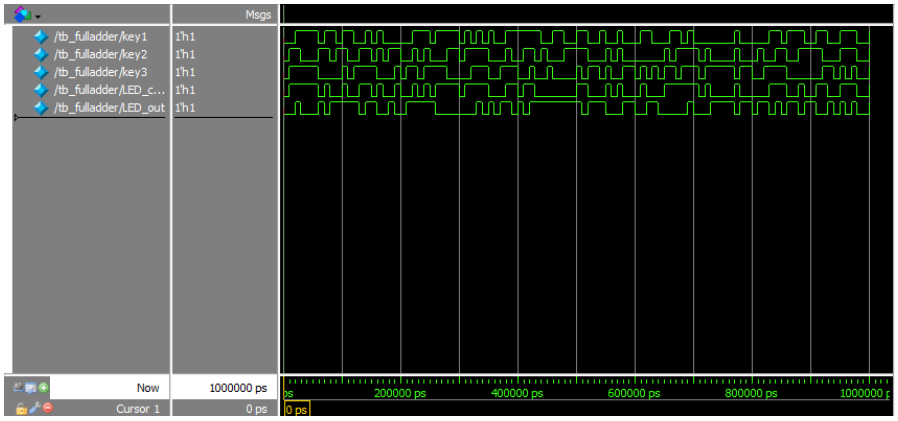
i Structure Block Diagram



ii Truth Table

Key1	Key2	Key3	LED_cout	LED_out
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

iii Signal Waveforms



iv Resources in Board

II: III Results

i Testbench

In this experiment, the testbench was built to accept three one-bit inputs. The testing inputs were randomly generated, and the outputs were presented by waveform. The expected results are listed below (carry, out):

1. All inputs are 0s. Output 0,0
2. One input is 1, and two are 0s. Output 0,1
3. Two inputs are 1, and one is 0. Output 1,0
4. ALL inputs are 1s. Output 1,1

It turned out that the actual output value was the same as we predicted.

II: IV Discussions and Conclusion

i Discussions

We encountered the problem of the testbench simulation not giving out the waveform plot in this experiment. It turns out that it is the problem with the testbench codes, in which the initiation part has the wrong name.

ii Conclusion

In this experiment, we learned how to use Quartus to create an FPGA project, write a Verilog code, and develop a testbench for the Verilog design.

II: V Appendices

References and Appendices

i Reference

ii Appendices

Capítulo III

2-4 Line Decoder

III: I Introduction

i Background

A decoder can take n-th input lines and then decode them into 2^n different output lines. One application of such a component is to drive a display array with relatively narrow input lines.

ii Purpose

In this experiment, we want to design a 2-4 line decoder with an enabler that can handle a two-bit input and decode them to light up 4 different LEDs.

iii Design and Key-results

The line decoder have one 2-bit input

III: II Materials and Methods

i Structure Block Diagram

ii Truth Table

A1	A0	B3	B2	B1	B0
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Capítulo IV

One-bit Digital Comparator

IV: I Introduction

i Background

The one-bit comparator can perform a logic comparison to judge the magnitude of two single-bit inputs. It outputs three different states to show the result which indicates greater, smaller, and equal.

ii Purpose

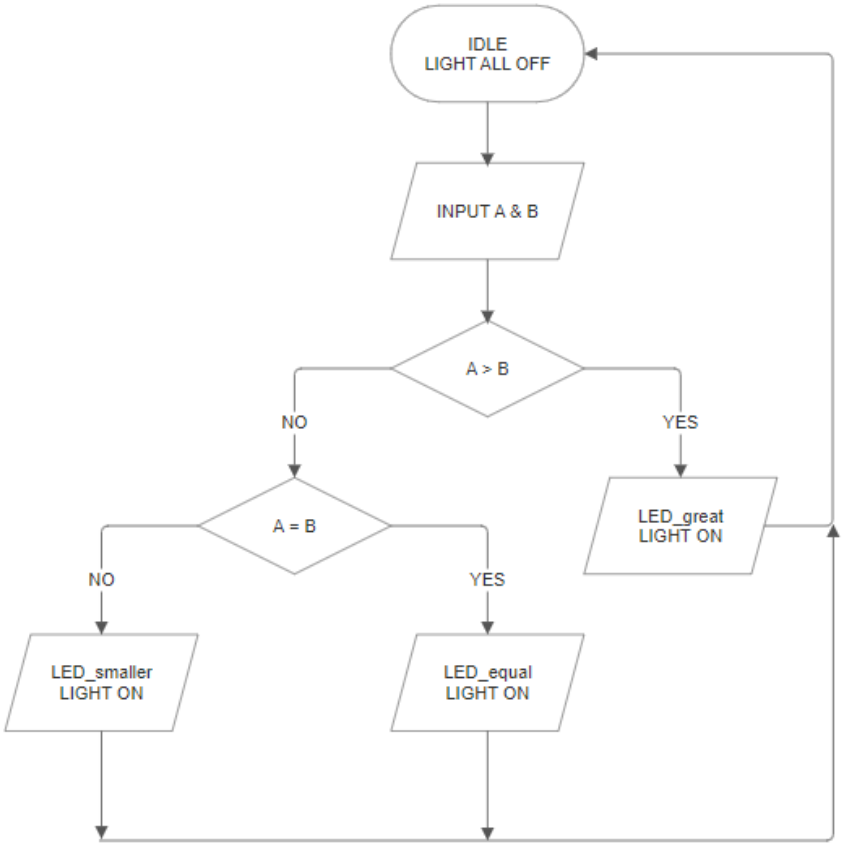
In this experiment, we aimed to design a circuit that is able to compare two one-bit inputs and give three different states of output, which shows the numerical relationship between two inputs.

iii Design and Key-results

iv Contribution

IV: II Materials and Methods

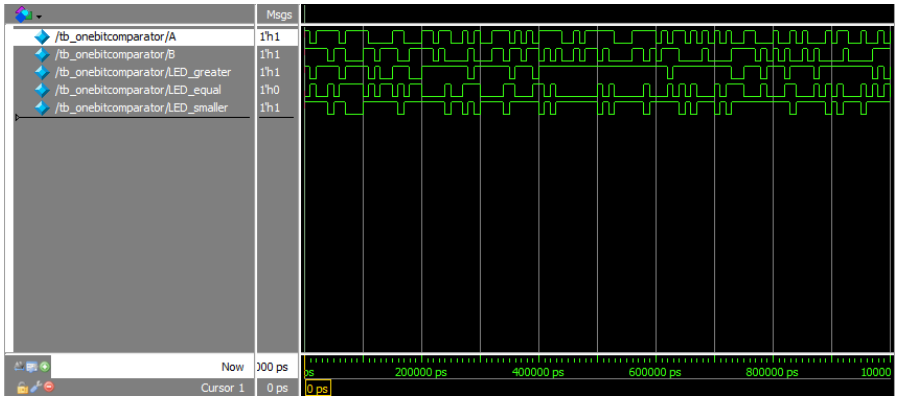
i Structure Block Diagram



ii Truth Table

A	B	LED_greater	LED_equal	LED_smaller
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

iii Signal Waveforms



iv Resources in Board

IV: III Results

i Testbench

In this experiment, the testbench was built to accept two one-bit inputs. The testing inputs were randomly generated, and the outputs were presented by waveform. The expected outputs are shown below:

1. Input A

IV: IV Discussions and Conclusion

i Discussions

During this experiment, we encountered a problem of differences in the recognition of signal inputs. When the button is pressed, we expect it is inputting signal 1 into the system. However, instead of entering signal 1, the chip recognizes the button pressing behaviour as sending signal 0. Eventually, the misinterpretation resulted in the opposite output. To fix this output error, we decided to reverse the logic judgment that was used to compare the input signals. Now, when the chip accepts the input A<B, which we originally predicted as A>B, it correctly produces the expected outcome of A>B.

ii Conclusion

In this experiment, we met some unexpected errors. Eventually, we overcame them by discussion. We successfully designed a circuit that can compare two single-bit inputs and give a correct magnitude relationship outcome.

IV: V Appendices

References and Appendices

i Reference

ii Appendices