5-1. Example: How to create single-port RAM IP core

Follow “5-1 How to create single-port RAM IP core.pdf” to study how to create and use the single-port RAM IP core.

Requirements:

1. You do NOT need to include this example in your report.

5-2. Example: How to create single-port ROM IP core

Follow “5-2 How to create single-port ROM IP core.pdf” to study how to create and use the single-port ROM IP core.

Requirements:

1. You do NOT need to include this example in your report.

5-3. Key Debounce

According to the lecture slide, write the key debounce module, and do the simulation. The simulation must simulate the key jitter and verify whether your designed module can achieve the key debounce function.

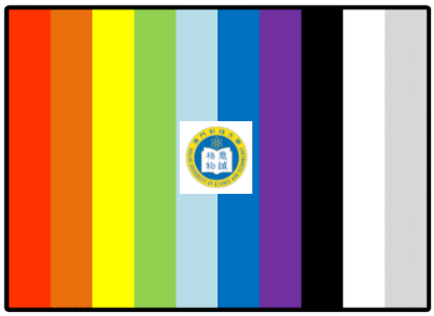
Requirements:

2. Write the Verilog codes to build the required circuit.
3. Do the simulation to verify whether your designs and codes satisfy the required functions.
4. You need to include this experiment in your report. In your report, you need to include:
    a) Introduction:
        i. Introduce the background. For example, you can introduce
            - what is the key debounce,
            - the risk of the key debounce
            - the possible methods of solving the key debounce, and which method we focused on in this experiment
            - …
        ii. Purpose of the experiment
        iii. Brief introduce your designs and key results
        iv. Contributions of your group members
        v. …
    b) Materials and Methods: Show your FPGA solution. You need to show
        i. your designed structure block diagrams,
        ii. your designed signal waveforms,
        iii. …
    c) Results: Show your simulation results. You need to show
        i. how you build the testbenches,
        ii. the testing inputs,
        iii. the expected outputs,
        iv. the actual outputs,
        v. the differences between the expected outputs and the actual outputs,
        vi. the expected values, actual values, and their differences of the important internal variables
        vii. …

a) Discussions. This part is not essential in this experiment, but you can show:
    i. If you find any bugs or problems that you can not solve in the given time, you can discuss them and show your possible solutions.
    ii. If you find any interesting results, you can discuss them.
    iii. …
d) Conclusion. You need to
    i. summarize all your designs and simulation results,
    ii. summarize the key discussions if you have
    iii. …
e) References. This is a list of all the sources cited in the report, formatted according to a specific citation style. You need to use the IEEE reference format (http://journals.ieeeauthorcenter.ieee.org/wp-content/uploads/sites/7/IEEE_Reference_Guide.pdf).
f) Appendices. This optional section can include codes, raw data, calculations, additional graphs, and other supplementary material that is relevant but not essential to the main report.

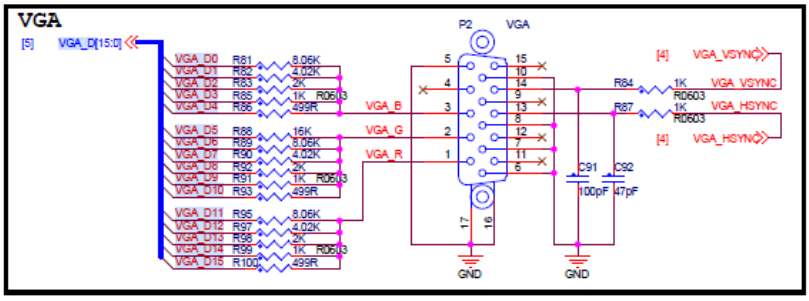
5-4. VGA Display with ROM

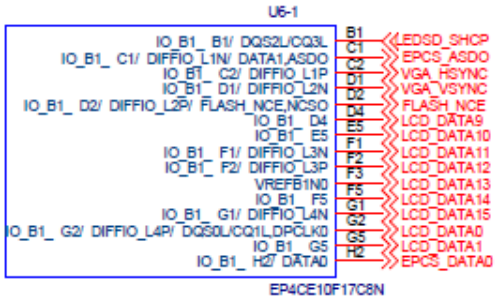
Write a VGA driver and use the FPGA development board to drive the VGA display to the MUST logo with ten-color equal-width color bars as the background. The VGA display mode is 640x480@60. The expected experimental result is the following figure.

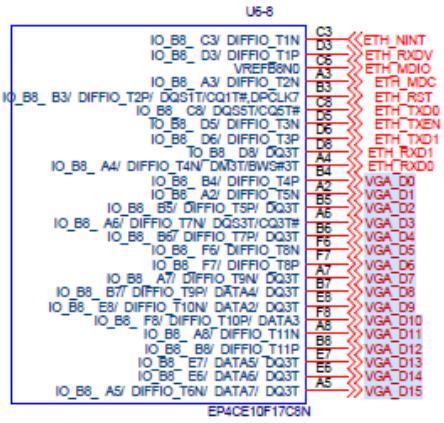


Note:

- The MUST logo image and the corresponding .mif file have already been provided in the Github project folder. You can directly use the .mif file as the memory initialization file, or use the given MATLAB file (.m file) to create the .mif file by yourself.
- Do NOT forget to plan pins before download your design to the development board







Requirements:

2. Write the Verilog codes to build the required circuit.
3. Do the simulation to verify whether your designs and codes satisfy the required functions.
4. You need to test your designs in the development board
5. You need to include this experiment in your report. In your report, you need to include:
    a) Introduction:
        i. Introduce the background. For example, you can introduce
            - what is the rom,
            - the key differences between the ROM and the RAM
            - …
        ii. Purpose of the experiment
        iii. Brief introduce your designs and key results
        iv. Contributions of your group members
        v. …
    b) Materials and Methods: Show your FPGA solution. You need to show
        i. your designed structure block diagrams,
        ii. your designed signal waveforms,
        iii. …
    c) Results: Show your simulation and corresponding testing results. You need to show
        i. how you build the testbenches,
        ii. the testing inputs,
        iii. the expected outputs,
        iv. the actual outputs,
        v. the differences between the expected outputs and the actual outputs,
        vi. the expected values, actual values, and their differences of the important internal variables
        vii. testing results in the development board
        viii. …
    b) Discussions. This part is not essential in this experiment, but you can show:
        i. If you find any bugs or problems that you can not solve in the given time, you can discuss them and show your possible

solutions.

ii. If you find any interesting results, you can discuss them.

iii. …

d) Conclusion. You need to

i. summarize all your designs and simulation results,

ii. summarize the key discussions if you have

iii. …

e) References. This is a list of all the sources cited in the report, formatted according to a specific citation style. You need to use the IEEE reference format (http://journals.ieeeauthorcenter.ieee.org/wp-content/uploads/sites/7/IEEE_Reference_Guide.pdf).

f) Appendices. This optional section can include codes, raw data, calculations, additional graphs, and other supplementary material that is relevant but not essential to the main report.