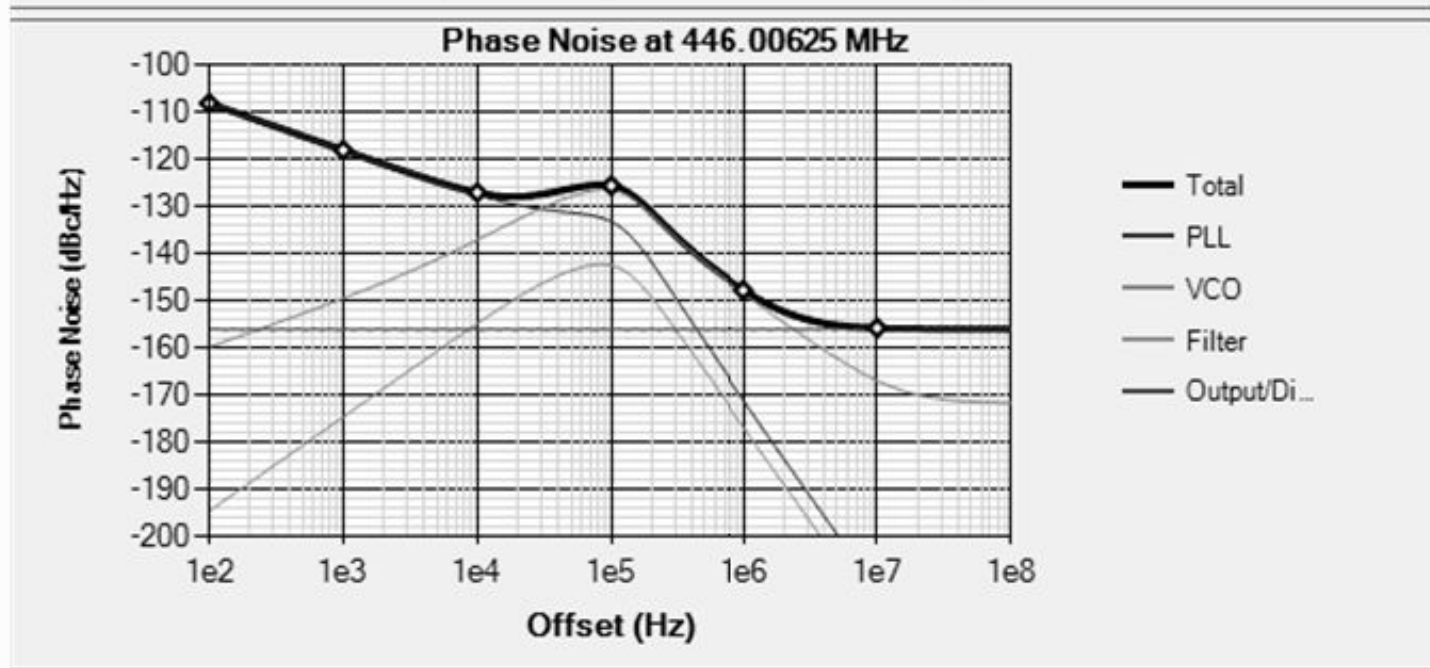
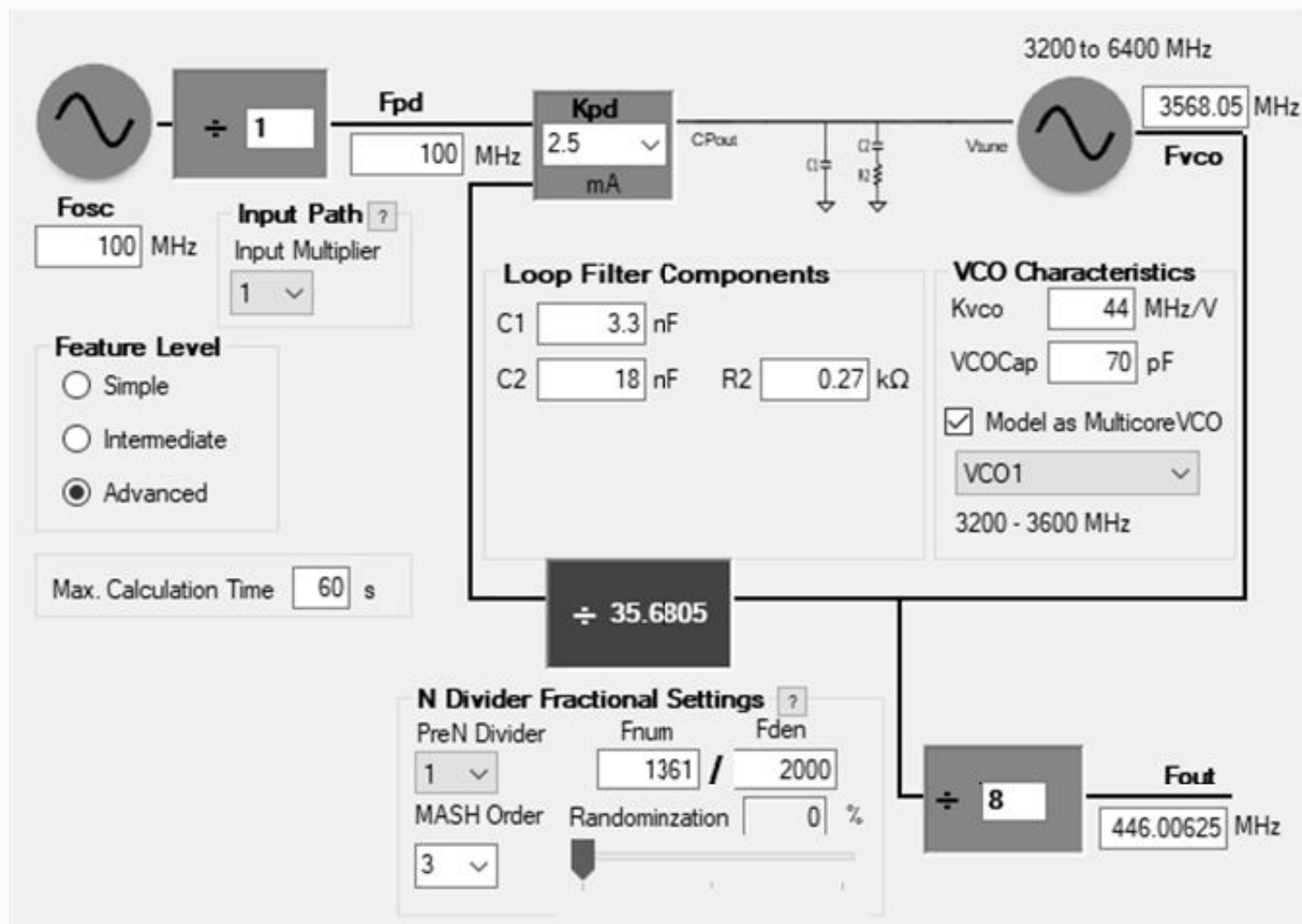


Project	Direct FM modulator test.PrjPcb		
Sheet Name	Connectors.SchDoc		
Drawn By	*	Variant Name	[No Variations]
		Sheet	3 of 4
Checked By	*	Revision	*
		Date	*



Select Device Filter Designer Phase Noise Spurs Lock Time Bode Plot

LMX2572LP Design Tips

Filter Architecture Filter Order 2nd Order Filter Type Passive

Filter Parameters Calculate Loop Filter Auto Parameter Strategy Maximize BW (Fast Lock Ti)

Design Target Actual

Loop Bandwidth 100 kHz 104.4671 kHz

Phase Margin 30 deg 45.8898 deg

Gamma 1.4 1.6048

Min. High Order Cap 1500 pF 330 pF

Capacitor Value Step 10% Resistor Value Step 10%

Simulation Shown Phase Noise Gain Margin 1000 dB

Forced Component Values C1 nF C2 nF R2 kΩ

Performance Summary Setup Conditions other Tabs Optimize Disabled

Parameter	Achieved
Jitter (fs)	125.3
Phase Noise at MI	-108
Phase Noise at MI	-118
Phase Noise at MI	-127
Total Lock Time (s)	130.4

