LMH6505 Wideband, Low Power, Linear-in-dB, Variable Gain Amplifier

Check for Samples: LMH6505

FEATURES

- **V_S = ±5V, T_A = 25°C, R_F = 1 kΩ, R_G = 100Ω, R_L = 100Ω, A_V = A_{VMAX} = 9.4 V/V, Typical Values Unless Specified.**
- **−3 dB BW 150 MHz**
- **Gain Control BW 100 MHz**
- **Adjustment Range (<10 MHz) 80 dB**
- **Gain Matching (Limit) ±0.50 dB**
- **Supply Voltage Range 7V to 12V**
- **Slew Rate (Inverting) 1500 V/µs**
- **Supply Current (No Load) 11 mA**
- **Linear Output Current ±60 mA**
- **Output Voltage Swing ±2.4V**
- **Input Noise Voltage 4.4 nV/√Hz**
- **Input Noise Current 2.6 pA/√Hz**
- **THD (20 MHz, R_L = 100Ω, V_O = 2 V_{PP}) −45 dBc**

APPLICATIONS

- **Variable Attenuator**
- **AGC**
- **Voltage Controlled Filter**
- **Video Imaging Processing**

DESCRIPTION

The LMH6505 is a wideband DC coupled voltage controlled gain stage followed by a high speed current feedback operational amplifier which can directly drive a low impedance load. The gain adjustment range is 80 dB for up to 10 MHz which is accomplished by varying the gain control input voltage, V_G.

Maximum gain is set by external components, and the gain can be reduced all the way to cutoff. Power consumption is 110 mW with a speed of 150 MHz and a gain control bandwidth (BW) of 100 MHz. Output referred DC offset voltage is less than 55 mV over the entire gain control voltage range. Device-to-device gain matching is within ±0.5 dB at maximum gain. Furthermore, gain is tested and ensured over a wide range. The output current feedback op amp allows high frequency large signals (Slew Rate = 1500 V/µs) and can also drive a heavy load current (60 mA) ensured.

Near ideal input characteristics (i.e. low input bias current, low offset, low pin 3 resistance) enable the device to be easily configured as an inverting amplifier as well.

To provide ease of use when working with a single supply, the V_G range is set to be from 0V to +2V relative to the ground pin potential (pin 4). V_G input impedance is high in order to ease drive requirement. In single supply operation, the ground pin is tied to a "virtual" half supply.

The LMH6505's gain control is linear in dB for a large portion of the total gain control range from 0 dB down to −85 dB at 25°C, as shown below. This makes the device suitable for AGC applications. For linear gain control applications, see the LMH6503 datasheet.

The LMH6505 is available in either the 8-Pin SOIC or the 8-Pin VSSOP package. The combination of minimal external components and small outline packages allows the LMH6505 to be used in space-constrained applications.

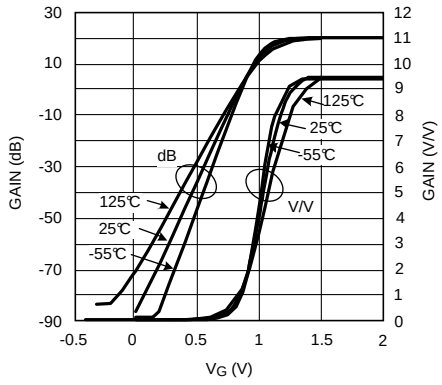


Figure 1. Gain vs. V_G

Typical Application

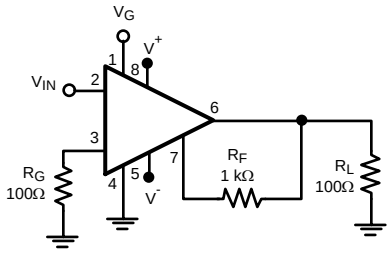


Figure 2. A_{VMAX} = 9.4 V/V

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
Input Current	±10 mA
Output Current (4)	120 mA
Supply Voltages (V^+ - V^-)	12.6V
Voltage at Input/ Output pins	V^+ +0.8V, V^- −0.8V
Storage Temperature Range	−65°C to 150°C
Junction Temperature	150°C
Soldering Information:	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations or value specified, whichever is lower.

Operating Ratings(1)

Supply Voltages (V^+ - V^-)		7V to 12V
Temperature Range (2)		−40°C to +85°C
Thermal Resistance:	(θ_{JC})	(θ_{JA})
8 -Pin SOIC	60	165
8-Pin VSSOP	65	235

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_J = 25°C, V_S = ±5V, A_{VMAX} = 9.4 V/V, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = ±0.1V, R_L = 100Ω, V_G = +2V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Frequency Domain Response						
BW	−3 dB Bandwidth	V_{OUT} < 1 V_{PP}		150		MHz
		V_{OUT} < 4 V_{PP}, A_{VMAX} = 100		38		
GF	Gain Flatness	V_{OUT} < 1 V_{PP} 0.9V ≤ V_G ≤ 2V, ±0.2 dB		40		MHz
Att Range	Flat Band (Relative to Max Gain) Attenuation Range (4)	±0.2 dB Flatness, f < 30 MHz		26		dB
		±0.1 dB Flatness, f < 30 MHz		9.5		
BW Control	Gain control Bandwidth	V_G = 1V (5)		100		MHz
CT (dB)	Feed-through	V_G = 0V, 30 MHz (Output/Input)		−51		dB
GR	Gain Adjustment Range	f < 10 MHz		80		dB
		f < 30 MHz		71		
Time Domain Response						
t_r, t_f	Rise and Fall Time	0.5V Step		2.1		ns
OS %	Overshoot			10		%
SR	Slew Rate (6)	Non Inverting		900		V/µs
		Inverting		1500		

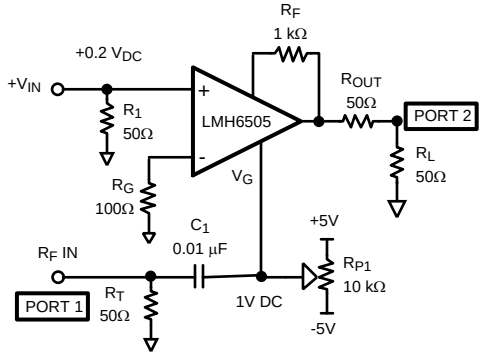
(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the Electrical Tables under conditions of internal self-heating where $T_J > T_A$.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(4) Flat Band Attenuation (Relative To Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either ±0.2 dB or ±0.1 dB), relative to A_{VMAX} gain. For example, for f < 30 MHz, here are the Flat Band Attenuation ranges:
±0.2 dB: 19.7 dB down to -6.3 dB = 26 dB range
±0.1 dB: 19.7 dB down to 10.2 dB = 9.5 dB range

(5) Gain control frequency response schematic:



(6) Slew rate is the average of the rising and falling slew rates.

Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for T_J = 25°C, V_S = ±5V, A_{VMAX} = 9.4 V/V, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = ±0.1V, R_L = 100Ω, V_G = +2V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Distortion & Noise Performance						
HD2	2nd Harmonic Distortion	$2V_{PP}$, 20 MHz		−47		dBc
HD3	3rd Harmonic Distortion			–61		
THD	Total Harmonic Distortion			−45		
En tot	Total Equivalent Input Noise	f > 1 MHz, R_{SOURCE} = 50Ω		4.4		nV/√Hz
I_N	Input Noise Current	f > 1 MHz		2.6		pA/√Hz
DG	Differential Gain	f = 4.43 MHz, R_L = 100Ω		0.30		%
DP	Differential Phase			0.15		deg
DC & Miscellaneous Performance						
GACCU	Gain Accuracy (See Application Information)	V_G = 2.0V		0	±0.50	dB
		0.8V < V_G < 2V		+0.1/−0.53	+4.3/−3.9	
G Match	Gain Matching (See Application Information)	V_G = 2.0V		—	±0.50	dB
		0.8V < V_G < 2V		—	+4.2/−4.0	
K	Gain Multiplier (See Application Information)		0.890 **0.830**	0.940	0.990 **1.04**	V/V
V_{IN} NL	Input Voltage Range	R_G Open		±3		V
V_{IN} L		R_G = 100Ω	±0.60 **±0.50**	±0.74		
I_{RG_MAX}	R_G Current	Pin 3	±6.0 **±5.0**	±7.4		mA
I_{BIAS}	Bias Current	Pin 2 (7)		−0.6	−2.5 **−2.6**	µA
TC I_{BIAS}	Bias Current Drift	Pin 2 (8)		1.28		nA/°C
R_{IN}	Input Resistance	Pin 2		7		MΩ
C_{IN}	Input Capacitance	Pin 2		2.8		pF
I_{VG}	V_G Bias Current	Pin 1, V_G = 2V (7)		0.9		µA
TC I_{VG}	V_G Bias Drift	Pin 1 (8)		10		pA/°C
R_{VG}	V_G Input Resistance	Pin 1		25		MΩ
C_{VG}	V_G Input Capacitance	Pin 1		2.8		pF
V_{OUT} L	Output Voltage Range	R_L = 100Ω	±2.1 **±1.9**	±2.4		V
V_{OUT} NL		R_L = Open		±3.1		
R_{OUT}	Output Impedance	DC		0.12		Ω
I_{OUT}	Output Current	V_{OUT} = ±4V from Rails	±60 **±40**	±80		mA
$V_{O\ OFFSET}$	Output Offset Voltage	0V < V_G < 2V		±10	±55 **±70**	mV
+PSRR	+Power Supply Rejection Ratio (9)	Input Referred, 1V change, V_G = 2.2V	–65	–72		dB
−PSRR	−Power Supply Rejection Ratio (9)	Input Referred, 1V change, V_G = 2.2V	–65	–75		dB
I_S	Supply Current	No Load	9.5 **7.5**	11	14 **16**	mA

(7) Positive current corresponds to current flowing into the device.
(8) Drift is determined by dividing the change in parameter distribution at temperature extremes by the total temperature change.
(9) +PSRR definition: $[|\Delta V_{OUT}/\Delta V^+| / A_V]$, −PSRR definition: $[|\Delta V_{OUT}/\Delta V^-| / A_V]$ with 0.1V input voltage. ΔV_{OUT} is the change in output voltage with offset shift subtracted out.

Connection Diagram

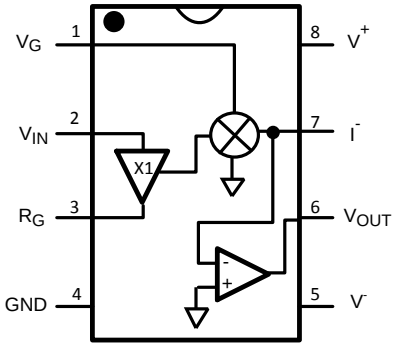
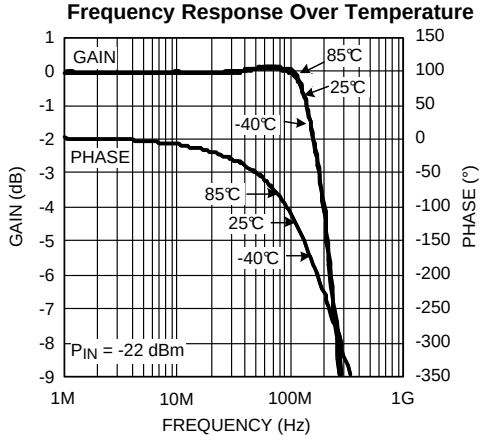


Figure 3. 8-Pin SOIC/VSSOP Top View

Typical Performance Characteristics

Unless otherwise specified: V_S = ±5V, T_A = 25°C, $V_G = V_{GMAX}$, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = 0.1V, input terminated in 50Ω. R_L = 100Ω, Typical values.

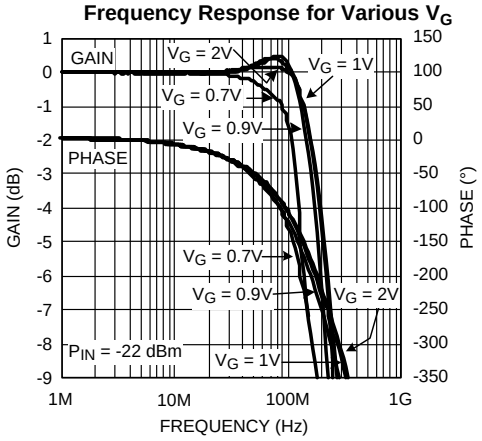
Frequency Response Over Temperature



Gain/Phase normalized to low frequency value at 25°C.

Figure 4.

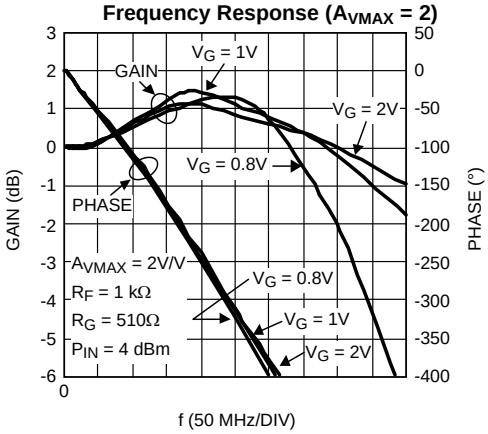
Frequency Response for Various V_G



Gain/Phase normalized to low frequency value at each setting.

Figure 5.

Frequency Response (A_{VMAX} = 2)



Gain/Phase normalized to low frequency value at each setting.

Figure 6.

Inverting Frequency Response

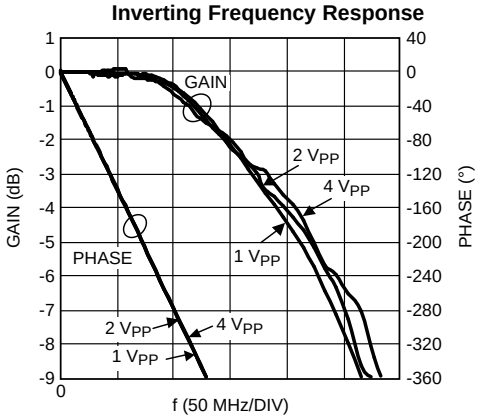
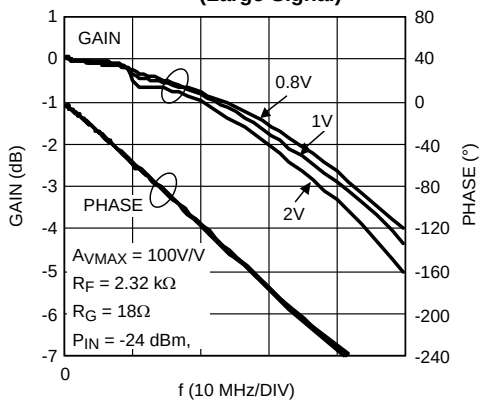


Figure 7.

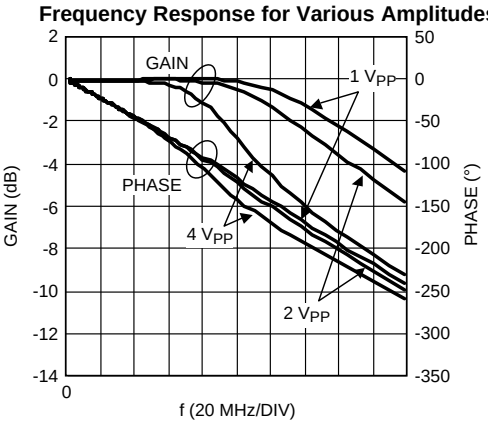
Frequency Response for Various V_G (A_{VMAX} = 100) (Large Signal)



Gain/Phase normalized to low frequency value at each setting.

Figure 8.

Frequency Response for Various Amplitudes



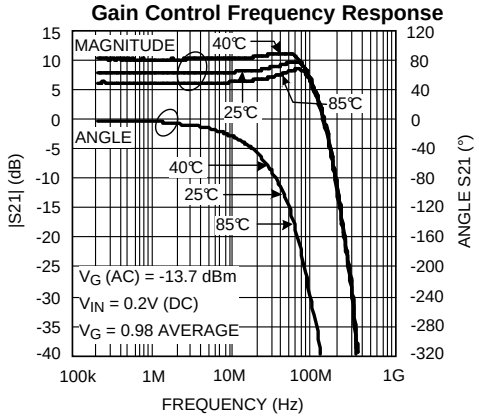
Gain/Phase normalized to low frequency value at each setting.

Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, T_A = 25°C, V_G = V_{GMAX}, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = 0.1V, input terminated in 50Ω. R_L = 100Ω, Typical values.

Gain Control Frequency Response



See Electrical Characteristics Note (5).

Figure 10.

I_S vs. V_S

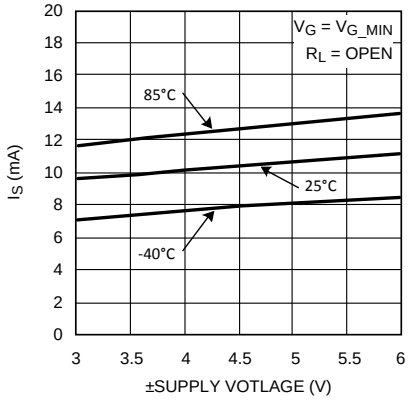


Figure 11.

I_S vs. V_S

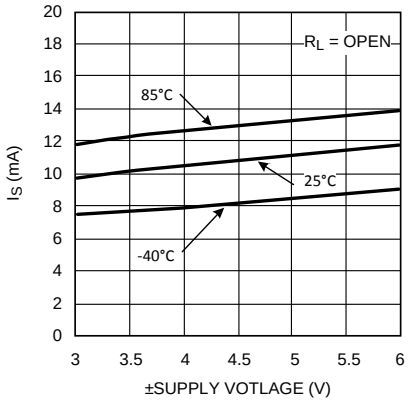


Figure 12.

Input Bias Current vs. V_S

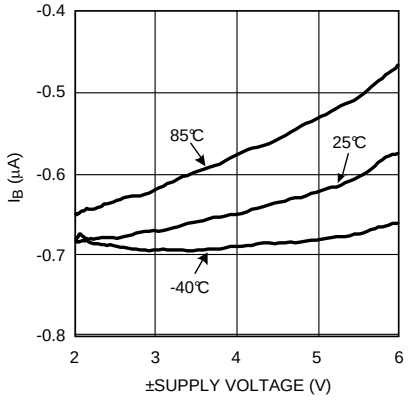
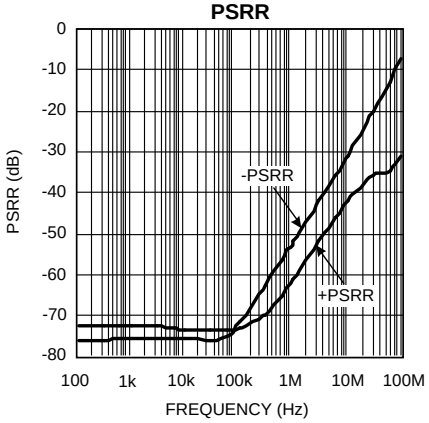


Figure 13.

PSRR



See Electrical Characteristics Note (9)

Figure 14.

A_{VMAX} vs. Supply Voltage

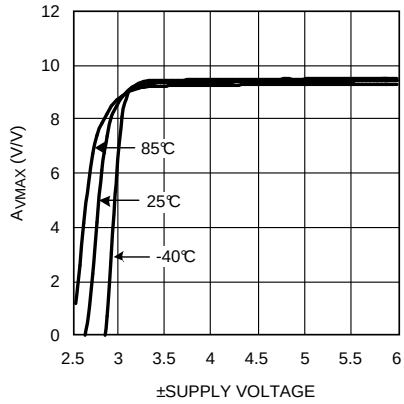


Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, T_A = 25°C, V_G = V_{GMAX}, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = 0.1V, input terminated in 50Ω. R_L = 100Ω, Typical values.

Feed through Isolation for Various A_{VMAX}

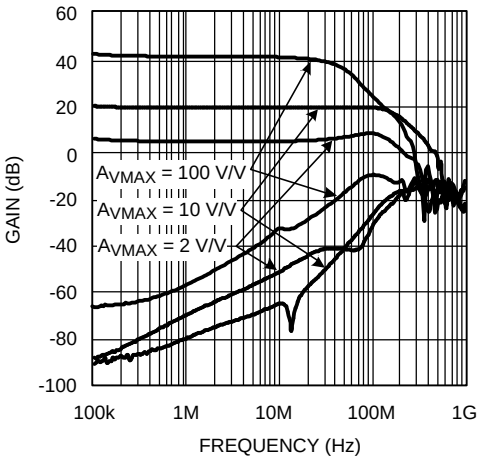


Figure 16.

Gain Variation Over entire Temp Range vs. V_G

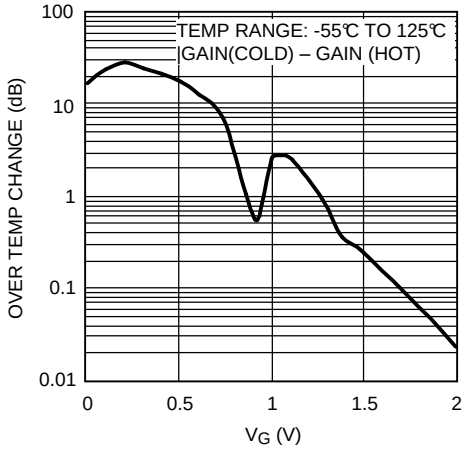
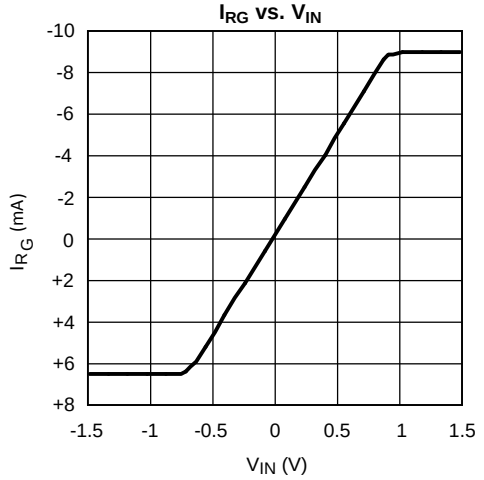


Figure 17.

I_{RG} vs. V_{IN}



See Electrical Characteristics Note (7).

Figure 18.

Gain vs. V_G

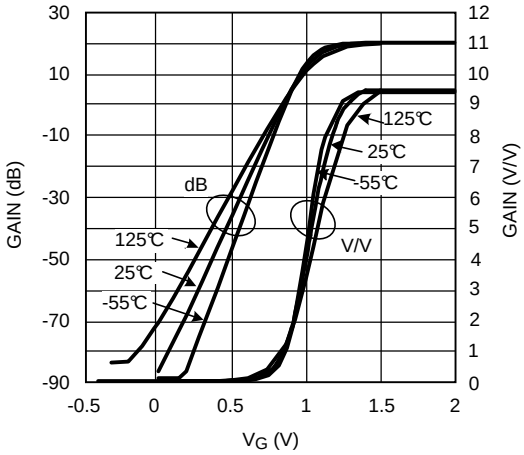


Figure 19.

Output Offset Voltage vs. V_G (Typical Unit #1)

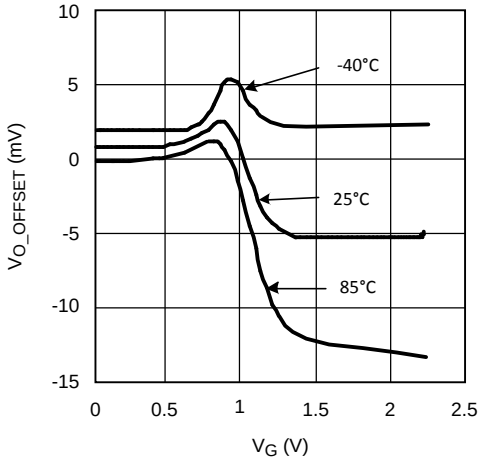


Figure 20.

Output Offset Voltage vs. V_G (Typical Unit #2)

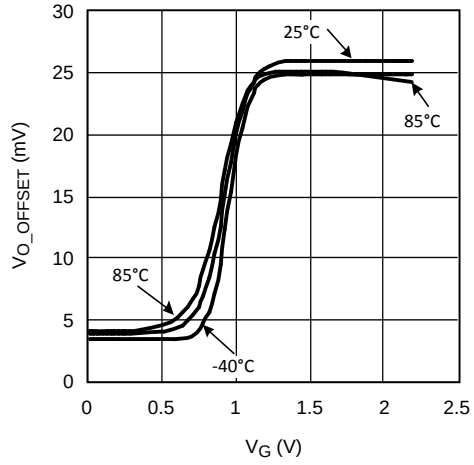


Figure 21.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, T_A = 25°C, V_G = V_{GMAX}, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = 0.1V, input terminated in 50Ω. R_L = 100Ω, Typical values.

Output Offset Voltage vs. V_G (Typical Unit #3)

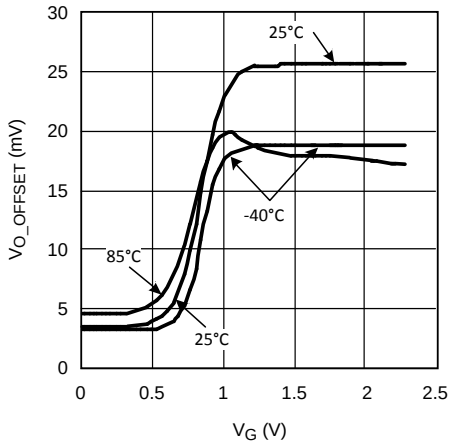


Figure 22.

Distribution of Output Offset Voltage

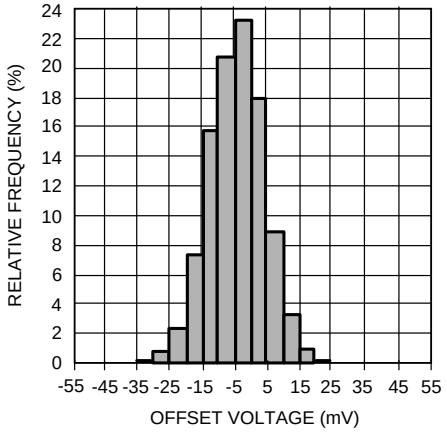


Figure 23.

Output Noise Density vs. Frequency

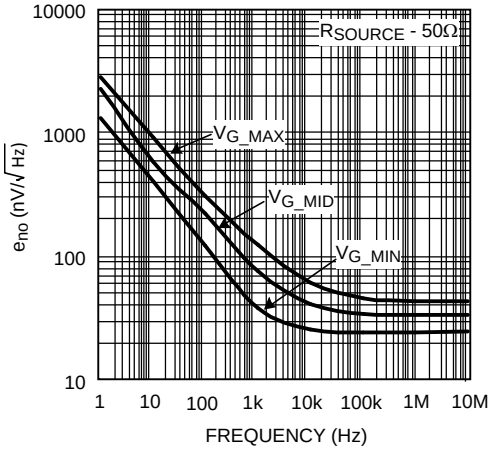


Figure 24.

Output Noise Density vs. Frequency

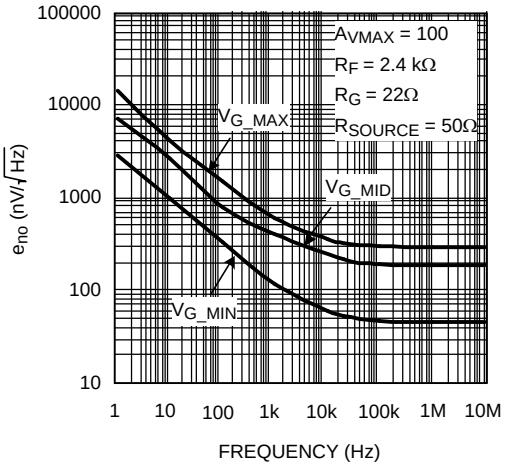


Figure 25.

Output Noise Density vs. Frequency

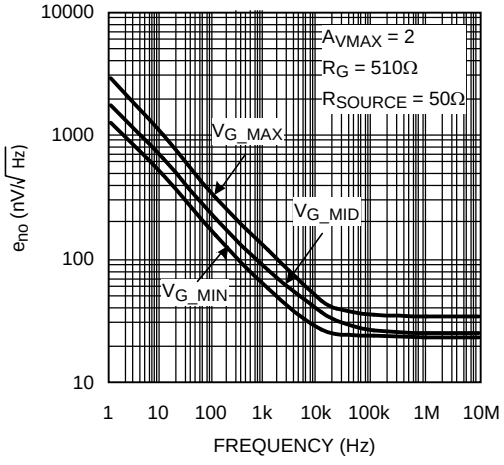


Figure 26.

Input Referred Noise Density vs. Frequency

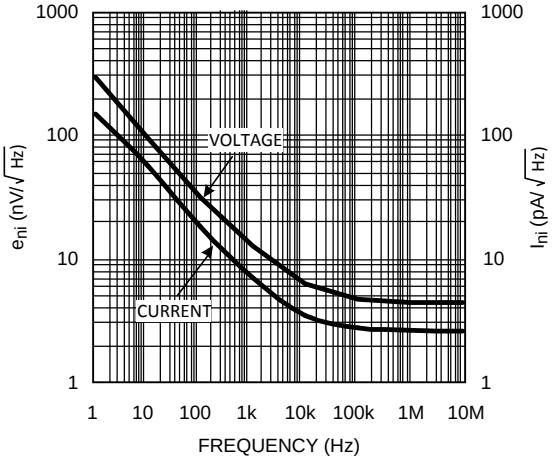


Figure 27.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, T_A = 25°C, V_G = V_{GMAX}, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = 0.1V, input terminated in 50Ω. R_L = 100Ω, Typical values.

Output Voltage vs. Output Current (Sinking)

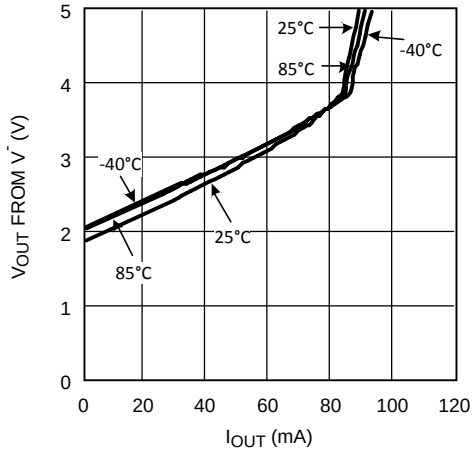


Figure 28.

Output Voltage vs. Output Current (Sourcing)

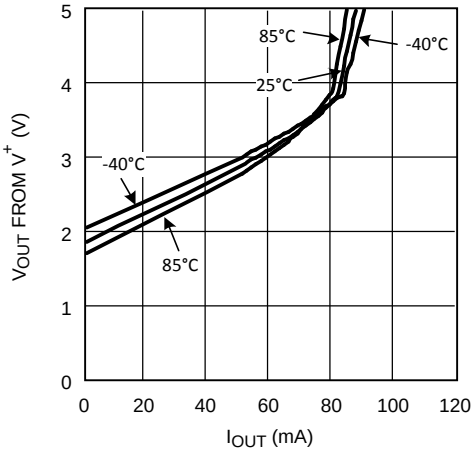


Figure 29.

Distortion vs. Frequency

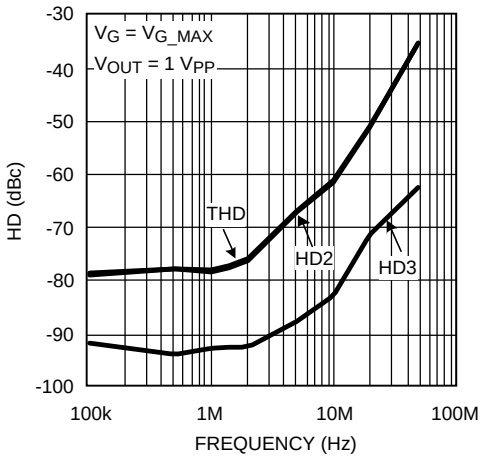


Figure 30.

HD vs. P_{OUT}

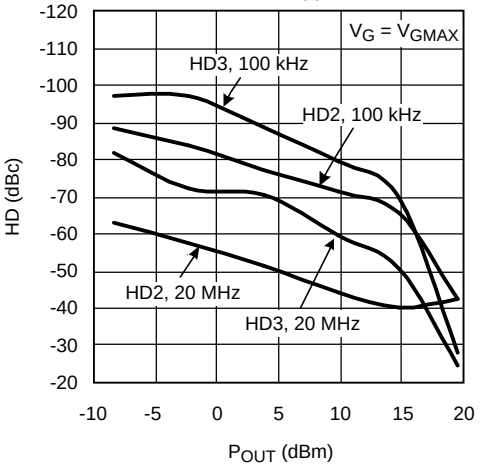


Figure 31.

THD vs. P_{OUT}

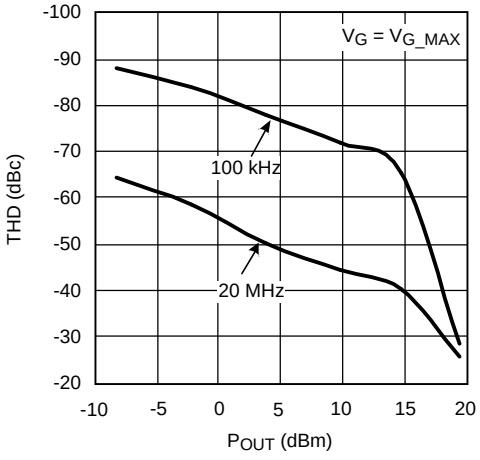


Figure 32.

THD vs. P_{OUT}

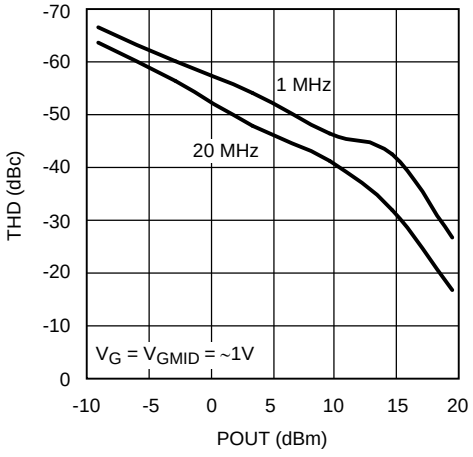


Figure 33.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, T_A = 25°C, V_G = V_{GMAX}, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = 0.1V, input terminated in 50Ω. R_L = 100Ω, Typical values.

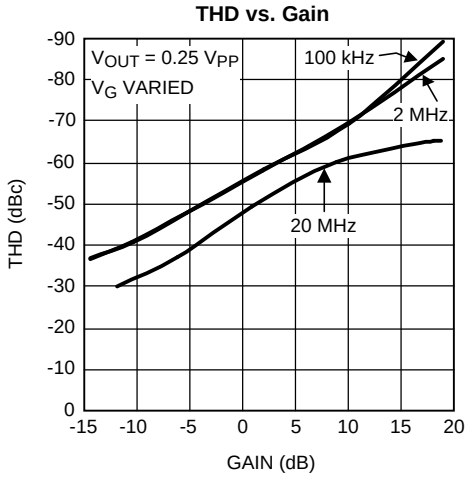


Figure 34.

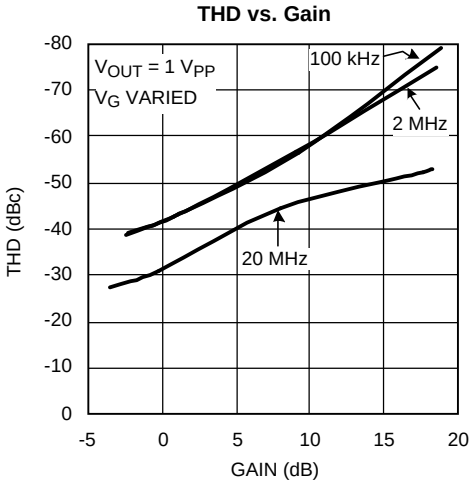


Figure 35.

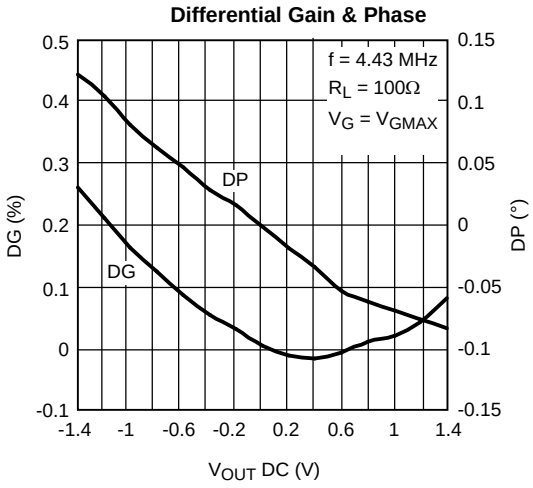


Figure 36.

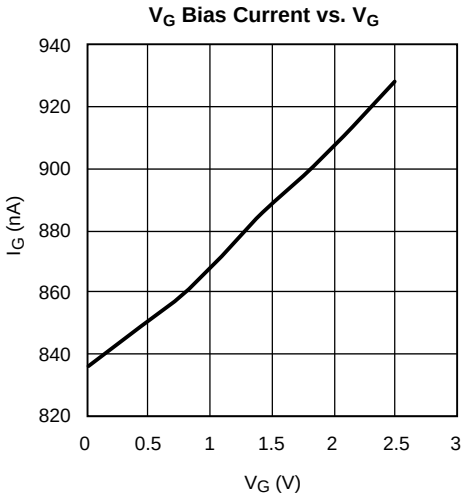


Figure 37.

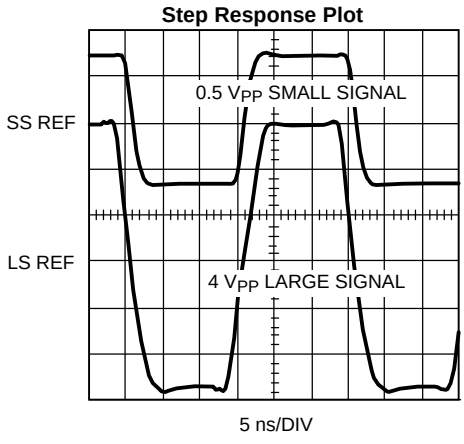


Figure 38.

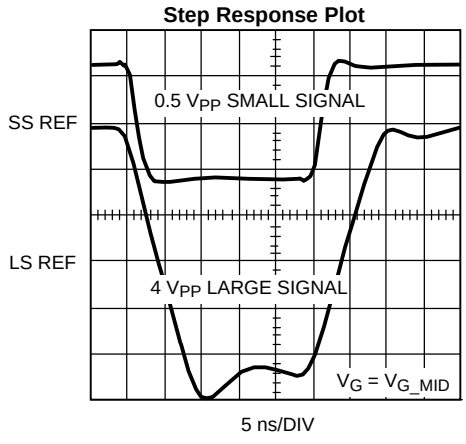


Figure 39.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, T_A = 25°C, V_G = V_{GMAX}, R_F = 1 kΩ, R_G = 100Ω, V_{IN} = 0.1V, input terminated in 50Ω. R_L = 100Ω, Typical values.

Gain vs. V_G Step

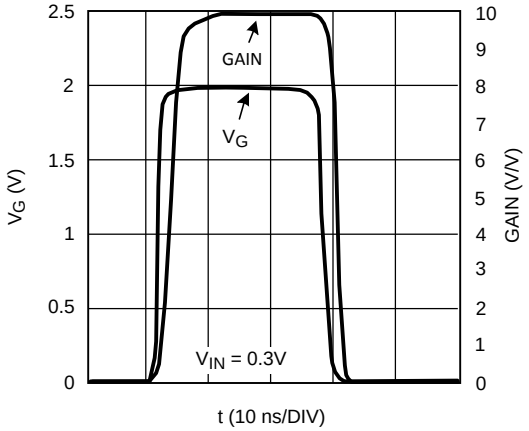


Figure 40.

APPLICATION INFORMATION

GENERAL DESCRIPTION

The key features of the LMH6505 are:

- Low power
- Broad voltage controlled gain and attenuation range (from A_{VMAX} down to complete cutoff)
- Bandwidth independent, resistor programmable gain range (R_G)
- Broad signal and gain control bandwidths
- Frequency response may be adjusted with R_F
- High impedance signal and gain control inputs

The LMH6505 combines a closed loop input buffer ("X1" Block in Figure 41), a voltage controlled variable gain cell ("MULT" Block) and an output amplifier ("CFA" Block). The input buffer is a transconductance stage whose gain is set by the gain setting resistor, R_G. The output amplifier is a current feedback op amp and is configured as a transimpedance stage whose gain is set by, and is equal to, the feedback resistor, R_F. The maximum gain, A_{VMAX}, of the LMH6505 is defined by the ratio: $K \cdot R_F/R_G$ where "K" is the gain multiplier with a nominal value of 0.940. As the gain control input (V_G) changes over its 0 to 2V range, the gain is adjusted over a range of about 80 dB relative to the maximum set gain.

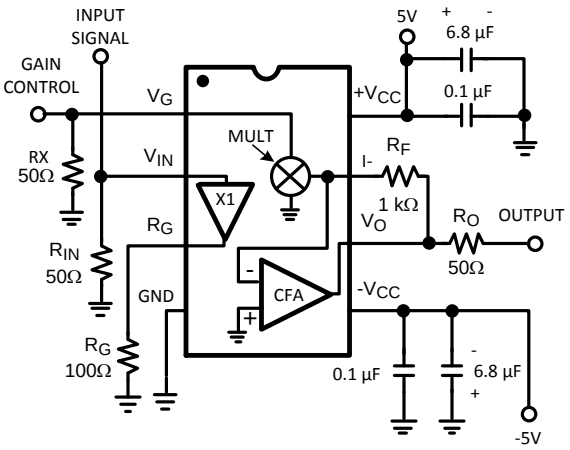


Figure 41. LMH6505 Typical Application and Block Diagram

SETTING THE LMH6505 MAXIMUM GAIN

$$A_{VMAX} = \frac{R_F}{R_G} \cdot K \quad (1)$$

Although the LMH6505 is specified at A_{VMAX} = 9.4 V/V, the recommended A_{VMAX} varies between 2 and 100. Higher gains are possible but usually impractical due to output offsets, noise and distortion. When varying A_{VMAX} several tradeoffs are made:

R_G: determines the input voltage range

R_F: determines overall bandwidth

The amount of current which the input buffer can source/sink into R_G is limited and is given in the I_{RG_MAX} specification. This sets the maximum input voltage:

$$V_{IN}\,(MAX) = I_{R_G\ MAX} \cdot R_G \quad (2)$$

As the I_{RG_MAX} limit is approached with increasing the input voltage or with the lowering of R_G, the device's harmonic distortion will increase. Changes in R_F will have a dramatic effect on the small signal bandwidth. The output amplifier of the LMH6505 is a current feedback amplifier (CFA) and its bandwidth is determined by R_F. As with any CFA, doubling the feedback resistor will roughly cut the bandwidth of the device in half.

For more about CFAs, see the basic tutorial, OA-20, *Current Feedback Myths Debunked*, (literature number SNOA376), or a more rigorous analysis, OA-13, *Current Feedback Amplifier Loop Gain Analysis and Performance Enhancements*, (literature number SNOA366).

OTHER CONFIGURATIONS

1. Single Supply Operation

   The LMH6505 can be configured for use in a single supply environment. Doing so requires the following:
   (a) Bias pin 4 and R_G to a "virtual half supply" somewhere close to the middle of V^+ and V^- range. The other end of R_G is tied to pin 3. The "virtual half supply" needs to be capable of sinking and sourcing the expected current flow through R_G.
   (b) Ensure that V_G can be adjusted from 0V to 2V above the "virtual half supply".
   (c) Bias the input (pin 2) to make sure that it stays within the range of 2V above V^- to 2V below V^+. See the Input Voltage Range specification in the Electrical Characteristics table. This can be accomplished by either DC biasing the input and AC coupling the input signal, or alternatively, by direct coupling if the output of the driving stage is also biased to half supply.

   Arranged this way, the LMH6505 will respond to the current flowing through R_G. The gain control relationship will be similar to the split supply arrangement with V_G measured with reference to pin 4. Keep in mind that the circuit described above will also center the output voltage to the "virtual half supply voltage."
2. Arbitrarily Referenced Input Signal

   Having a wide input voltage range on the input (pin 2) (±3V typical), the LMH6505 can be configured to control the gain on signals which are not referenced to ground (e.g. Half Supply biased circuits). This node will be called the "reference node". In such cases, the other end of R_G which is the side not tied to pin 3 can be tied to this reference node so that R_G will "look at" the difference between the signal and this reference only. Keep in mind that the reference node needs to source and sink the current flowing through R_G.

GAIN ACCURACY

Gain accuracy is defined as the actual gain compared against the theoretical gain at a certain V_G, the results of which are expressed in dB. (See Figure 42).

Theoretical gain is given by:

$$A(V/V) = K \times \frac{R_F}{R_G} \times \frac{1}{1 + e^{\left[\frac{N - V_G}{V_C}\right]}} \quad (3)$$

where

- K = 0.940 (nominal) N = 1.01V
- V_C = 79 mV at room temperature

For a V_G range, the value specified in the tables represents the worst case accuracy over the entire range. The "Typical" value would be the difference between the "Typical Gain" and the "Theoretical Gain." The "Max" value would be the worst case difference between the actual gain and the "Theoretical Gain" for the entire population.

GAIN MATCHING

As Figure 42 shows, gain matching is the limit on gain variation at a certain V_G, expressed in dB, and is specified as "±Max" only. There is no "Typical." For a V_G range, the value specified represents the worst case matching over the entire range. The "Max" value would be the worst case difference between the actual gain and the typical gain for the entire population.

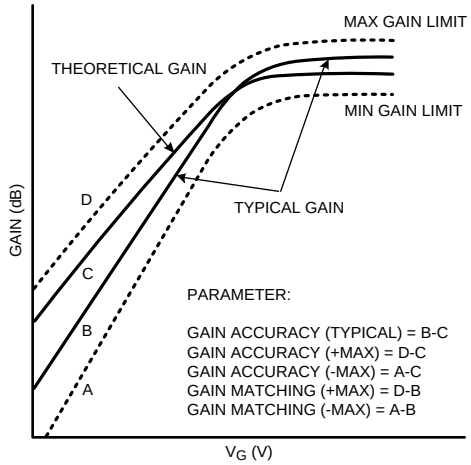


Figure 42. LMH6505 Gain Accuracy & Gain Matching Defined

GAIN PARTITIONING

If high levels of gain are needed, gain partitioning should be considered:

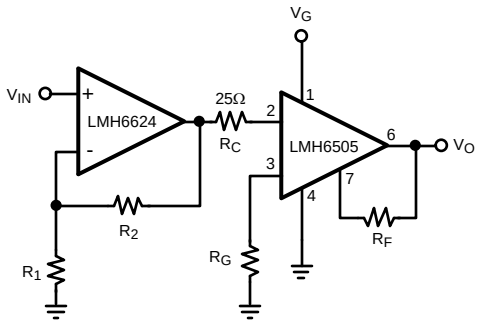


Figure 43. Gain Partitioning

The maximum gain range for this circuit is given by the following equation:

$$\text{MAXIMUM GAIN} = \left[1 + \frac{R_2}{R_1}\right] \cdot \left[\frac{R_F}{R_G}\right] \cdot K \tag{4}$$

The LMH6624 is a low noise wideband voltage feedback amplifier. Setting R_2 at 909Ω and R_1 at 100Ω produces a gain of 20 dB. Setting R_F at 1000Ω as recommended and R_G at 50Ω, produces a gain of about 26 dB in the LMH6505. The total gain of this circuit is therefore approximately 46 dB. It is important to understand that when partitioning to obtain high levels of gain, very small signal levels will drive the amplifiers to full scale output. For example, with 46 dB of gain, a 20 mV signal at the input will drive the output of the LMH6624 to 200 mV and the output of the LMH6505 to 4V. Accordingly, the designer must carefully consider the contributions of each stage to the overall characteristics. Through gain partitioning the designer is provided with an opportunity to optimize the frequency response, noise, distortion, settling time, and loading effects of each amplifier to achieve improved overall performance.

LMH6505 GAIN CONTROL RANGE AND MINIMUM GAIN

Before discussing Gain Control Range, it is important to understand the issues which limit it. The minimum gain of the LMH6505 is theoretically zero, but in practical circuits it is limited by the amount of feedthrough, here defined as the gain when V_G = 0V. Capacitive coupling through the board and package, as well as coupling through the supplies, will determine the amount of feedthrough. Even at DC, the input signal will not be completely rejected. At high frequencies feedthrough will get worse because of its capacitive nature. At frequencies below 10 MHz, the feed through will be less than −60 dB and therefore, it can be said that with A_{VMAX} = 20 dB, the gain control range is 80 dB.

LMH6505 GAIN CONTROL FUNCTION

In the plot, Gain vs. V_G (Figure 19), we can see the gain as a function of the control voltage. The “Gain (V/V)” plot, sometimes referred to as the S-curve, is the linear (V/V) gain. This is a hyperbolic tangent relationship and is given by Equation 3. The “Gain (dB)” plots the gain in dB and is linear over a wide range of gains. Because of this, the LMH6505 gain control is referred to as “linear-in-dB.”

For applications where the LMH6505 will be used at the heart of a closed loop AGC circuit, the S-curve control characteristic provides a broad linear (in dB) control range with soft limiting at the highest gains where large changes in control voltage result in small changes in gain. For applications requiring a fully linear (in dB) control characteristic, use the LMH6505 at half gain and below ($V_G \leq 1V$).

GAIN STABILITY

The LMH6505 architecture allows complete attenuation of the output signal from full gain to complete cutoff. This is achieved by having the gain control signal V_G “throttle” the signal which gets through to the final stage and which results in the output signal. As a consequence, the R_G pin's (pin 3) average current (DC current) influences the operating point of this “throttle” circuit and affects the LMH6505's gain slightly. Figure 44 below, shows this effect as a function of the gain set by V_G.

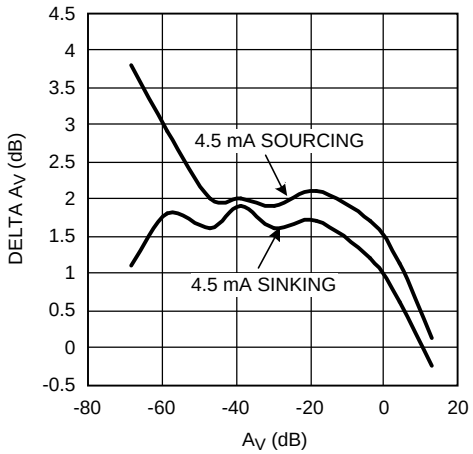


Figure 44. LMH6505 Gain Variation over R_G DC Current Capability vs. Gain

This plot shows the expected gain variation for the maximum R_G DC current capability (±4.5 mA). For example, with gain (A_V) set to −60 dB, if the R_G pin DC current is increased to 4.5 mA sourcing, one would expect to see the gain increase by about 3 dB (to −57 dB). Conversely, 4.5 mA DC sinking current through R_G would increase gain by 1.75 dB (to −58.25 dB). As you can see from Figure 44 above, the effect is most pronounced with reduced gain and is limited to less than 3.75 dB variation maximum.

If the application is expected to experience R_G DC current variation and the LMH6505 gain variation is beyond acceptable limits, please refer to the LMH6502 (Differential Linear in dB variable gain amplifier) datasheet instead at http://www.ti.com/lit/gpn/LMH6502.

AVOIDING OVERDRIVE OF THE LMH6505 GAIN CONTROL INPUT

There is an additional requirement for the LMH6505 Gain Control Input (V_G): V_G must not exceed +2.3V (with ±5V supplies). The gain control circuitry may saturate and the gain may actually be reduced. In applications where V_G is being driven from a DAC, this can easily be addressed in the software. If there is a linear loop driving V_G, such as an AGC loop, other methods of limiting the input voltage should be implemented. One simple solution is to place a 2.2:1 resistive divider on the V_G input. If the device driving this divider is operating off of ±5V supplies as well, its output will not exceed 5V and through the divider V_G can not exceed 2.3V.

IMPROVING THE LMH6505 LARGE SIGNAL PERFORMANCE

Figure 45 illustrates an inverting gain scheme for the LMH6505.

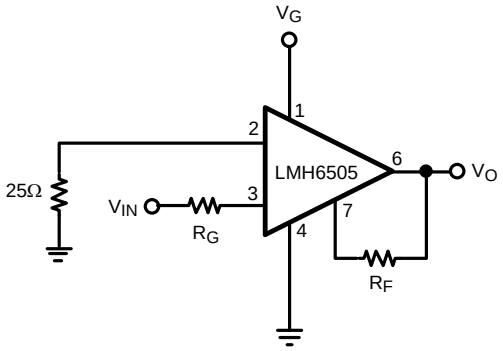


Figure 45. Inverting Amplifier

The input signal is applied through the R_G resistor. The V_{IN} pin should be grounded through a 25Ω resistor. The maximum gain range of this configuration is given in the following equation:

$$A_{VMAX} = -\left[\frac{R_F}{R_G}\right] \cdot K \tag{5}$$

The inverting slew rate of the LMH6505 is much higher than that of the non-inverting slew rate. This ≈ 2X performance improvement comes about because in the non-inverting configuration the slew rate of the overall amplifier is limited by the input buffer. In the inverting circuit, the input buffer remains at a fixed voltage and does not affect slew rate.

TRANSMISSION LINE MATCHING

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 46 shows a typical circuit configuration for matching transmission lines.

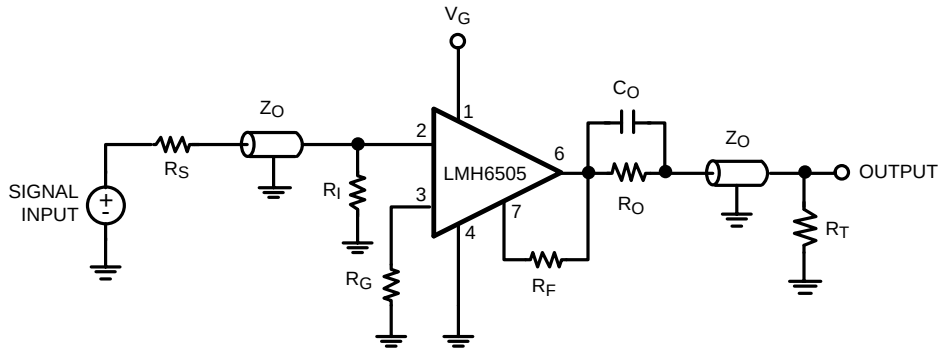


Figure 46. Transmission Line Matching

The resistors R_S, R_I, R_O, and R_T are equal to the characteristic impedance, Z_O, of the transmission line or cable. Use C_O to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp's output impedance with frequency.

MINIMIZING PARASITIC EFFECTS ON SMALL SIGNAL BANDWIDTH

The best way to minimize parasitic effects is to use surface mount components and to minimize lead lengths and component distance from the LMH6505. For designs utilizing through-hole components, specifically axial resistors, resistor self-capacitance should be considered. For example, the average magnitude of parasitic capacitance of RN55D 1% metal film resistors is about 0.15 pF with variations of as much as 0.1 pF between lots. Given the LMH6505's extended bandwidth, these small parasitic reactance variations can cause measurable frequency response variations in the highest octave. We therefore recommend the use of surface mount resistors to minimize these parasitic reactance effects.

RECOMMENDATIONS

Here are some recommendations to avoid problems and to get the best performance:

- Do not place a capacitor across R_F. However, an appropriately chosen series RC combination can be used to shape the frequency response.
- Keep traces connecting R_F separated and as short as possible.
- Place a small resistor (20-50Ω) between the output and C_L.
- Cut away the ground plane, if any, under R_G.
- Keep decoupling capacitors as close as possible to the LMH6505.
- Connect pin 2 through a minimum resistance of 25Ω.

ADJUSTING OFFSETS AND DC LEVEL SHIFTING

Offsets can be broken into two parts: an input-referred term and an output-referred term. These errors can be trimmed using the circuit in Figure 47. First set V_G to 0V and adjust the trim pot R_4 to null the offset voltage at the output. This will eliminate the output stage offsets. Next set V_G to 2V and adjust the trim pot R_1 to null the offset voltage at the output. This will eliminate the input stage offsets.

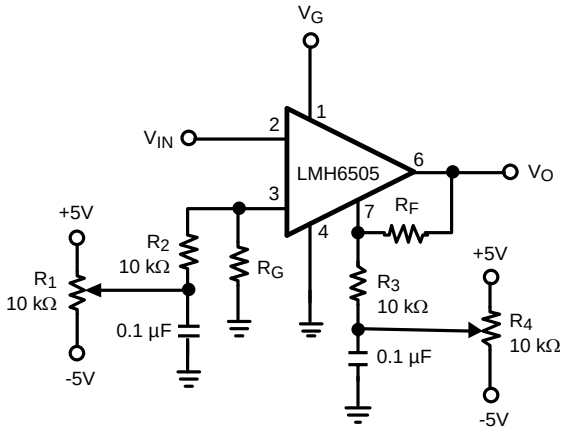


Figure 47. Offset Adjust Circuit

DIGITAL GAIN CONTROL

Digitally variable gain control can be easily realized by driving the LMH6505 gain control input with a digital-to-analog converter (DAC). Figure 48 illustrates such an application. This circuit employs TI's eight-bit DAC0830, the LMC8101 MOS input op amp (Rail-to-Rail Input/Output), and the LMH6505 VGA. With V_{REF} set to 2V, the circuit provides up to 80 dB of gain control in 256 steps with up to 0.05% full scale resolution. The maximum gain of this circuit is 20 dB.

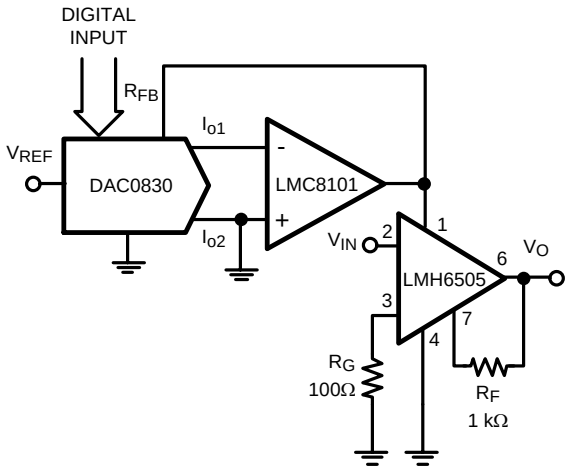


Figure 48. Digital Gain Control

USING THE LMH6505 IN AGC APPLICATIONS

In AGC applications, the control loop forces the LMH6505 to have a fixed output amplitude. The input amplitude will vary over a wide range and this can be the issue that limits dynamic range. At high input amplitudes, the distortion due to the input buffer driving R_G may exceed that which is produced by the output amplifier driving the load. In the plot, THD vs. Gain, total harmonic distortion (THD) is plotted over a gain range of nearly 35 dB for a fixed output amplitude of 0.25 V_{PP} in the specified configuration, R_F = 1 kΩ, R_G = 100Ω. When the gain is adjusted to −15 dB (i.e. 35 dB down from A_{VMAX}), the input amplitude would be 1.41 V_{PP} and we can see the distortion is at its worst at this gain. If the output amplitude of the AGC were to be raised above 0.25 V_{PP}, the input amplitudes for gains 40 dB down from A_{VMAX} would be even higher and the distortion would degrade further. It is for this reason that we recommend lower output amplitudes if wide gain ranges are desired. Using a post-amp like the LMH6714/LMH6720/LMH6722 family or the LMH6702 would be the best way to preserve dynamic range and yield output amplitudes much higher than 100 mV_{PP}. Another way of addressing distortion performance and its limitations on dynamic range, would be to raise the value of R_G. Just like any other high-speed amplifier, by increasing the load resistance, and therefore decreasing the demanded load current, the distortion performance will be improved in most cases. With an increased R_G, R_F will also have to be increased to keep the same A_{VMAX} and this will decrease the overall bandwidth. It may be possible to insert a series RC combination across R_F in order to counteract the negative effect on BW when a large R_F is used.

AUTOMATIC GAIN CONTROL (AGC)

Fast Response AGC Loop

The AGC circuit shown in Figure 49 will correct a 6 dB input amplitude step in 100 ns. The circuit includes a two op amp precision rectifier amplitude detector (U1 and U2), and an integrator (U3) to provide high loop gain at low frequencies. The output amplitude is set by R_9. The following are some suggestions for building fast AGC loops: Precision rectifiers work best with large output signals. Accuracy is improved by blocking DC offsets, as shown in Figure 49.

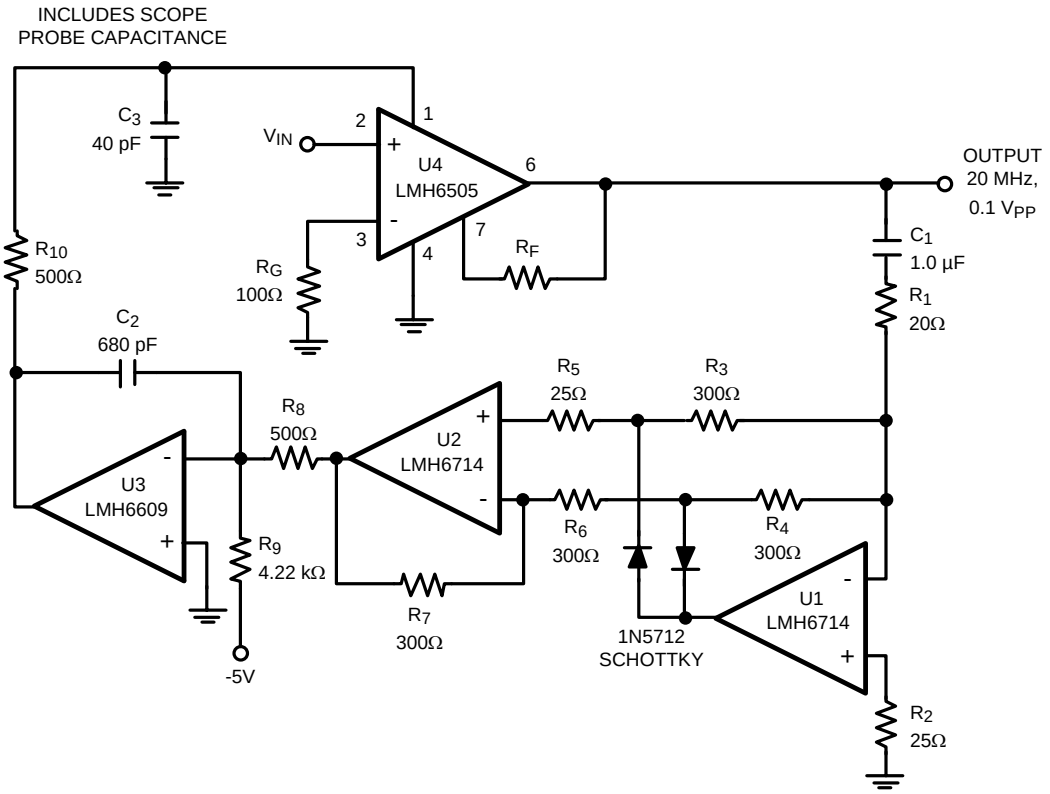


Figure 49. Automatic Gain Control Circuit

Signal frequencies must not reach the gain control port of the LMH6505, or the output signal will be distorted (modulated by itself). A fast settling AGC needs additional filtering beyond the integrator stage to block signal frequencies. This is provided in Figure 49 by a simple R-C filter (R_{10} and C_3); better distortion performance can be achieved with a more complex filter. These filters should be scaled with the input signal frequency. Loops with slower response time, which means longer integration time constants, may not need the $R_{10} – C_3$ filter.

Checking the loop stability can be done by monitoring the V_G voltage while applying a step change in input signal amplitude. Changing the input signal amplitude can be easily done with an arbitrary waveform generator.

CIRCUIT LAYOUT CONSIDERATIONS & EVALUATION BOARDS

A good high frequency PCB layout including ground plane construction and power supply bypassing close to the package is critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the I⁻ input (pin 7) so it is best to keep the node trace area small. Shunt capacitance across the feedback resistor should not be used to compensate for this effect. Capacitance to ground should be minimized by removing the ground plane from under the body of R_G. Parasitic or load capacitance directly on the output (pin 6) degrades phase margin leading to frequency response peaking.

The LMH6505 is fully stable when driving a 100Ω load. With reduced load (e.g. 1k.) there is a possibility of instability at very high frequencies beyond 400 MHz especially with a capacitive load. When the LMH6505 is connected to a light load as such, it is recommended to add a snubber network to the output (e.g. 100Ω and 39 pF in series tied between the LMH6505 output and ground). C_L can also be isolated from the output by placing a small resistor in series with the output (pin 6).

Component parasitics also influence high frequency results. Therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended.

Texas Instruments suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6505	SOIC	LMH730066

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6505MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 05MA	Samples
LMH6505MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 05MA	Samples
LMH6505MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AZ2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

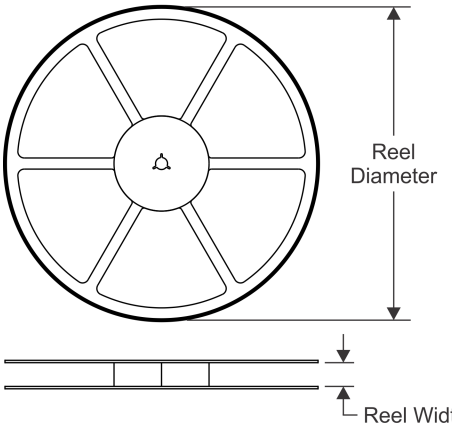
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

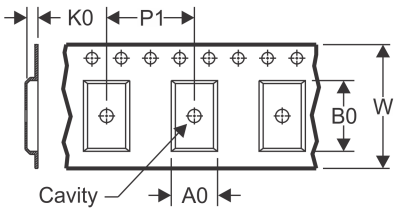
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

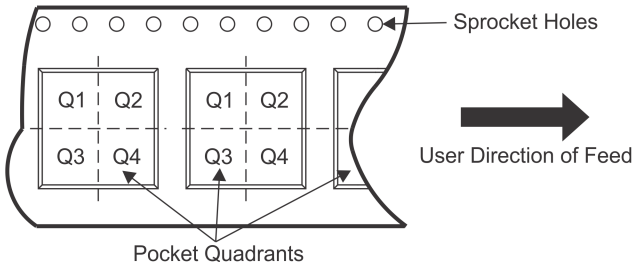


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

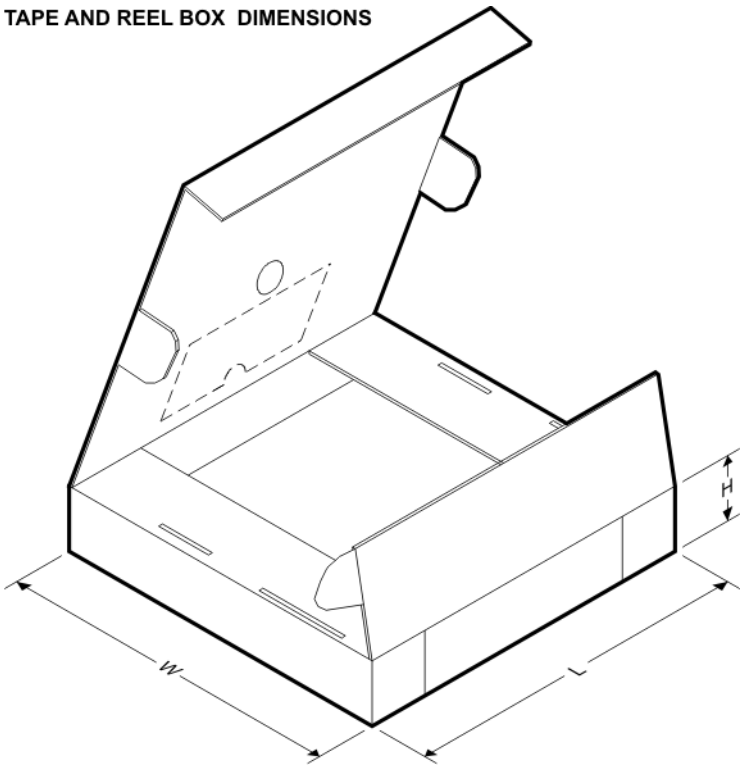
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6505MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6505MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

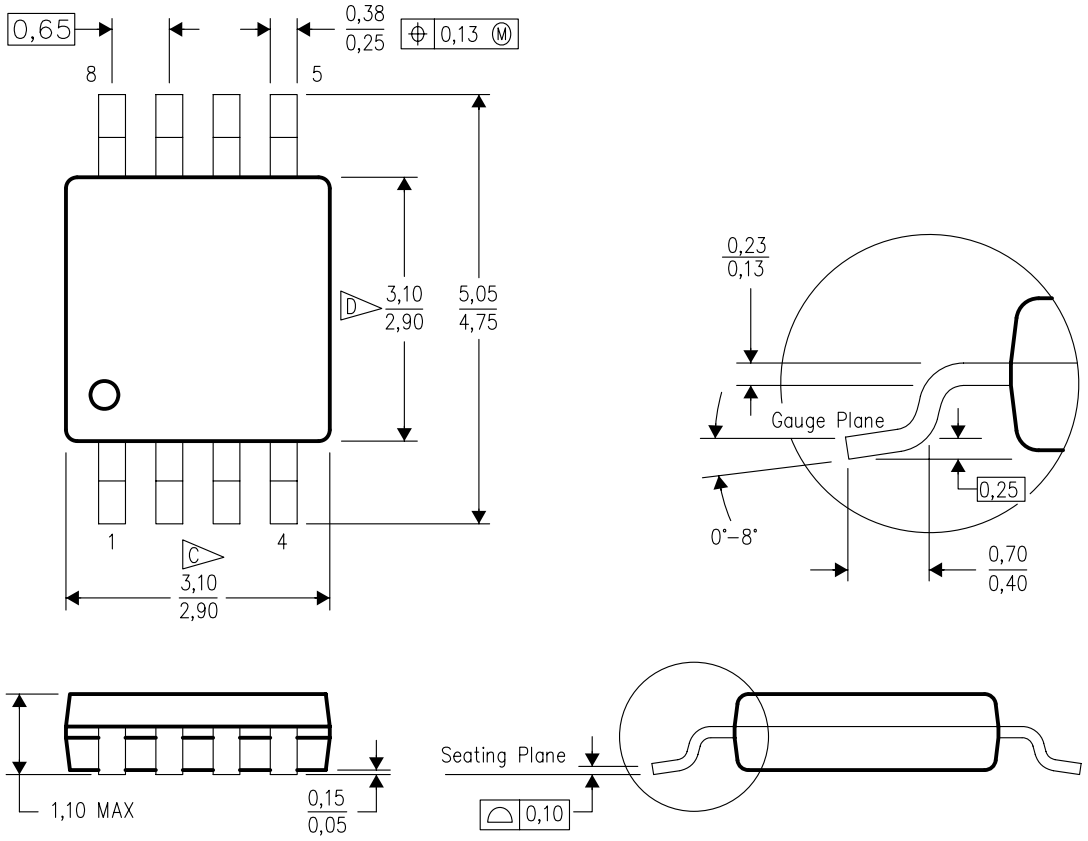
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6505MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6505MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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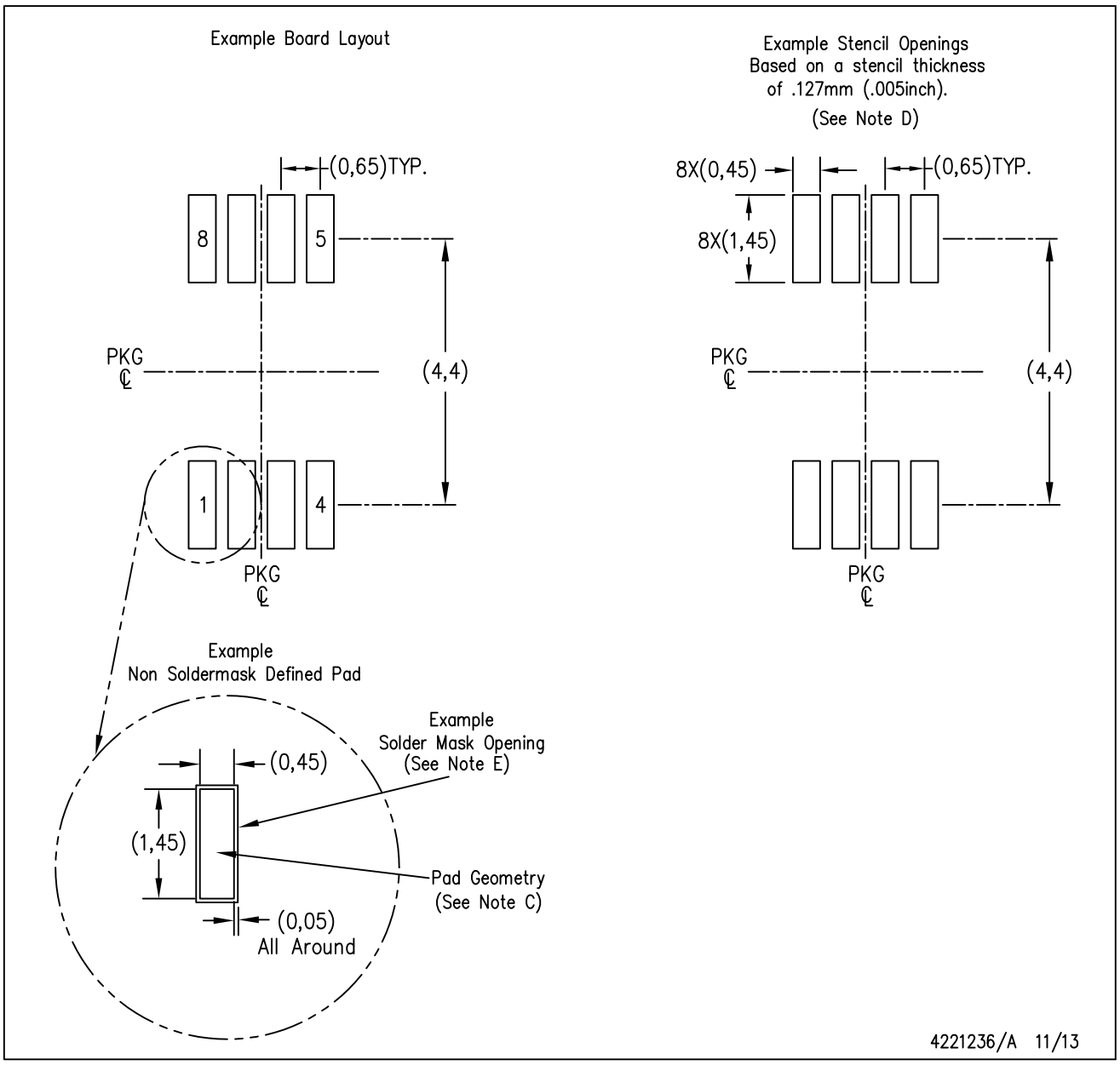
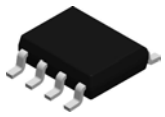
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

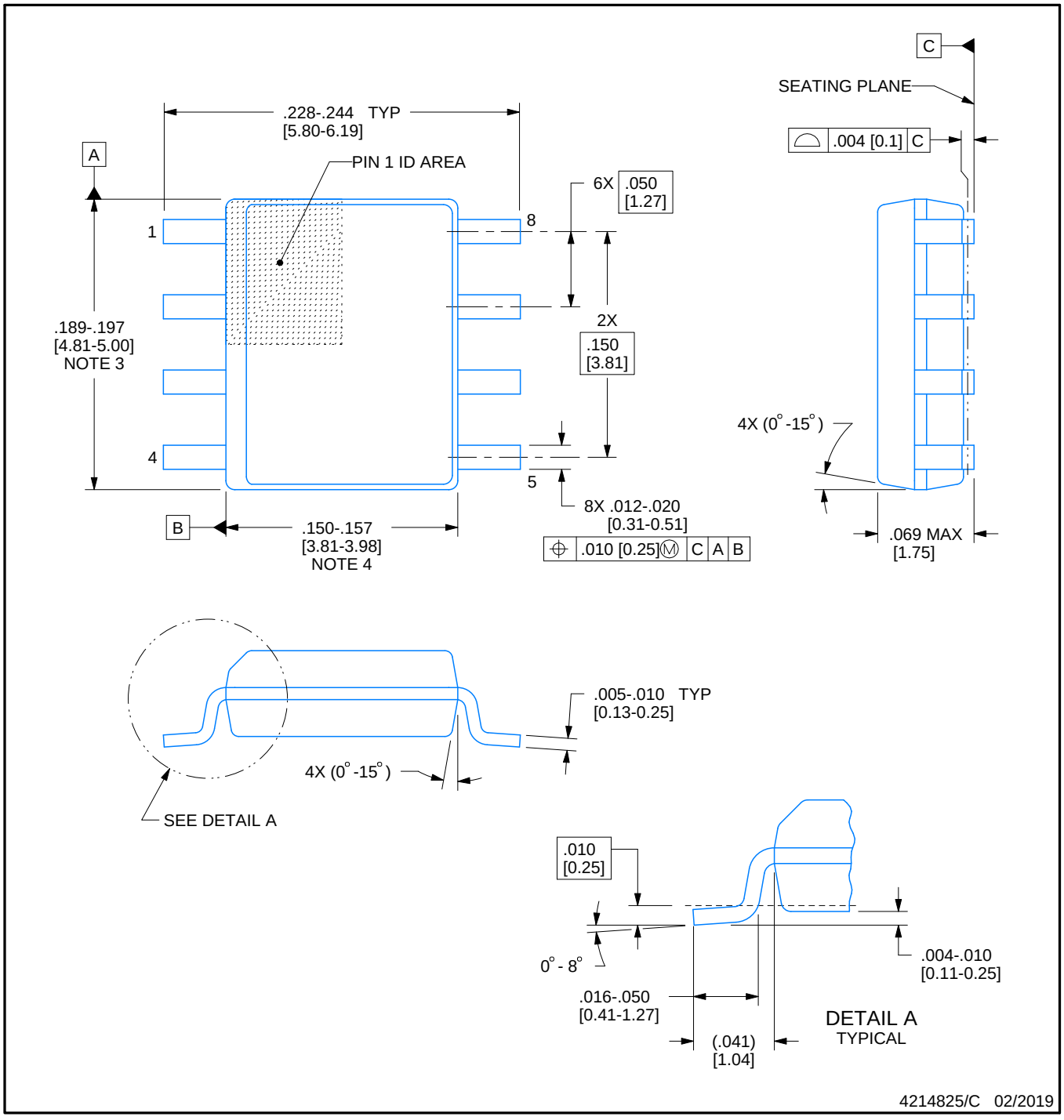


PACKAGE OUTLINE

D0008A

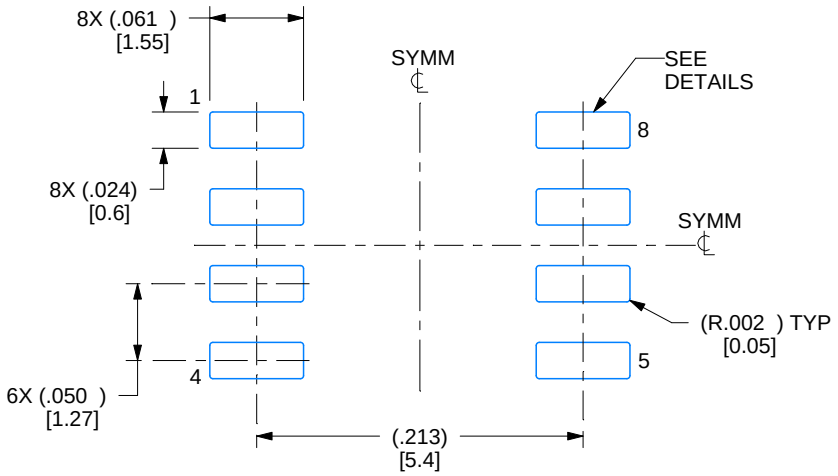
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

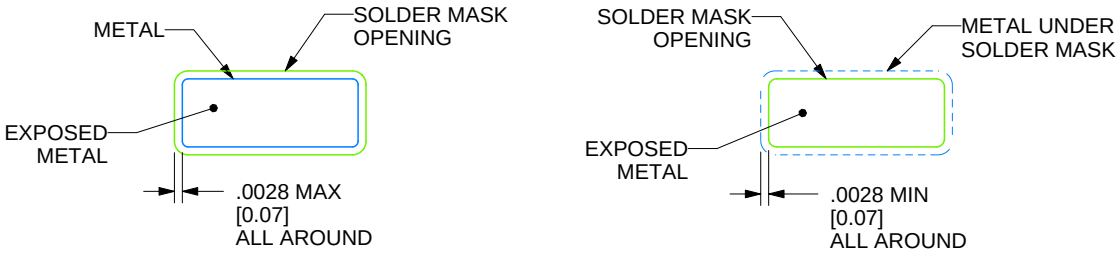


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

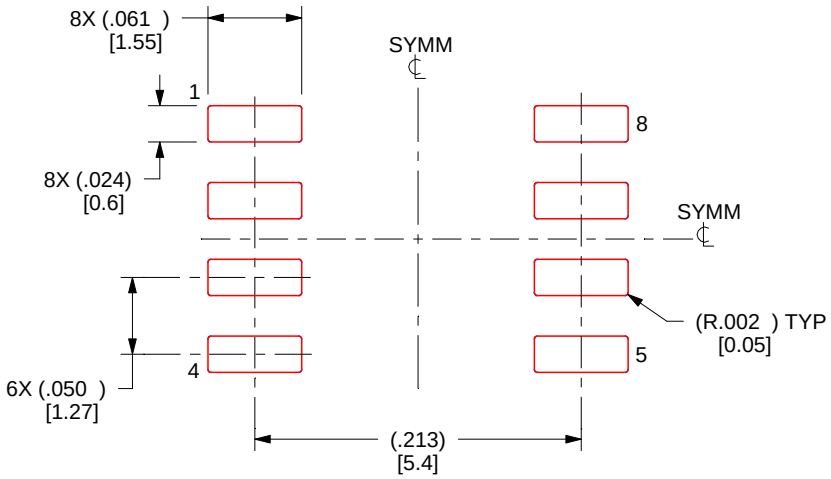
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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