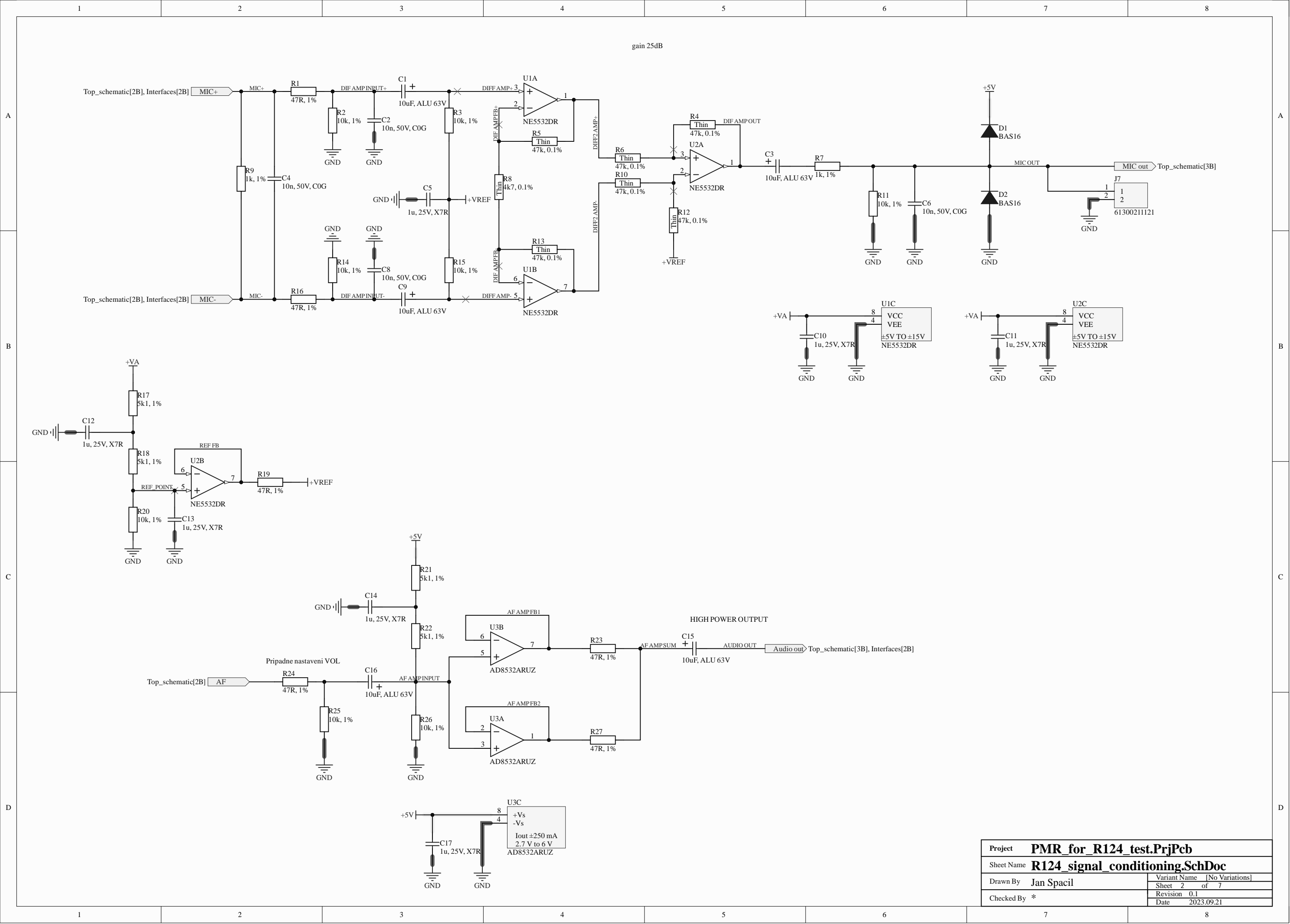


Project PMR_for_R124_test.PrjPcb	
Sheet Name Top_schematic.SchDoc	
Drawn By Jan Spacil	Variant Name [No Variations]
	Sheet 1 of 7
Checked By *	Revision 0.1
	Date 2023.09.21



Project		PMR_for_R124_test.PrjPcb	
Sheet Name		R124_signal_conditioning.SchDoc	
Drawn By	Jan Spacil	Variant Name	[No Variations]
		Sheet	2 of 7
Checked By	*	Revision	0.1
		Date	2023.09.21

A

B

C

D

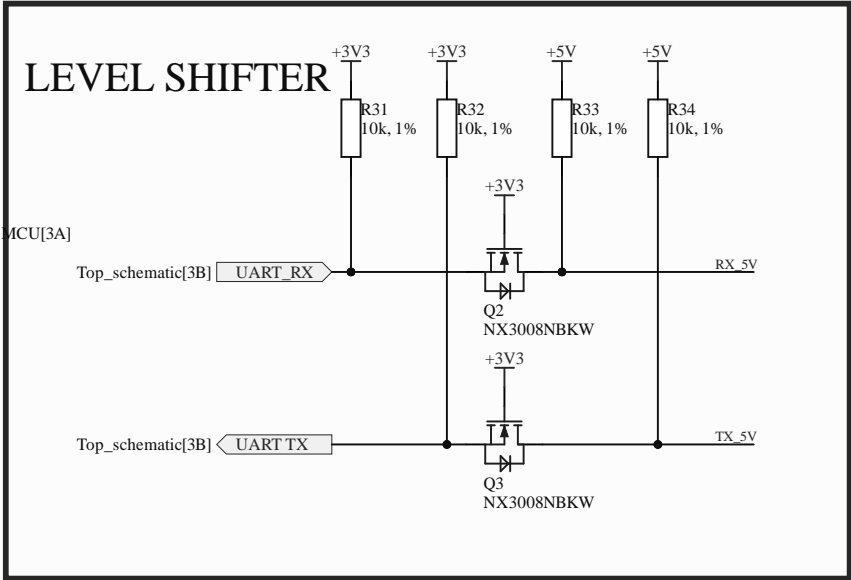
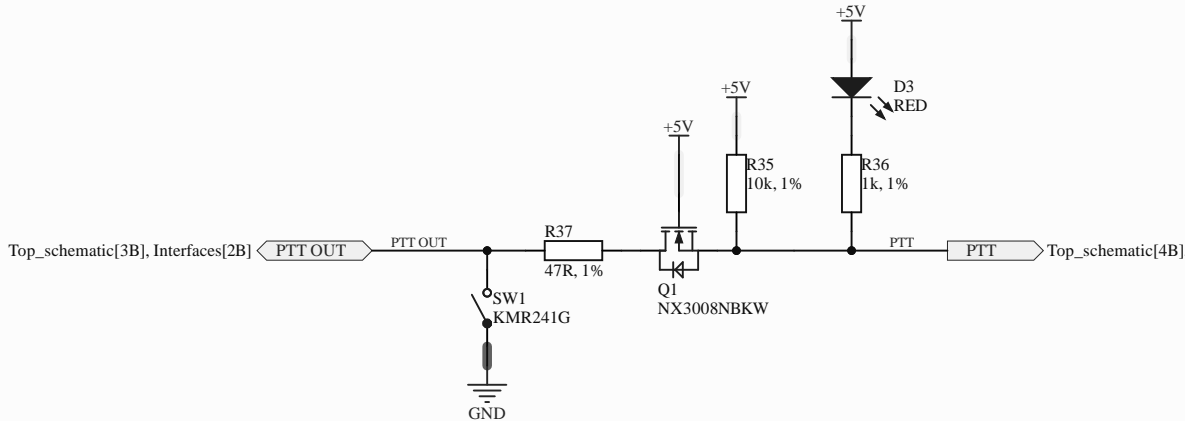
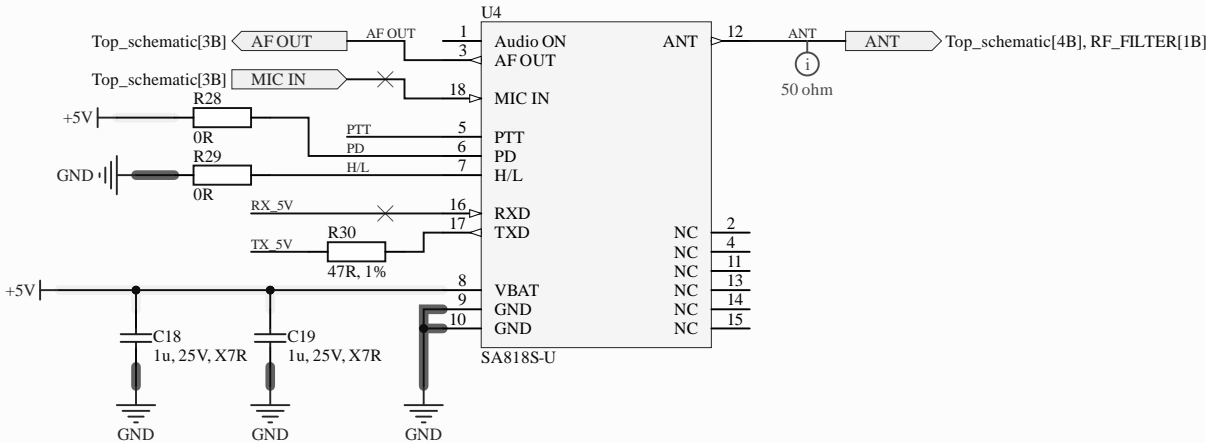
A

B

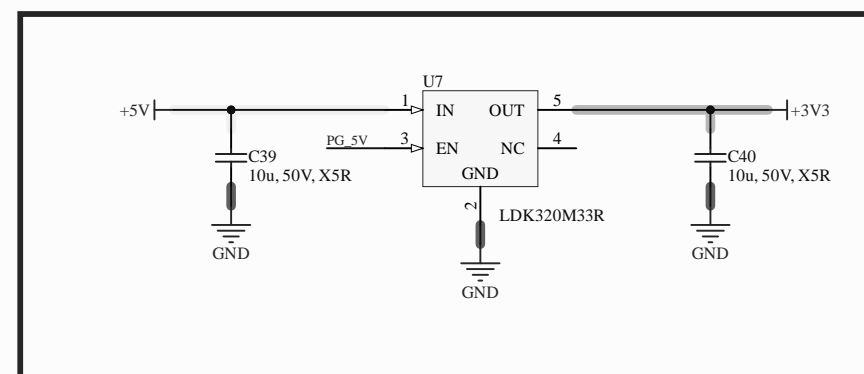
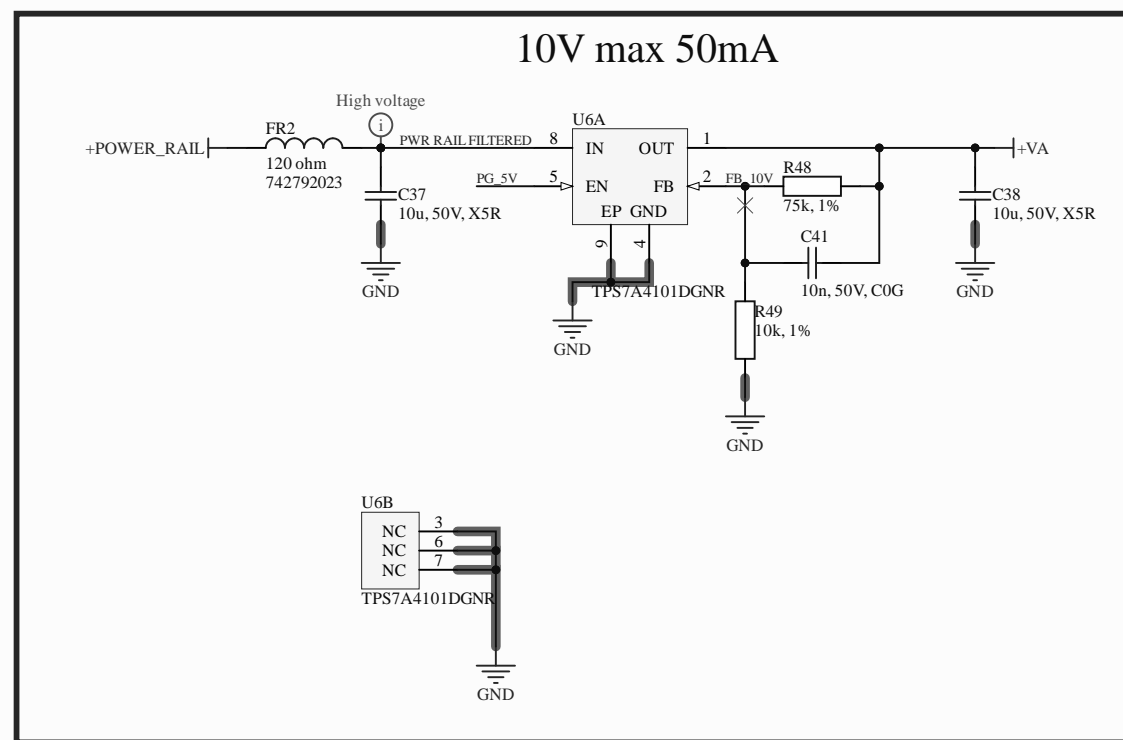
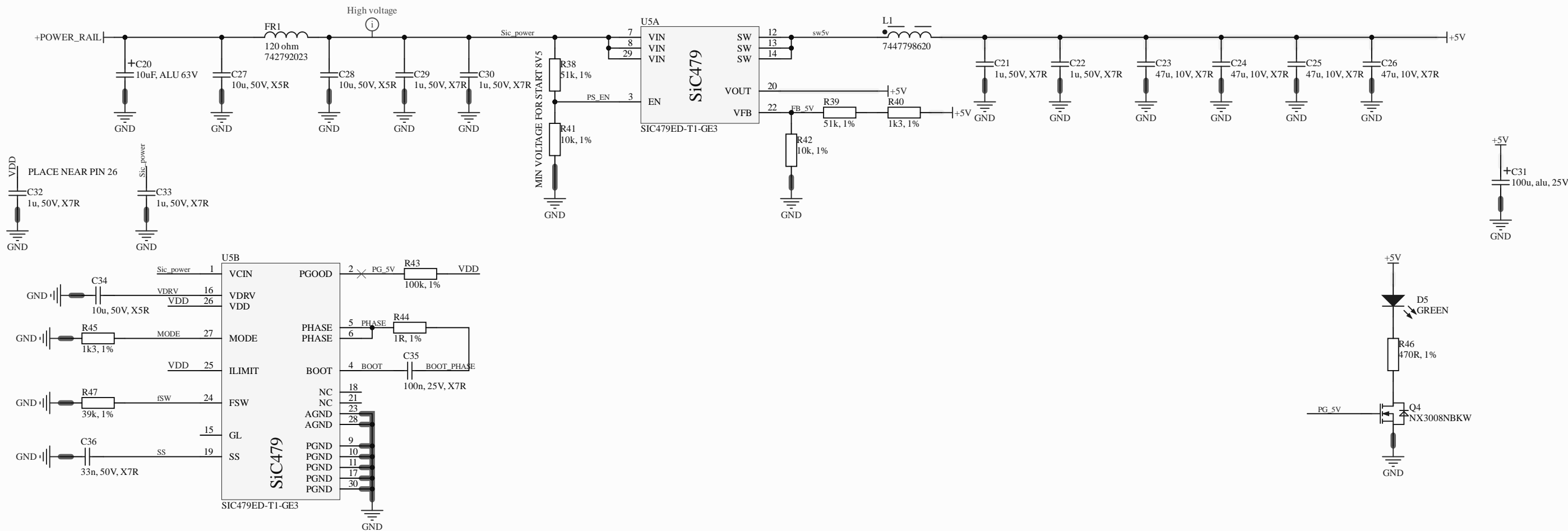
C

D

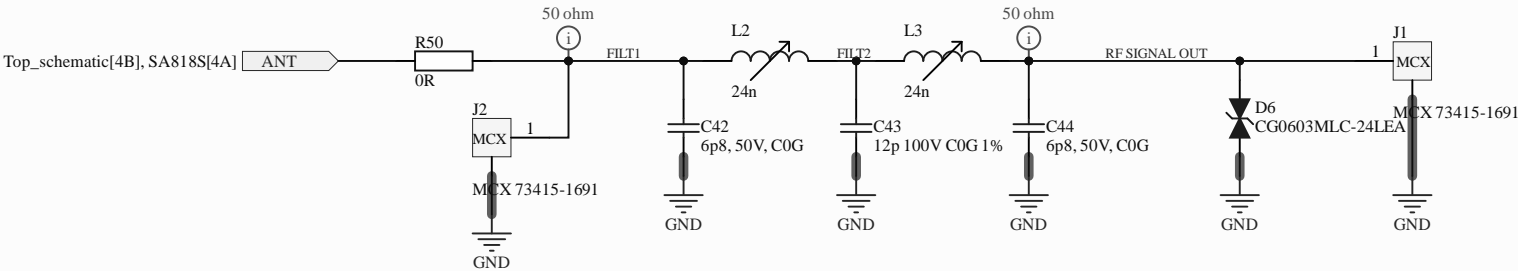
Module Input,
Transmitting/receiving control,
"0" force the module to enter TX
state; and "1" to Rx state



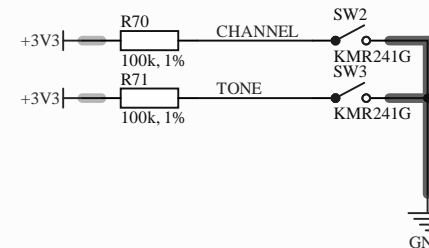
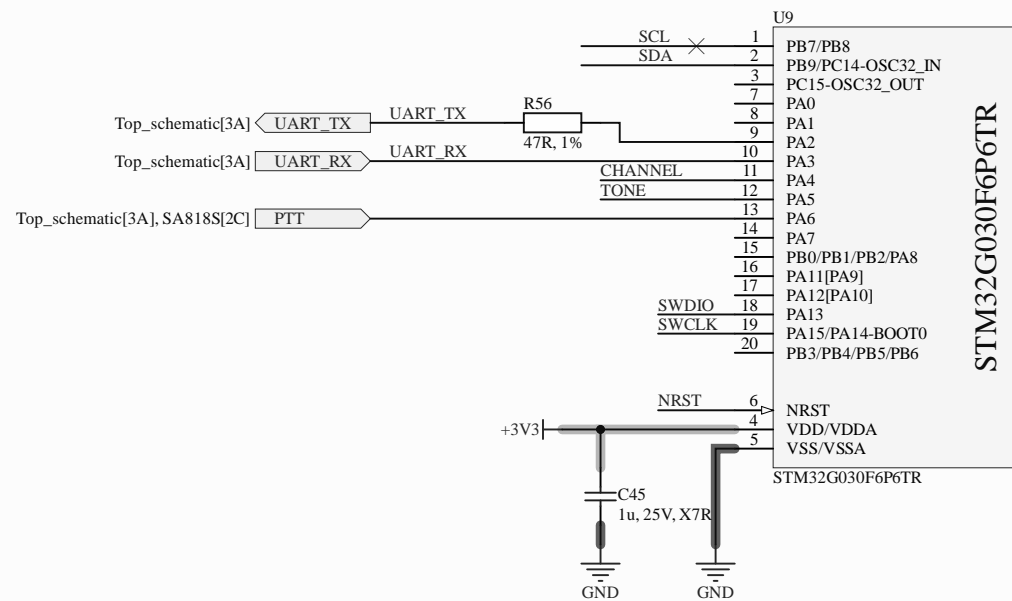
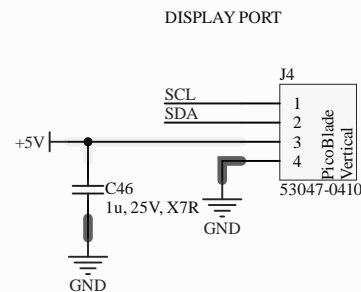
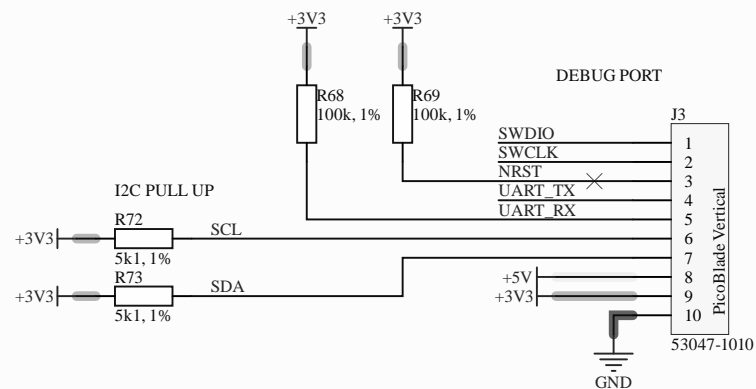
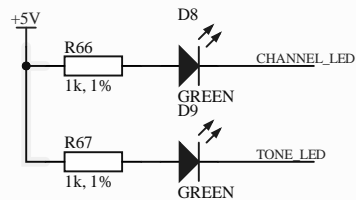
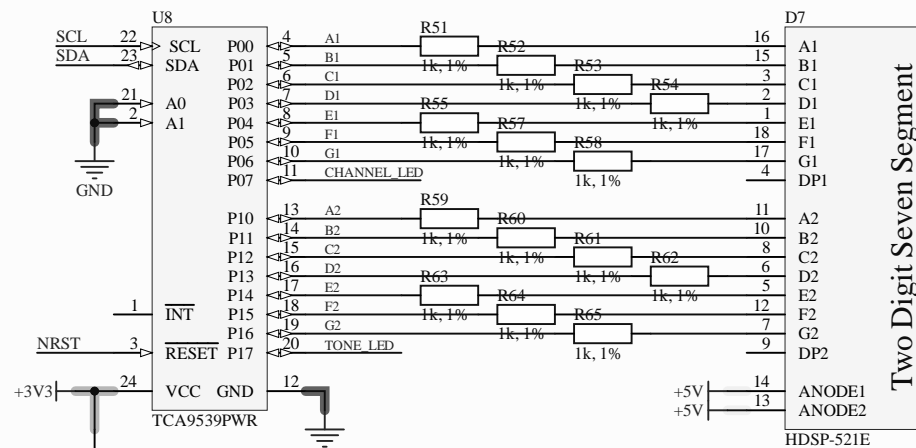
Project PMR for R124 test.PrjPcb	
Sheet Name SA818S.SchDoc	
Drawn By Jan Spacil	Variant Name [No Variations]
	Sheet 3 of 7
Checked By *	Revision 0.1
	Date 2023.09.21



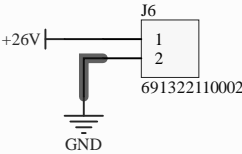
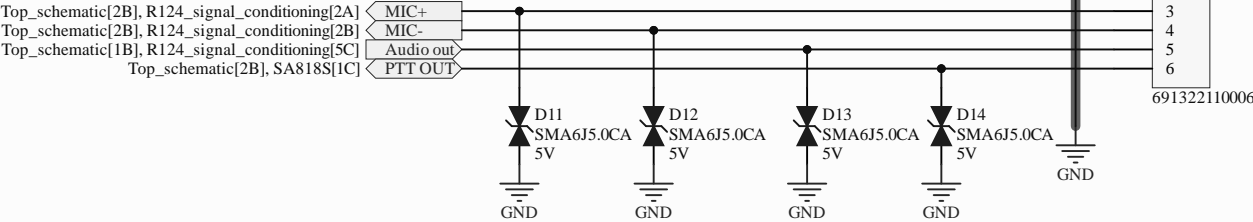
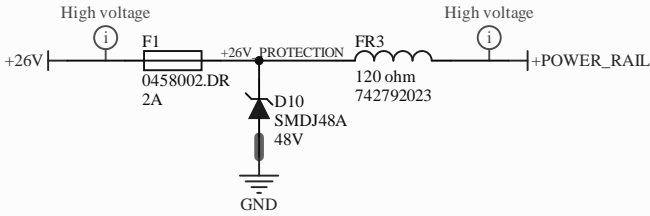
Project	PMR_for_R124_test.PrpPcb		
Sheet Name	Power.SchDoc		
Drawn By	Jan Spacil	Variant Name	[No Variations]
		Sheet	4 of 7
Checked By	*	Revision	0.1
		Date	2023.09.21



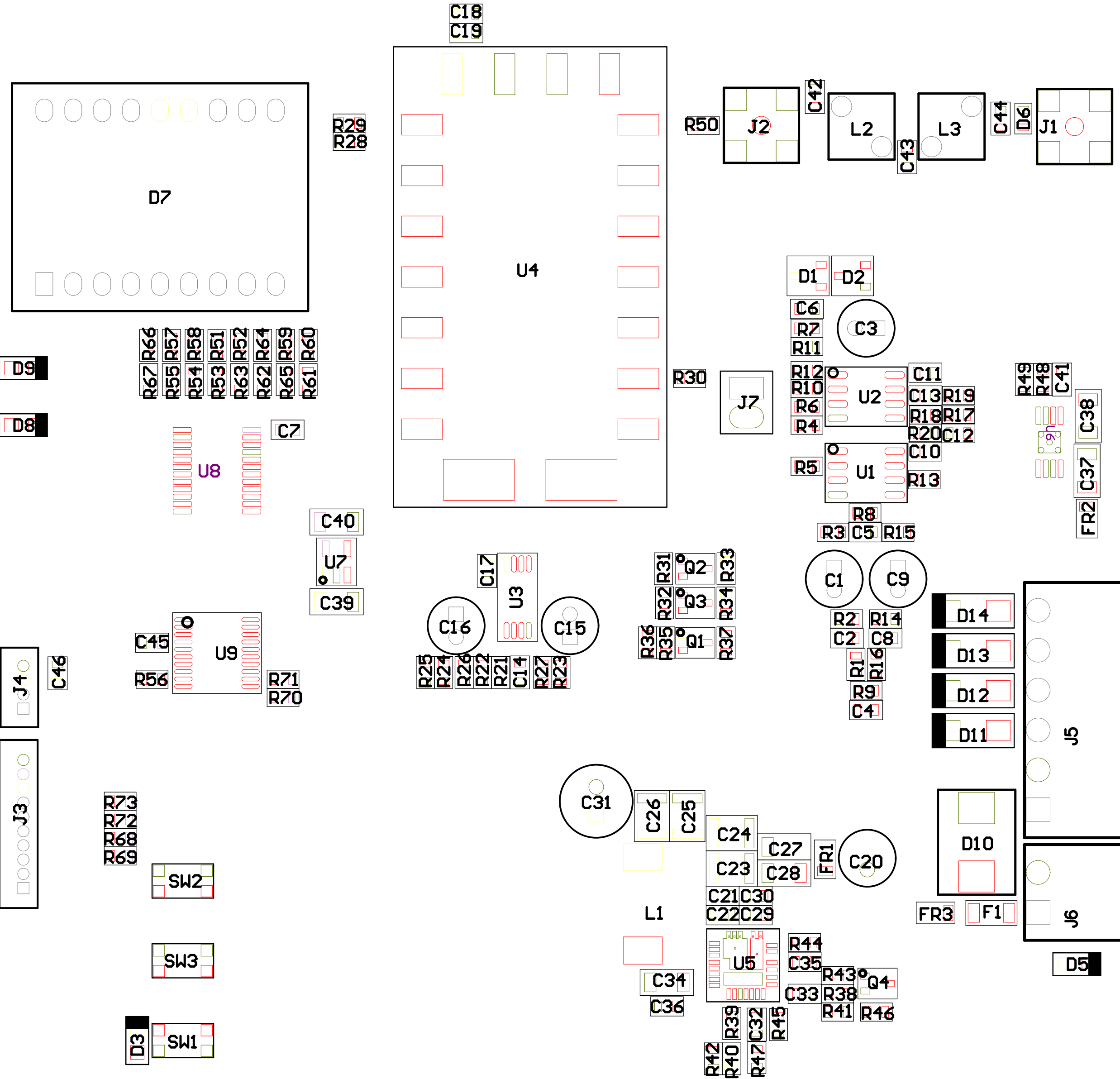
Project		PMR_for_R124_test.PrjPcb	
Sheet Name		RF_FILTER.SchDoc	
Drawn By	Jan Spacil	Variant Name [No Variations]	
		Sheet 5 of 7	
Checked By *		Revision 0.1	
		Date 2023.09.21	

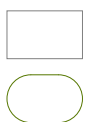
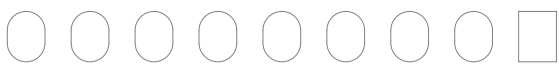
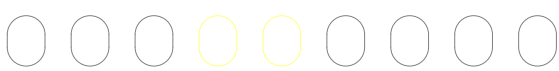
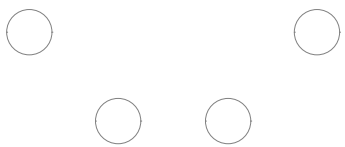


Project	PMR_for_R124_test.PrfPcb		
Sheet Name	MCU.SchDoc		
Drawn By	Jan Spacil	Variant Name	[No Variations]
		Sheet 6	of 7
Checked By	*	Revision	0.1
		Date	2023.09.21



Project		PMR_for_R124_test.PrjPcb	
Sheet Name		Interfaces.SchDoc	
Drawn By	Jan Spacil	Variant Name [No Variations]	
		Sheet 7 of 7	
Checked By	*	Revision 0.1	
		Date 2023.09.21	





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