

# Multek Design Guidelines

## Rigid PCB Fabrication

**DFM-MDG-01-K**

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# Multek Design Guidelines – Rigid PCB Fabrication

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## Approvals

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## Revision History

REV	DESCRIPTION OF CHANGE	ORIGINATOR	RELEASE DATE
A	Original Publication Revised BGA artwork, IL Graphics, etc. Change PTH to plane, RCC, BGA table, etc.	Glen Walther	6/13/2002
B	Complete re-write of the PCB Guidelines	Ric Stanley	5/12/2003
C	Corrections to HDI guideline Section B	Ric Stanley	9/14/2003
D	Corrected FHS for Brazil	Ric Stanley	10/20/2003
E	Multek "watermark" added	Ric Stanley	12/17/2003
F	New resistor formula, laser hole size change	Ric Stanley	5/12/2004
G	Revised documentation	Steve Morris	4/15/2005
H	Revised documentation	Steve Morris	6/30/2008
I	Converted & Release into DMS format	Darren Hitchcock	3/11/2009
J	Updated capabilities / minor adjustments. Change document number from TLG-ENG-1-007-00 to ATG-ENG-1-021	Darren Hitchcock	8/31/2009
K	Complete Rewrite of the Guidelines including the addition of Facility Capability Survey for All Rigid PCB Factories	Todd Robinson & Holle Galyon	01/08/2014

## Change History

Date	Change Summary
3/25/02	Original publication, Owner/Author, Glen Walther, Multek, Inc., Irvine, Ca.92618
4/02/02	Revise BGA artwork p.15, Glen Walther
4/19/02	Revise I/L graphics pgs 18 ,19 & 26. Glen Walther
6/13/02	Change "C" Drilled PTH to Plane, Standard from 0.012" to 0.010" pg 17. G. Walther Change RCC resin thickness from 50/50 to 35/35, pg 11, G. Walther Add "dm," drill margin and "T" thickness to Mechanical Blind graphic & table., G. Walther Update I/L BGA Geometry Tables, pages 18, 19, & 20. G. Walther
5/12/03	Complete re-write of the PCB Guidelines Ric Stanley Illustrations Ric Stanley
9/14/03	Correction to the HDI guideline section B. (Rev C)
10/20/03	Corrected finished hole size for Brazil from .008" to .010" pg 18 (Rev D)
12/17/03	Added Multek "watermark" to complete document. (Rev E)
05/12/04	Added new planar resistor formula to page 67. (Rev. F)
05/12/04	Changed laser drilled hole size from .008" standard to .010" preferred; .008" advanced. Pg 29 (Rev F)
05/12/04	Added UL 796 to un-pierced copper area changing the 5.00" standard to an example. Pg. 44
05/12/04	Removed Thermount and Polyimide from special materials. Pg 14
04/15/05	Revised documentation (Rev G) S. Morris
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## 1. FORWARD

This document is a guideline for understanding capabilities within the Multek family of Rigid Manufacturing facilities. This document is designed to provide Multek customers a vantage point into which facility would best suit their requirements.

This design guide will concentrate on how the customer can obtain the highest yields at the lowest cost. Design techniques and capability details show how to obtain the most robust designs using Multek's standard processes. This guide will also outline some areas that are "Advance Technology" and understanding that these processes are capable within Multek to support specific design challenges, there may be a cost impact.

Multek is a global supplier of rigid, flexible and rigid/flex printed circuit board. For detail on these locations, please visit the following link to [Facility Locations](#) for additional details. For our advanced technology capabilities, Multek recommended that you discuss these requirements with our [Field Applications Engineering](#) (FAE). Please note that this is a guide to all of Multek's capabilities and not all facilities are capable of meeting some of the advanced technology capabilities of other Multek facilities. The FAE team is available to address any questions you may have and help in determining which fabrication facility will meet your technical and business needs. For business related support, please contact a [Business Development Manager](#) in your area. Information contained in this document is subject to change, without notice. If any clarification or additional input is required, please contact Multek Sales or Technical support in your area.

Multek FAE team member in your area can address any questions regarding this document. For contact information, please visit the following link: [Multek – FAE Support](#)

## 2. DATA TRANSMISSION

FTP access to <ftp.multek.com>

Transmission of data in a timely manner is critical to the process. Customers have 24-hour access to the Multek ftp sites. Multek will assign a private FTP account for each customer as required.

Your secure FTP account can be created by contacting either your local sales representative or FAE team member. A document or email with detailed instructions on how to access the FTP site upon completion of the account setup. Multek recommend planning 24 ahead to ensure account setup is completed.

Email is not a recommended secure method of transferring any data packages international. Limitation in file size over 10 MB and mailbox capacity can hinder file transfer.

## 3. INCOMING DATA REQUIREMENTS

Communication is critical to meeting quality, reliability, and delivery expectations. The PWB designer has months and sometimes years to be familiar with the details and requirements of the design. The PWB fabricator most often only has hours to understand the same details and requirements. Concise, complete, and accurate documentation and data files are very important to ensure the clear communication to the fabricator and assembler of the PWB.

See the DATA PACKAGE CHECKLIST section for requirements and recommendations to make a complete Data Package to be sent with each design.

Multek support the industry standard data formats used in today. The preferred format is ODB++, but other supported formats are Gerber, IPC and standard NC data formats. Multek recommends the ODB++ format, as it contains all the required information for fabrication of the PCB. ODB++ will optimize the efficiencies of the CAM process.

Multek does accept data in other formats as outlined in the section below. The objective is to achieve 100% data compatibility and in most cases, time is of the essence to begin producing your product. By adhering to the rules set forth below, Multek will ensure a timely analysis of your data with direct feedback of any issues.

See the DATA AND DOCUMENTATION FORMATTING and DATA PACKAGING sections for a list of formats for the various files as well as compression and file transfer methods.

Use this document as a guideline for preparing data and documentation when issuing orders to Multek.

### **3.1. DATA PACKAGE CHECKLIST**

- Readme.txt – Including Contact information for Engineering and Purchasing
- Copper Layer(s)
- Solder Mask Layer(s)
- Silkscreen Layer(s)
- Drill File(s)
- Profile (outline)
- Netlist
- Fabrication Drawing
- Assembly Array Drawing – this is not required if boards ship as single routed individual parts
- Solder Paste Layer(s) – recommended but not required
- Epoxy Via Fill Layer(s) – optional
- Solder Mask Plugging Layer(s) – optional
- OEM General PWB Specification – optional
- Aperture List (not needed if an embedded format is used like RS274X or ODB++)

## **4. DATA AND DOCUMENTATION FORMATTING**

### **4.1. README**

The Readme file is very important. It provides important information to the person receiving the data package. It should contain the following:

- Contact information for individuals responsible for Data Transfer, Business Questions and Technical Questions
- A list of all the files contained in the compressed data package
- Include any special merge instructions
- Include a detailed description of how each file is to be used
- Company Name, Part Number, Date
- List any known Netlist errors that can be ignored.
- For Example: AGND is intentionally shorted to DGND and will generate a Netlist error. Please ignore the AGND to DGND short.

The file should be in a common readable format, such as ASCII, PDF, or Word document.

### **4.2. NETLIST**

It is highly recommended that a Netlist generated from the CAD system is sent with the electronic data files. This allows Multek to perform a check of the CAM data against a master CAD Netlist from the design system. Netlist compares are done to ensure data translation from the CAD output is accurate. Multek does not guarantee the electrical integrity of the design at any point, but utilizes this Netlist compare as a check to ensure

data integrity. If a netlist is not provided, Multek will generate a Netlist based on the net connections in the Gerber and NC Drill files. This netlist will become the reference netlist of record for all associated CAM work post generation.

## Netlist Formats

Preferred Format	Alternative Formats Accepted
ODB++	IPC-D-356
IPC-D-356A	Mentor Neutral Format Cadence Allegro Format

## 4.3. ARTWORK DATA

The electronic data files should contain the artwork files for each of the items listed below. Please follow IPC conventions by having Layer 1 for the top side of the board. Multek recommends removing the board profile/outline from each layer and have it detailed as a separate layer for easier reference. All layers are as viewed from the top side through the board and should be aliened to each other.

- Copper Layer(s)
- Positive data for all signal layers
- Positive data for all external layers
- Positive data for all plated layers, including internal signal or plane layers that use blind or buried via technology.
- Negative data for internal plane layers is recommended. Positive plane data will influence the file size and CAM throughput.
- Solder Mask Layer(s)
- Silkscreen Layer(s)
- Solder Paste Layer(s)
- Epoxy Via Fill Layer(s) – optional
- Solder Mask Plugging Layer(s)
- Selective Gold Layer(s) for PCBs with more than one surface finish.
- Board Outline Layer – Separate file from other layers to be used as reference for outline routing.
- Special mechanical requirement layers such as plated slots or cutouts that are unique from the board outline.

## Artwork Data

Preferred Format	Alternative Formats Accepted
ODB++	Gerber 274D (with Aperture List)
Gerber 274X	AutoCAD DWG or DFX

## 4.4. NC DATA

Include a NC file for each of the following mechanical requirements:

### Drill File(s)

- 1 NC Drill file for each set of layers being drilled
  - A single files for each drill requirement (Through Hole, Blind, Buried and Back-drilled)

Example: For an 8 layer board with  $\mu$ Vias top & bottom and buried vias between layer 2 & 7, there should be 4 drill files. (L1-L2, L2-L7, L7-L8, and L1-L8).

- Routing Profile (outline) if not included in the section mentioned above.

NC Format details such as Unit, Format and Zero Suppression should be noted in a separate ASCII File or in the header of the NC Data file.

## NC Drill Format

Preferred Format	Alternative Formats Accepted
ODB++	Excellon I
Excellon II	Plotted Gerber Data Format

## 4.5. DRAWING(s)

The electronic data files should contain the appropriate drawings that fully describe the specifications and tolerances for the PCB.

### 4.5.1. FABRICATION DRAWING(s) SHOULD INCLUDE THE FOLLOWING DETAILS:

- Title and Revision Block with reference to PCB Project Name, Part Number and Revision
- Drill Chart with Finished Hole Size (FHS) and tolerance.
- Each Drill requirement should show as a unique Drill Chart. For Example each Blind Via Buried Via and Back-drill requirement should be separated from the through hole requirements and have a unique Drill Chart Table.
- Board outline with dimensions specifying critical features
- It is important to include X and Y dimensions on the Fabrication Drawing from a corner of the Profile to a hole in the Drill file. This will ensure that the profile aligns correctly to the datum location inside the board.
- Fabrication Notes detailing requirements and reference to corporate or industry standard specifications.
- Surface Finish requirements including deposit thickness
- Detailed drawings or special notes should outline features requiring additional attention in manufacturing or by quality control during fabrication.
- Detailed Board Stack-up with required overall board thickness, layer names, copper thickness and dielectric thickness referenced of critical requirement.
- Impedance Table detailing the Impedance Value & Tolerance, Impedance Layer, Reference Plane(s) Layer, Line Width and Spacing for Differential Pairs.

### 4.5.2. FINISHED ASSEMBLY PANEL ARRAY DRAWING(s)

- Title and Revision Block with reference to PCB Project Name, Part Number and Revision
- Drill Chart with Finished Hole Size (FHS) and tolerance.
- This will typically be unique to only features on the Panel Array not internal PCB Holes covered in the Fabrication Drawings.
- Array Dimensions with reference to internal hole or Zero of the board
- Board orientation for rotation or mirrored requirement
- Details of Break-a-way or Score requirements
- Detail of Fiducial requirements

## Drawing Format

Preferred Format	Alternative Formats Accepted
Adobe Acrobat PDF Format	Gerber 274X HPGL AutoCAD DFX or DWG Postscript or Encapsulated Postscript

## 4.5.3. SPECIFICATION DOCUMENT(S) - OPTIONAL

- The customer must list the general specifications on the Fabrication Drawing. In most cases, the customer drawings will reference the IPC specifications (i.e.: IPC-6011/6012 and IPC-A-600). However, in some cases the customer specifies their own general specification in addition to, or instead of IPC general specifications.
- If you use a general specification that is not an IPC document, then please submit this document to Multek several weeks in advance of placing your first order. This will allow time for the implementation and negotiation of items in the specification (depending on the complexity).
- If the customer does not provide reference to a specification on the drawing or readme files, Multek will default to IPC-6012 Class II standards.
  - Hierarchy of conflict requirement are as follow:
    - Purchase Order
    - Data Files
    - Customer Drawing
    - Customer Specification
    - Industry Specification

## 4.6. DATA COMPRESSION, ENCRYPTION, AND FILE TRANSFER

Before transferring any data electronically, the customer should use data compression to optimize the file transfer process. Grouping large numbers of files into a single compressed file will help optimize the transmission time and reduce file storage size requirements.

If the customer requires added security outside of the controlled server access, such as ZIP file password or PGP Encryption contact your local FAE or BDM before transmitting files to Multek. Multek will require additional support from the customer to manage added security within the transmitted file.

### Data Compression Formats

Preferred Method	Alternative Methods Accepted
ODB++ *.tgz compressed output ZIP, ARC, WINZIP, 7z	Unix tar or compress command RAR Compression

## 5. MATERIAL, PRODUCTION PANELS AND STACK-UPS

Multek offers a wide range of Materials to meet today's technology requirements. Materials are categorized into different technology ranges based on factors of Physical, Thermal and Electrical capabilities. Many designs today require a wide range of requirements to meet these specifications. Below are some key topics to consider when choosing from one of many materials offered by Multek. For additional details on Multek material offering please reference section [23](#) Material Cross Reference.

## 5.1. MATERIALS

### 5.1.1. LEAD-FREE ASSEMBLY REQUIREMENT

Lead-free (Pb-free) soldering processes require increased temperature profiles over standard eutectic processing, necessitating more thermal robust PCB materials. Initially Glass Transition Temperature (Tg) was used to determine the robust of a material. However, through the process of qualifying Pb-Free materials, it has been shown the Degradation Temperature (Td) is the more critical value. For robust Pb-Free materials, Multek recommends a Td value of 330°C or higher. This characteristic is only an indicator of lead-free performance and not a guarantee of Pb-free capability. We recommend you work through any material selection option with Multek's FAE and Engineering Support teams.

### 5.1.2. HALOGEN FREE REQUIREMENTS

Halogen Free or “Green” materials are popular in the consumer electronics market. These materials have complied with regulations to remove hazardous substance such as Bromides and other controlled substances from their make-up. These materials will come in a large range of offerings to meet many electrical and price targets.

### 5.1.3. MID AND LOW LOSS MATERIALS

Electrical performance of materials is one of the key attributes when selecting the right offering for a design. The characteristics of preferred electrical performance are traditionally based on the Dielectric Constant (Dk) and Loss Tangent (Df) properties of the specific material. As processing speeds continue to increase, the focus on dB loss performance has increased in importance. Multek offers an extensive selection Mid and Low loss materials offering with varying Df values. These materials tend to be more expensive and often have higher processing cost so a price for performance evaluation should be done to ensure the proper material is selected. Please contact your local FAE for assistance in selecting the best option.

Material Loss Reference

Material Grade	Loss Tangent
High Loss	> 0.0200
Standard Loss	0.0190 - 0.0120
Mid Loss	0.0110 - 0.009
Low Loss	0.0089 - 0.005
Ultra Low Loss	0.002 - 0.004

*It should be noted that Copper type will have a large impact of dB loss due to copper roughness. Many Mid to Ultra Low Loss material will come with lower profile copper foil at a premium to help improve the losses related to copper roughness.*

### 5.1.4. HYBRID MATERIAL STACK UP

Typical PWB design utilizes a homogeneous stack up or the same material resin systems for the core and prepreg layers. However, there are times when a hybrid stack up can be used to balance the need for performance and cost. In these applications a lower loss, higher performance material may be used for one or two layers where critical traces are being routed. These lower loss materials come at a premium

and since the electrical performance is limited to couple of layers, a lower cost material can be used for the balance of the design minimizing cost.

When designing a hybrid PWB, a common prepreg material must be used throughout the stack up. One drawback to this option is UL recognition. Even though individual material offerings have UL rating, combining resin systems requires addition UL testing and certification. Please contact your Field Application Engineer for the approved combination.

## 5.2. PANEL SIZES

Raw Material is manufactured in large sheet format. This large sheet is not conducive for PCB manufacturing, so smaller panels are cut from the master sheet. Various panel sizes are available from a master sheet, which can be utilized to optimize the finished PCBs on the production panel. The goal is to eliminate any waste being generated from the cut of the master sheet, but in turn utilize the available panels to maximize the utilization of the PCB within this panel. This is referred to as “Panel Utilization”. Panel utilization is one of the largest contributors to overall board cost. Poor panel utilization will generate larger amounts of material waste.

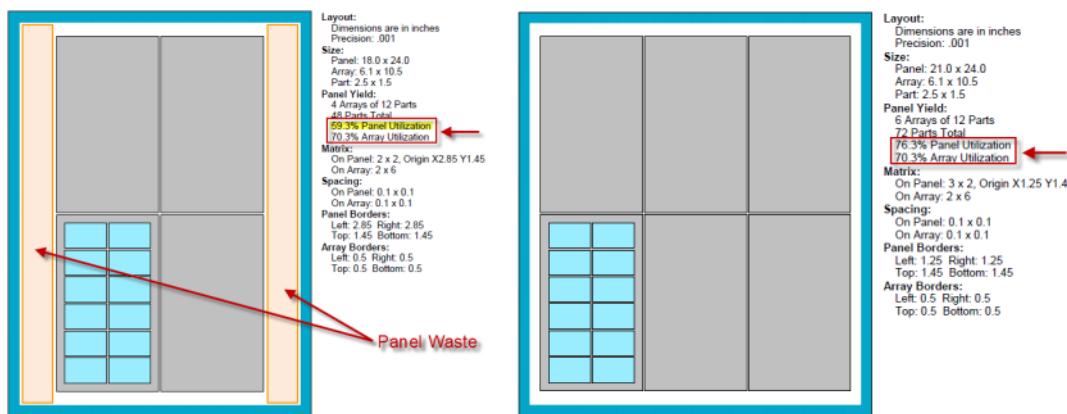


Figure 1

### Panel Sizes Available

Preferred			Available Alternatives		
14 x 24	16 x 18	16 x 21	12 x 18	14 x 16	16 x 20
18 x 24	21 x 24		21 x 27		

## 5.3. MINIMUM & MAXIMUM BOARD SIZE

Based on various panel sizes you can have a variety of PCB form factors that will provide optimized panel utilization. There are minimum PCB sizes allowed on production panels. To prevent damage or other handling issues during post PCB Fabrication equipment and during panel depopulation a minimum board size is required at Multek. If a smaller PCB size is required, Multek can offer a Shipped Array Panel with smaller parts contained into an Assembly Panel with routed or scored break-a-way tabs. (See Array Section for additional Details)

Preferred		Alternatives	
Minimum Board Size	Maximum Board Size	Minimum Board Size	Maximum Board Size
3.00 x 5.00	16.50 x 22.50	1.00 x 2.00	19.60 x 25.60

\* Mass Lamination tooling method can offer a larger panel size.

## 5.4. NON-USEABLE PANEL AREA

On a production panel, there will be a border area on the outer edge of the panel that is reserved for production tooling and nomenclature. This “non-useable” area cannot be used for any finished PCB. You can take advantage of this non-useable area when panelizing a smaller board for a shipped panel array. Any break-a-way or excess Assembly Panel Array can encroach into the non-useable area, as long as any tooling holes or nomenclature contained on this area is acceptable for that section. Often utilizing support from the FAE team, customer have been able to add notches or cut outs in strategic location to avoid interference of the production tooling and take advantage of encroaching into the non-useable area with the finished PCB.

When determining the optimum PCB form factor size Multek recommend working with the FAE team to determine the optimum panel size and board dimensions to achieve the highest level of Panel Utilization. This should take place early in the design phase to help prevent any extensive mechanical changes that may occur.

### Non-Useable Area of a Panel

Industry Preferred			Multek Alternatives		
Panel Size	Border Area	Useable Area	Panel Size	Border Area	Useable Area
18 x 24	0.75 x 0.75	16.50 x 22.50	18 x 24	0.67 x 0.67	16.66 x 22.66

## 5.5. ROUTER PATH BETWEEN PARTS

When calculating the finished shippable part configuration, it is critical to take into account the routing path required to cut the shipped panel or board from the master panel. When determining the spacing between parts required for the cutting Multek recommends using the largest routing channel as possible, as it increases the machine efficiencies using larger bits. Typical spacing between Array Panels would be 0.150 inches, which will allow a 0.125 router bit to cut clean edges on all parts. If gaining on panel utilization by reducing the separation of parts is available, then reduction to .093 or even .062 may be considered, but may affect price due to slower routing speed and increased machine time. For spacing between parts arrayed in a shipped panel, Multek recommended to use a minimum 0.100 spacing in all route-n-retain process.

## 5.6. STACK-UPS AND MULTILAYER PCB BUILD UPS

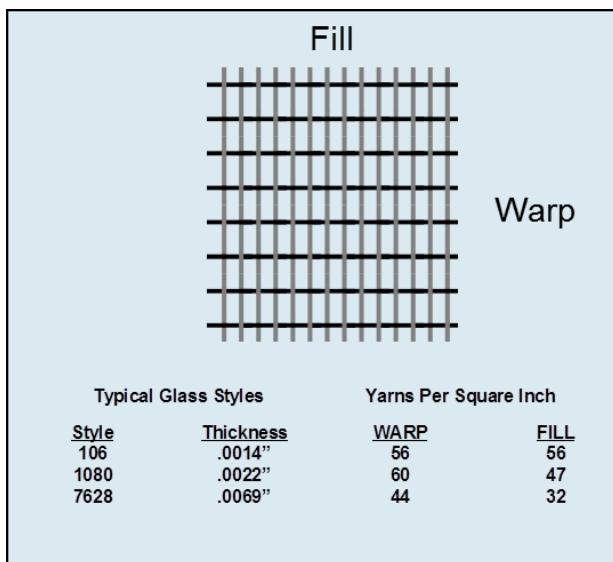
Manufacturing will build PCB in paired layers, a top and bottom etched copper image on a single sheet of cured laminate. You can combine these etched layers with an adhesive dielectric to create multiple paired layers or a multilayer PCB. The PCB manufacture will drill holes and plate them with copper to create the electrical connection. When discussing the term “Stack-up” it refers to the sequence of stacked layers and the dielectrics used between these layers at the basic level. The stack-up can also reference connected layer by unique drilling process and other pertinent information required for the build-up of a multilayer PCB.

### 5.6.1. DIELECTRICS

PCB materials come in a variety of capabilities. The primary focus of a good material is one that meets both the thermal and electrical requirements of the unique design. Over the years, advancements in material science have been significant and wide ranges of materials are now available to meet critical design and environmental requirements. Dielectric refers to the material placed between the copper layers of the PCB. When discussing dielectrics the main topic of interest is the thickness. Thickness is critical to the circuit design for both electrical and mechanical requirements.

Dielectric comes in two major forms C-Stage or fully cured “core” with copper applied to the top and bottom. B-Stage or commonly known as “prepreg” which is a partially cured form of the C-stage core, without copper, that is dried to a pre-cured stage for handling. This prepreg would be used as adhesive

layers to bind the cores together in the finished stack of PCB layers. Introducing heat and pressure to the prepreg will cause the resin to soften and flow, then fully cure at the right temperature. This binds all the layers together creating the finished stack-up. The prepreg is typically the same family of material as the core. This is the most common stack-up to create a homogeneous offering of material properties within a stack-up. Reinforcement of a fiberglass weave cloth or other material is added to the resin in the dielectrics to ensure dimensional stability in the X, Y and Z-axis. Different offering of glass weave come in various diameters. The types of glass filament and the number of layers of glass cloth create the various core thicknesses to meet mechanical and electrical requirements.



<b>A - Stage</b>	Stage at which resin is soluble and fusible
<b>B - Stage</b>	Resin impregnated into woven glass Resin is more viscous and insoluble but plastic and fusible Dry to touch
<b>C - Stage</b>	Risen in solid state "CURED" infusible and insoluble

## 5.6.2. COPPER

Copper foil comes in a variety of thickness. Below is the table that shows the copper weight call out in reference to the thickness of the copper across the core surface. Copper also comes in a variety of surface roughness and attention should be paid to the use of smoother copper with lower loss materials. Please contact your FAE for support on Low Loss Dielectrics and Copper Foil options.

Common Copper Thickness Available

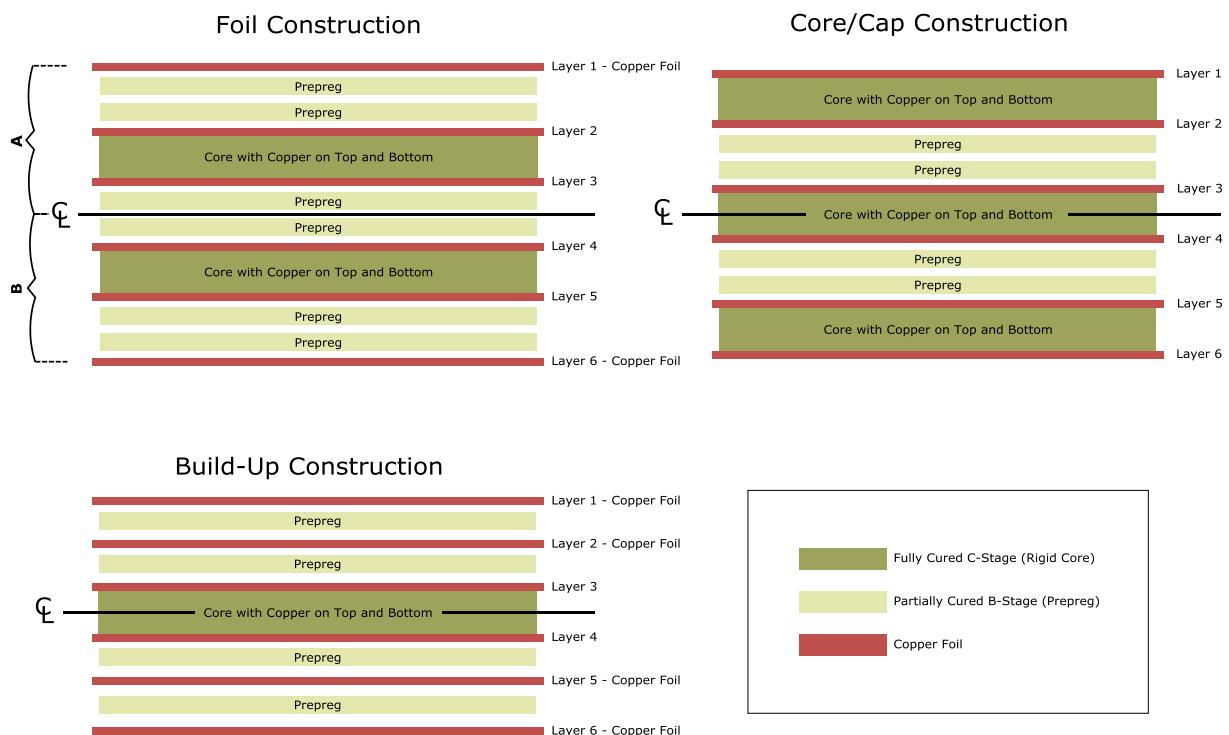
Copper Weight in Ounces	Thickness	
½ oz. or H oz.	0.0007"	17.78 um
1 oz.	0.0014"	35.56 um
2 oz.	0.0028"	71.12 um
3 oz.	0.0042"	106.68 um

\* Finished copper thickness will be slightly less than the above on finished circuit layers due to cleaning and prep for manufacturing.

## 5.6.3. STACK-UP RULES

Stack-ups are done in two methods, Foil and Capped (or Core) Constructions. Foil construction is the most common method for producing a multilayer PCB. Foil constructions will build up the internal layers first then add foil on the top and bottom for the outer layer process. Blind and Buried Via (BBV)

designs or in High Density Interconnect (HDI) will use a Build-up method for each laser or blind via drill layer. The Build-up method can be considered a stacked foil construction method.



When determining stack-up of the PCB the following items should be considered critical:

- Use Foil Construction whenever possible,
- Use Cap construction when recommended by manufacturing. Often this change can help improve the yield or reliability of the finished PCB for unique process requirements.
- Cap constructions are done with mixed material Hybrid constructions with RF requirements. This is done to maintain tight dielectric thickness control for RF requirements.
- Stack-ups should be symmetrical from the center of the middle paired layers out to the outer most layers.
- Copper should be balanced and evenly distributed when possible to prevent warpage (A=B in from the center out).
- Copper layers and the same core should be as close as possible to the same thickness weight. If you use 1 oz. copper on the top of a core use 1 oz. on the bottom. Often due to design requirements, you may need to reduce or increase copper thickness on one side of a core. Use of adjacent thickness on the table above, will minimize the impact to manufacturing process and yield.
  - For example, if you use H oz. on the top of a core, it is OK to use 1 oz. on the bottom. It is recommended not to use H oz. on one side and 2 oz. on the opposite side as the core will susceptible to poor etching quality and a potential increase warpage of the finished PCB.
- Use a single ply of prepreg whenever possible to help eliminate excessive cost for multiply constructions dielectric openings.
- Consider using higher resin preps when copper thickness warrants more resin to fill around the circuit image to prevent resin voiding.
- Use the same cores types and preps throughout the stack-up whenever possible. This will help to eliminate the number of materials types required to inventory and process during manufacturing.

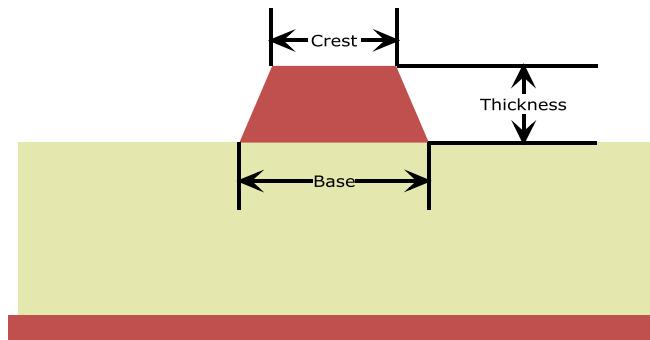
Consistency in core thickness and prepreg will improve registration and other production variables, which can lead to potential yield loss. Additionally, more varieties, within a single stack-up, will increase inventory cost long term.

## 6. ETCHED CIRCUIT DESIGN CAPABILITIES

Copper feature capabilities and etching capabilities can be a challenge to understand and may vary based on the copper thickness, imaging method, plating requirements and any additional process that impact the overall thickness of Copper on the etched surface. Multek utilizes both Laser Direct Imaging (LDI) and Photolithography (Silver Film) transfer for circuit image. During the circuit imaging process a photosensitive plating/etching resist is placed over the copper for image transfer. This photo resist is exposed with light to create the desired imaged features on each layer from the design Gerber files. This process can be done using the traditional silver film mask imaging process or through an LDI process which uses a laser to expose the etch resist. Both systems have benefit and limitations. For Many designers focus on trace width control, which is critical, but it is always good to keep in mind that PCB fabrication challenges with the removal of this excess copper during the circuit image and etching process. When compromises on design features are required, it is often recommend to increase the spacing between copper features, instead of increasing copper trace widths.

### 6.1. CONDUCTOR X-SECTION

Etching of internal circuit layers is driven by the thickness of the copper being etched or removed. Thicker copper will require wider spacing between copper features and wider conductor widths (traces). The etching process is an aqueous process and traces will never be perfectly square or rectangle. As the etching solution is introduced to the copper surface the etching will travel horizontal as it penetrates vertical into the copper. This is often referred to as under-cut, which provides a trapezoidal conductor shape. Based on the thickness of the copper the crest to base dimension of the conductor can be drastically different. Trace x-section measurements are referenced in Crest and Base width. All traces will have a level of trapezoidal shape. The copper thickness will determine the amount of reduction in trace crest width as the etching process is completed. Typical rule of 1 mil per ounce of copper is the standard difference between crest of trace to base width. When noting any trace width dimension it will always reference to the base width of the trace, unless the noted documentation states otherwise.



$$\text{Crest} = \text{Thickness} - \text{Base}$$

### 6.2. ETCH COMPENSATION

As the conductor, widths and spaces, get smaller, the fabricator must increase the size of the photoresist feature to ensure that the required conductor dimension are achieved during the etching process. The process is known

as “etch compensation”. Etch compensation allows the space between conductors to be etched more cleanly without over-etching the conductors. This reduces the risk for shorts on the finished PWB and still provides for the conductor widths specified in the design. This needs to be balanced with the reduction of the space in the photoresist, which makes it more difficult to get the etching chemistry between these spaces where copper is removed.

Etch compensation is not specified in the design and all original customer data should represent the finished desired circuit widths. Etch compensation is part of the fabrication tooling process that helps improve yields and will be unique to each manufacturers process and equipment. However, it is helpful in understanding the limits of capability in line conductor width and spacing based on the thickness of the base starting copper.

Depending on the base copper thickness, there are limitations on the width and spacing available in production to ensure a reliable etched circuit. The thicker the base copper the more difficult it will be to maintain good etch definition for finer conductor widths.

## 6.3. INTERNAL CIRCUIT LAYERS

Internal circuit layer processing is typically done by a print and etch method. This means the positive circuit image is transferred to the surface of the copper inner layer and the circuit image is protected with a etch barrier resist after developing. During the etching process excess copper is removed. When the protective etch resist is removed the finished copper circuit is completed for that individual layer.

### 6.3.1. TRACE AND SPACE GEOMETRY (INTERNAL LAYERS)

Preferred			Alternatives		
Starting Copper Foil Thickness	Inch	µm	Starting Copper Foil Thickness	Inch	µm
Min. Trace Width 0.5 oz. Cu:	0.003	76.2	Min. Trace Width 0.5 oz. Cu:	0.002	50.8
Min. Spacing 0.5 oz. Cu:	0.003	76.2	Min. Spacing 0.5 oz. Cu:	0.002	50.8
Min. Trace Width 1.0 oz. Cu:	0.004	101.6	Min. Trace Width 1.0 oz. Cu:	0.003	76.2
Min. Spacing 1.0 oz. Cu:	0.005	127.0	Min. Spacing 1.0 oz. Cu:	0.004	101.6
Min. Trace Width 2.0 oz. Cu:	0.006	152.4	Min. Trace Width 2.0 oz. Cu:	0.006	152.4
Min. Spacing 2.0 oz. Cu:	0.007	177.8	Min. Spacing 2.0 oz. Cu:	0.004	101.6

The above numbers are basic numbers for production within Multek. Capabilities are different for each Multek facility and it is recommended to reference section [24 Facilities Capabilities Survey](#) at the end of this document to understand the target facilities detailed capabilities. We also recommend contacting your local sales or technical support for any questions you may have regarding production capabilities.

## 6.4. EXTERNAL CIRCUIT LAYERS

External etched features are processed different from internal layers due to requirement of plating the holes drilled in the panel to create the interconnect. Base foil is used as a starting point and then plating is added to the surface of the panel to create the finished circuit image. The base foil is then etched away to leave the finished circuit pattern. This process will often result in a thicker trace than internal layers. Most stack-ups will detail the starting and plated thickness, which combined create the final overall copper trace thickness. If only one dimension is detailed, this will typically be the finished copper thickness, but it is prudent to check with the manufacturer supplying the stack-up for clarification.

Other attributes such as Via In Pad Plated Over (VIPPO) or the combination of Copper Filled Micro Via (Cu- $\mu$ Via) will require additional plating cycles and increase the base copper thickness for etching. This in turn will affect

the minimum trace and space geometries. Additional details on these processes are covered in section later in the document.

#### 6.4.1. TRACE AND SPACE GEOMETRY (EXTERNAL LAYERS)

Preferred			Alternatives		
Base Foil Thickness (Before Plating)	Inch	µm	Base Foil Thickness (Before Plating)	Inch	µm
Min. Trace Width 0.5 oz. Cu:	0.003	76.2	Min. Trace Width 0.5 oz. Cu:	0.002	50.8
Min. Spacing 0.5 oz. Cu:	0.004	101.6	Min. Spacing 0.5 oz. Cu:	0.003	76.2
Min. Trace Width 1.0 oz. Cu:	0.004	101.6	Min. Trace Width 1.0 oz. Cu:	0.003	76.2
Min. Spacing 1.0 oz. Cu:	0.004	101.6	Min. Spacing 1.0 oz. Cu:	0.004	101.6
Min. Trace Width 2.0 oz. Cu:	0.005	127.0	Min. Trace Width 2.0 oz. Cu:	0.004	101.6
Min. Spacing 2.0 oz. Cu:	0.0055	139.7	Min. Spacing 2.0 oz. Cu:	0.005	127.0

The above numbers are basic numbers for production within Multek. Capabilities are different for each Multek facility and it is recommended to reference section [24 Facilities Capabilities Survey](#) at the end of this document to understand the target facilities detailed capabilities. We also recommend contacting your local sales or technical support for any questions you may have regarding production capabilities.

## 7. MECHANICAL DRILLING

Mechanical Drilling is the process of drilling holes into the panel with a metal drill bit, typically carbide. Drill and router machines come with multiple head that contain variable speed spindle that spins at 80-300+ RPM, depending on the holes size. Drilling accuracy uses three precision axes. Sophisticated scales are referenced to maintain a tight tolerance while the drill table and heads move to the required hole location. The X-axis, which would be the spindle head moving left to right, is moved simultaneous to the Y-axis, which is the drill table moving forward and backward. This denotes the location of the hole drilled into the panel on a table grid. Simple ASCII code X042573Y0375 (Which has an implied decimal 2.4 with trailing zero omitted to save on memory) guides the machine movement. The spindle spins at a target RPM and then a feed rate is used specific to the drill diameter to insert the drill into the panel for drilling the hole. The feed rate not only tells the drill how fast to move the spindle down into the panel, but many machines have control over the depth of the drill, known as a Z-axis control. An inaccurate Spindle Speed Rate and Feed Rate, can affect the quality of the hole, as well as a dull drill bit tip or cutting edge. Every material and drill size will be optimized to maximize the hole quality and prolong the drill bit life for cutting quality holes. Cost associated with drilling can be one of the larger factor to consider, as the machine time is long for higher hole count panels and the drill bits become expensive.

Typically, you can get 250-2500 drill hits per bit, depending on size and material. More brittle material like a Ceramic filled material will cause the drill bits to dull faster.

### 7.1. THROUGH HOLES

All through holes (thru holes) are drilled with mechanical drills. This process ensures consistent diameter and accuracy. The holes will drill all the way through the panel and come out the backside. Entry and Back-up materials are used to ensure hole quality.

Control Depth Blind Vias are done during the same process as the thru holes by controlling the Z-axes depth of the drilling machine for these specific hole locations.

## 7.2. DRILLED HOLES VS. FINISHED HOLE (TYPICAL OVER DRILL)

It is important to note that when specifying a hole diameter on the fabrication drawing that you state whether it is the finished hole size (FHS) or the drilled hole size (DHS). It is common in the industry to specify the FHS in the hole chart contained on the Fabrication Drawing provided with the data. One of the few instances when a DHS is specified it is in reference to a press-fit connector holes. Special requirements for DHS and FHS are part of the Press Fit Connector for both insertion and retention reliability and SI performance. These details are noted on the Fabrication Drawing. The FHS is listed in the Hole Chart and the DHS is indicated by a flag referencing the note for the hole size required to meet the connectors requirements.

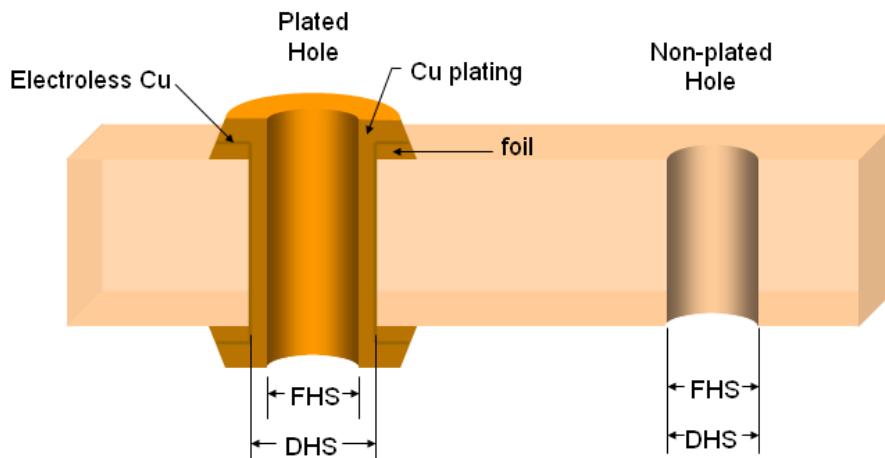
Symbol	Finished Hole Size	Type	Quantity	Tolerance
+	0.012	Plated	5302	+0.003 / -0 .012
◊	0.026	Plated	2132	+/- 0.002
*	0.050"	Plated	22	+/- 0.003
○	0.062	Plated	56	+/- 0.003
⊗	0.075"	Non-Plated	4	+/-0 .003
◊	0.100	Plated	1	+/- 0.003
☒	0.125"	Non-Plated	14	+ 0.003 / -0.001
☒	0.080 x 0.180	Plated	4	+/- 0.005

It is equally important to indicate if the holes are plated or unplated (non-plated) in the Gerber files and in the hole chart on the fabrication drawing.

For plated holes, the FHS is smaller than the DHS. Depending on the plating thickness required in the hole and the surface finish used, a DHS will be 0.002 – 0.005 inches over FHS. This allows adequate copper to be plated in the hole and closed down to the desired FHS. Later we will discuss annular ring related issues and understanding the concept of DHS and FHS will help greatly in knowing what pad size is required for a specific FHS.

For unplated holes, the DHS is very close to the FHS specified. There may still be a difference between the DHS and FHS for unplated holes due to the FHS specified on the fabrication drawing and the available drill bit diameters.

Please specify the FHS in the hole chart with a tolerance of +/- .003 for component holes and +/- .002 for Press Fit connectors. Via holes do not require a tight tolerance as they are used for connection to the internal layers only and no component lead will solder into these holes. Via holes should have a tolerance of +0.003 / - FHS. Unplated holes should be +/- 0.003 for standard capability, understanding that the larger the hole diameter the more relaxed the tolerance should be as drill bit selection may have larger gap between sizes. Some hole sizes over 250 mils may be routed during a separate machining process and +/- 0.005 should be considered standard.



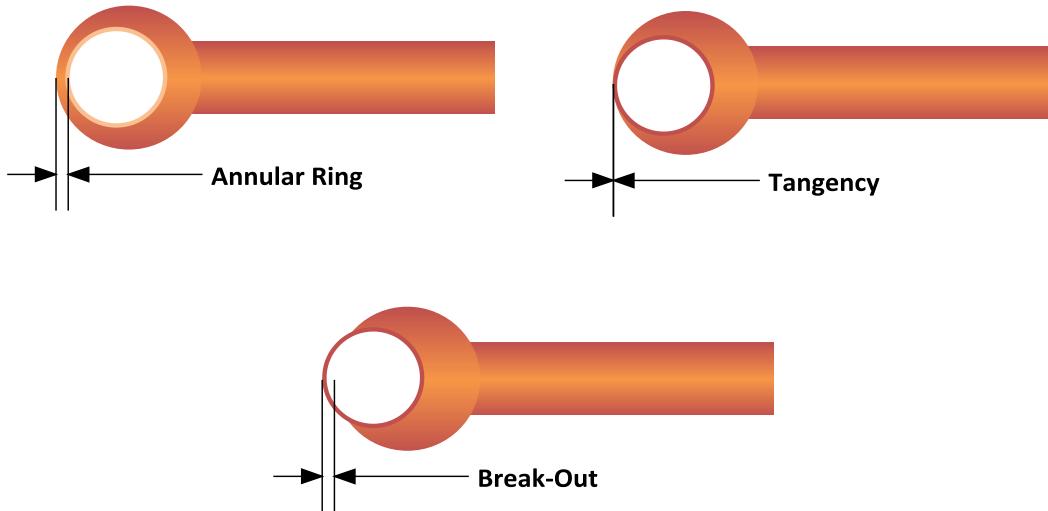
### 7.3. PAD SIZES IN RELATIONSHIP TO DHS/FHS

It is important to remember that getting a good hole wall plating requirement and ensuring you have good connection will rely on the hole to copper pad ratio also known as pad annular ring (AR). Annular ring is the amount of copper the surrounds the diameter of the hole barrel. Although the target location is to drill the hole into the middle of the pad, due to machine tolerance and material movement the pad will reference a targeting area for the drill to hit. If a hole requirement has a specific minimum AR requirement, then this should be calculated in the math used for determining the pad size.

$$\text{PadSize} = (\text{DHS} + 0.010) + 2(\text{AR})$$

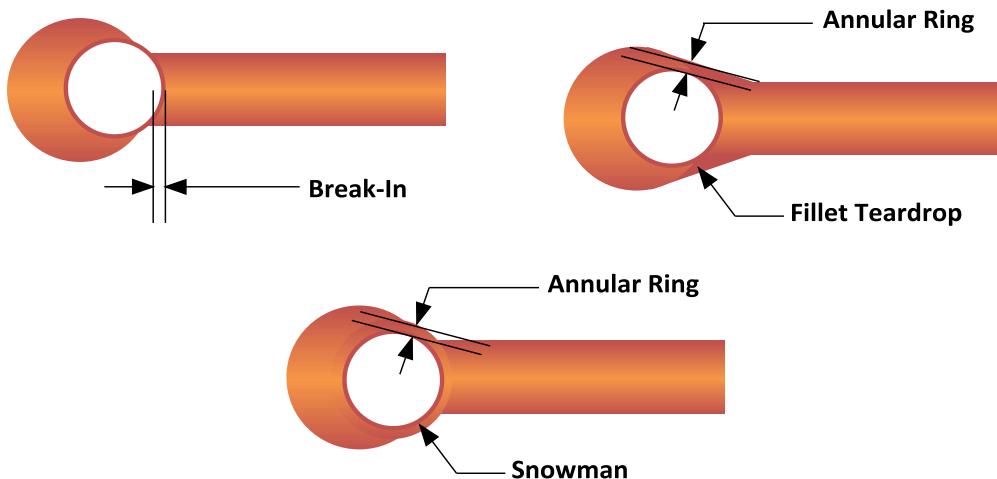
In some cases if the drill annular ring requires Tangency only, which means no breakout of the pad but also no annular ring, then 0.009 inches can replace 0.010 in the formula above. Please check the Capability Survey section for details on AR requirements for the facility or choice or contact Engineering for support.

When the customer specification and Fabrication Drawing do not provide annular ring requirements, Multek will default to the standard published by IPC in IPC-6012 Class II.



## 7.4. TEAR DROPPING

Manufacturers today like to add copper to the trace to pad junction point, which ensure adequate annular ring, and prevent a drill Break-in location from weakening the connection between the trace to the plated hole. There are two main processes commonly used to provide added copper support. The main teardrop method adds a fillet shaped extension on the pad, which tapers as it progresses down the trace. The Snowman connection adds a pad that is slightly larger than the drilled hole creating a “Snowman” shaped support junction. The teardrop is the most common practice and preferred at Multek.

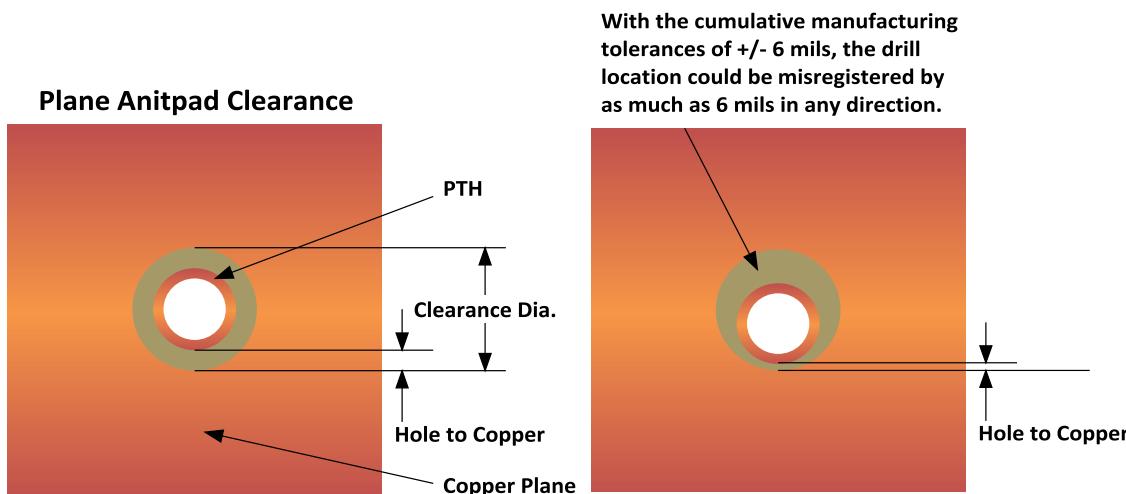


## 7.5. ANTIPAD SIZE IN RELATIONSHIP TO DHS/FHS

Another feature design requirement to understand is the relationship of the DHS to the Voltage and Ground Planes. On plane layers, it is common to pull the copper away from the PTH to ensure no connection at these locations. When copper is pulled back from a plated hole it is referred to as an Antipad or Plane Clearance pad. On plane layers, a minimum clearance is required to ensure no shorting occurs and account for annular ring minimums for voltage isolation safety and internal registration budgets. Multek will typically require a minimum 0.010 mils of copper pull back from the DHS with standard technology and 0.0085 for more advanced designs.

$$\text{antipad size} = \text{DHS} + 0.020$$

It is important to ensure that plane clearance does not create isolations to holes requiring connection to the plane due to the overlapping or reduced copper web between plane clearances. Special attention should be made to ensure that enough copper web is provided to ensure a robust connection.



## 7.6. ASPECT RATIO

The aspect ratio is the board thickness divided by the smallest DHS. The formula for calculating aspect ratio of the PCB is as follows:

$$\text{Aspect Ratio} = \frac{\text{BoardThickness}}{\text{SmallestDHS}}$$

It is extremely important that the customer understand the aspect ratio to ensure proper copper formation in the plated holes is capable. If the PCB is 0.100" thick then the smallest standard drill size available is that could be used would be .010 inches. Depending on the facility, as detailed in the Capability Survey at the end of the document, and with added capabilities in pulse plating, Multek is capable of 15:1 aspect ratios at certain facilities.

## 7.7. SAMPLE DRILL TABLE WITH TOLERANCES

Standard Drill Tables on Fabrication Drawings will detail the following items. Symbols are used to reference the location of these drilled holes within the board outline on the drawings.

Symbol	Finished Hole Size	Type	Quantity	Tolerance
+	0.012	Plated	5302	+0.003 / -0 .012
◊	0.026	Plated	2132	+/- 0.002
*	0.050"	Plated	22	+/- 0.003
○	0.062	Plated	56	+/- 0.003
◎	0.075"	Non-Plated	4	+/- 0.003
◊	0.100	Plated	1	+/- 0.003
☒	0.125"	Non-Plated	14	+ 0.003 / -0.001
☒	0.080 x 0.180	Plated	4	+/- 0.005

Drill tolerances should be as robust as possible. Driving tighter tolerances can result in yield loss cost. Multek recommends the following tolerances for various types of holes or drilled slots.

Types	Recommended Tolerance
Via Holes	+0.003 / -FHS *
Component Holes	+/- 0.003
Press Fit Holes	+/- 0.002
Large Component holes > 0.062	+/- 0.005
NPT Holes Standard	+/- 0.005
NPT Holes Special	+/- 0.002

\* Via holes are only used for connecting to the internal layers and it is recommended to open the tolerance to allow for manufacturing to optimize the DHS selected to achieve proper annular ring and minimize aspect ratio issues for plating.

## 7.8. NON-PLATED THROUGH HOLES

Non-Plated through Holes (NPTH) have the best registration when drilled during the primary drilling process with the plated thru holes. This can only be done if the copper is removed from the hole by up to 0.010 mils. This process will allow the plating resist to cover over the hole causing a tent to protect the hole from plating. The larger the hole the more difficult it is for the resist to cover the hole. Any hole over 0.187-0.250 will most likely have issues holding the tent of resist and will need to be drilled during a secondary drill process or at final routing when the individual part or is cut from the production panel. If copper is required to be adjacent to the Non Plated hole, then a secondary drilling process will need to be done for these holes after copper plating and etching is completed. It is not recommended to do any alignment or tight true position tolerance NPT holes

## 7.9. DRILL TABLE

There is a variety of drill sizes available. Most manufacturers in Asia and Europe will carry Metric drill sizes and North America will inventory standard tool sizes. .

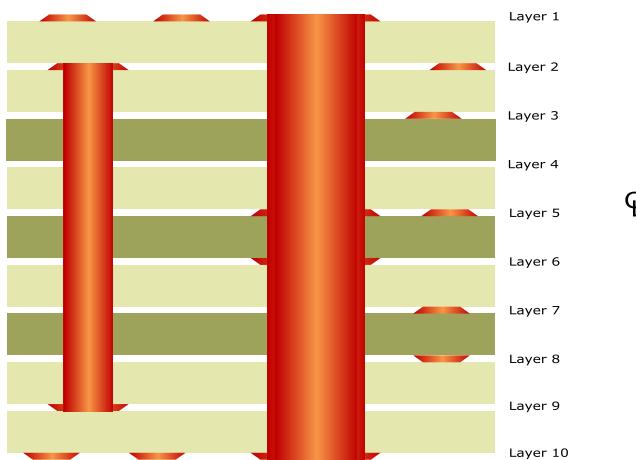
Drill Size	Decimal (in)								
0.05 mm	0.0020	0.85 mm	0.0335	44	0.0860	27	0.1440	5.10 mm	0.2008
0.10 mm	0.0040	65	0.0350	2.20 mm	0.0866	3.70 mm	0.1457	7	0.2010
0.13 mm	0.0050	0.90 mm	0.0354	2.25 mm	0.0886	26	0.1470	5.15 mm	0.2028
0.15 mm	0.0059	64	0.0360	43	0.0890	3.75 mm	0.1476	13/64"	0.2031
97	0.0059	63	0.0370	2.30 mm	0.0906	25	0.1495	6	0.2040
96	0.0063	0.95 mm	0.0374	2.35 mm	0.0925	3.80 mm	0.1496	5.20 mm	0.2047
95	0.0067	62	0.0380	42	0.0935	3.85 mm	0.1516	5	0.2055
94	0.0071	61	0.0390	3/32"	0.0938	24	0.1520	5.25 mm	0.2067
93	0.0075	1.00 mm	0.0394	2.40 mm	0.0945	3.90 mm	0.1535	5.30 mm	0.2087
92	0.0079	60	0.0400	41	0.0960	23	0.1540	4	0.2090
0.20 mm	0.0079	59	0.0410	2.45 mm	0.0965	3.95 mm	0.1555	5.35 mm	0.2106
91	0.0083	1.05 mm	0.0413	40	0.0980	5/32"	0.1562	5.40 mm	0.2126
90	0.0087	58	0.0420	2.50 mm	0.0984	22	0.1570	3	0.2130
89	0.0091	57	0.0430	39	0.0995	4.00 mm	0.1575	5.45 mm	0.2146
88	0.0095	1.10 mm	0.0433	2.55 mm	0.1004	21	0.1590	5.50 mm	0.2165
0.25 mm	0.0098	1.15 mm	0.0453	38	0.1015	4.05 mm	0.1594	5.55 mm	0.2185
87	0.0100	56	0.0465	2.60 mm	0.1024	20	0.1610	7/32"	0.2188
86	0.0105	3/64"	0.0469	37	0.0140	4.10 mm	0.1614	5.60 mm	0.2205
85	0.0110	1.20 mm	0.0472	2.65 mm	0.1043	4.15 mm	0.1634	2	0.2212
84	0.0115	1.25 mm	0.0492	2.70 mm	0.1063	4.20 mm	0.1654	5.65 mm	0.2224
0.30 mm	0.0118	1.30 mm	0.0512	36	0.1065	19	0.1660	5.70 mm	0.2244
83	0.0120	55	0.0520	2.75 mm	0.1083	4.25 mm	0.1673	5.75 mm	0.2264
82	0.0125	1.35 mm	0.0531	7/64"	0.1094	4.30 mm	0.1693	1	0.2280
81	0.0130	54	0.0550	35	0.1100	18	0.1695	5.80 mm	0.2283
80	0.0135	1.40 mm	0.0551	2.80 mm	0.1102	4.35 mm	0.1713	5.85 mm	0.2302

0.35 mm	0.0138	1.45 mm	0.0571	34	0.1110	11/64"	0.1719	5.90 mm	0.2323
79	0.0145	1.50 mm	0.0591	2.85 mm	0.1122	17	0.1730	A	0.2340
1/64"	0.0156	53	0.0595	33	0.1130	4.40 mm	0.1732	5.95 mm	0.2343
0.40 mm	0.0157	1.55 mm	0.0610	2.90 mm	0.1142	4.45 mm	0.1752	15/64"	0.2344
78	0.0160	1/16"	0.0625	32	0.1160	16	0.1770	6.00 mm	0.2362
0.45 mm	0.0177	1.60 mm	0.0630	2.95 mm	0.1161	4.50 mm	0.1772	B	0.2380
77	0.0180	52	0.0635	3.00 mm	0.1181	4.55 mm	0.1791	6.05 mm	0.2382
0.50 mm	0.0197	1.65 mm	0.0650	31	0.1200	15	0.1800	6.10 mm	0.2402
76	0.0200	1.70 mm	0.0669	3.05 mm	0.1201	4.60 mm	0.1811	C	0.2420
75	0.0210	51	0.0670	3.10 mm	0.1220	14	0.1820	6.15 mm	0.2421
0.55 mm	0.0217	1.75 mm	0.0689	3.15 mm	0.1240	4.65 mm	0.1831	6.20 mm	0.2441
74	0.0225	50	0.0700	1/8"	0.1250	13	0.1850	D	0.2460
0.60 mm	0.0236	1.80 mm	0.0709	3.20 mm	0.1260	4.70 mm	0.1850	6.25 mm	0.2461
73	0.0240	1.85 mm	0.0728	3.25 mm	0.1280	4.75 mm	0.1870	6.30 mm	0.2480
72	0.0250	49	0.0730	30	0.1285	3/16"	0.1875	6.35 mm	0.2500
0.65 mm	0.0256	1.90 mm	0.0748	3.30 mm	0.1299	4.80 mm	0.1890	E	0.2500
71	0.0260	48	0.0760	3.35 mm	0.1319	12	0.1890	1/4"	0.2500
0.70 mm	0.0276	1.95 mm	0.0768	3.40 mm	0.1339	4.85 mm	0.1909	6.40 mm	0.2520
70	0.0280	5/64"	0.0781	3.45 mm	0.1358	11	0.1910	6.50 mm	0.2559
69	0.0292	47	0.0785	29	0.1360	4.90 mm	0.1929	F	0.259
0.75 mm	0.0295	2.00 mm	0.0787	3.50 mm	0.1378	10	0.1935		
68	0.0310	2.05 mm	0.0807	3.55 mm	0.1398	4.95 mm	0.1949		
1/32"	0.0312	46	0.0810	28	0.1405	9	0.1960		
0.80 mm	0.0315	45	0.0820	9/64"	0.1406	5.00 mm	0.1968		
67	0.0320	2.10 mm	0.0827	3.60 mm	0.1417	5.05 mm	0.1988		
66	0.0330	2.15 mm	0.0846	3.65 mm	0.1437	8	0.1990		

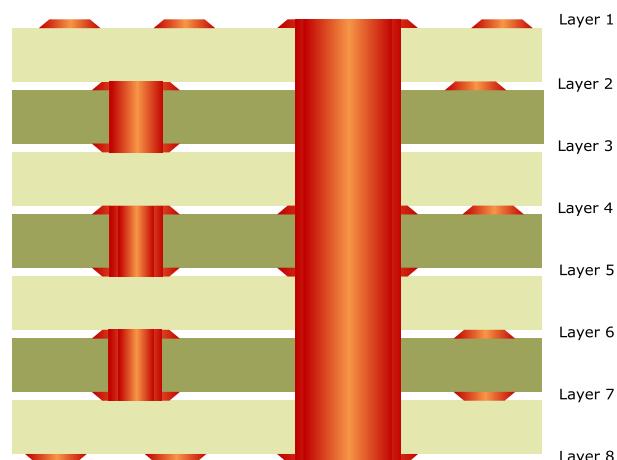
## 7.10. BURIED VIA

Buried via are thru holes that are drilling only through inner layers. These vias are not visible to the surface of the board. Buried vias help address routing density issues on the surface and are combined with blind vias in sequential build-up methods of fabrication. Buried vias can be drilling into just one internal core that connects the top and bottom layer or into a multi-layer subpart. Buried vias connect multiple layers together internally. Buried vias will follow standard thru hole requirements for annular ring, aspect ratio and drill to copper requirements.

Buried Multilayer Sub

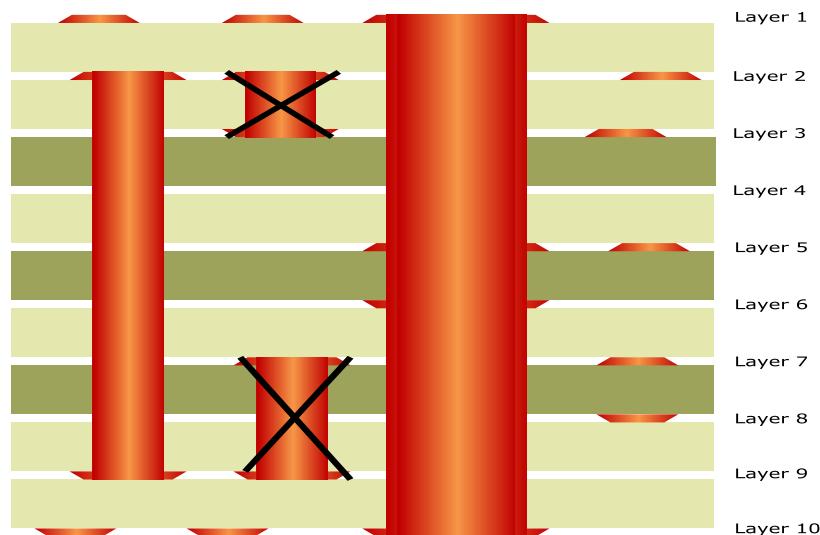


Buried Cores



## 7.10.1. NO OVERLAPPING DRILLED HOLES

It is important to note that when designing with buried vias you should avoid overlapping via structures. Buried drill layers that start on the same layer but finish on a different layer cause challenges to production and increase cost significantly. When multiple drilling processes are used, this will increase the base copper thickness for each plating cycle and require more robust design structures on these layers.

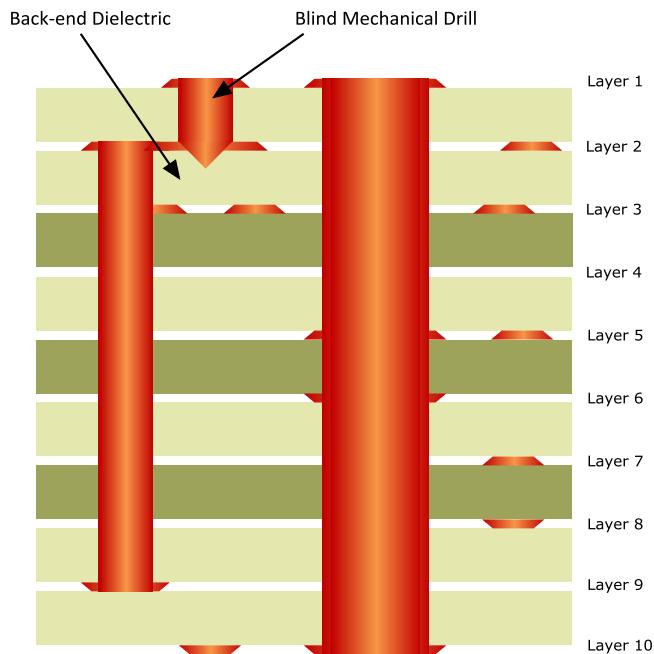


## 7.10.2. VIPPO BURIED VIAS

When the dielectric thickness of a buried sublam is greater than 0.050 inches, it is required to fill the vias with epoxy before the next build-up lamination process. This will prevent an excessive amount of resin being leached into the hole barrel and causing lamination voids or resin starvation at the bonding locations. This can result in delamination or other reliability issues seen after fabrication.

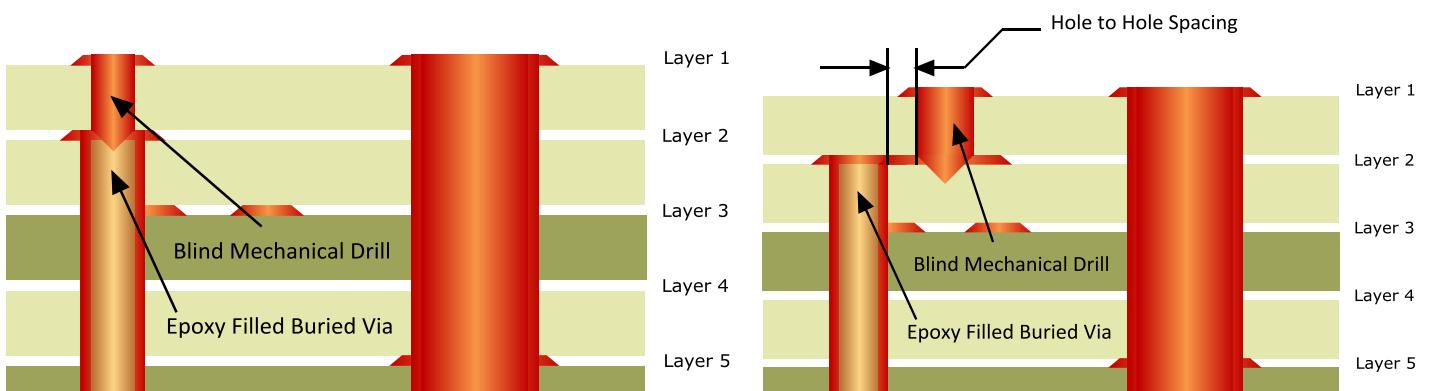
## 7.11. BLIND MECHANICAL VIA

Blind Via drill from the top or bottom surface into the board, but do not pass all the way through. Typically, blind vias are done in buildup technology and used to connect adjacent layers. With mechanically drilled blind vias, larger hole sizes are available and deeper depths are available with larger hole sizes. There are pitfalls to mechanically drilled blind vias that are addressed below. When you only have a few holes per board that are blind drilled, mechanical is an option to help eliminate the setup cost for utilizing a laser for drilling. Blind mechanical vias will follow the same design guidelines that a mechanical through hole does with relationship to annular ring and spacing. The only difference with Blind via is that an aspect ratio for copper plating, should be maintained to 0.75:1 to ensure quality plating of the hole barrel. The reduction in aspect ratio has to do with the limited plating solution that migrates into the hole. Since the solution does not have a free flow through the hole barrel, the molecular exchange of copper replenishment is limited and impacts the throwing power for the copper build-up.



### 7.11.1. CAPPED, AND STACKED OR NOT TO STACK

Blind vias drills should not be drilled into buried via holes. It is best to offset the drill locations to prevent overlapping holes or hole-to-hole spacing violations. A minimum of 8 mil spacing from hole wall to hole wall is recommended for mechanical drilling. If drilling into the pad stack is required, we recommend you contact a local FAE for clarification on capability and yield impact, which can effect pricing greatly.



### 7.11.2. BACK END DIELECTRIC REQUIREMENT

Because most standard mechanical drills are chisel tipped, you will have an angle to the point that needs to be accounted for. Typical angles are about 25% of the diameter. With relationship to the drill tip angle penetration of a minimum of 10-15% into the landing target layer will ensure reliable connection. This could cause issues with drill tip pass through on the back-end dielectric. If the back-end dielectric is too thin there is a higher probability for shorting. It is recommended to have a 5 mil back end dielectric thickness minimum. The 5 mils will account for minimum drill pass through and machine tolerance. If

the design requires a larger depth than 5 mils it is recommended to increase the back-end dielectric to 10% of the drill depth to ensure no adjacent layer shorting.

### 7.11.3. RELIEVE COPPER ON BACK SIDE OPTION

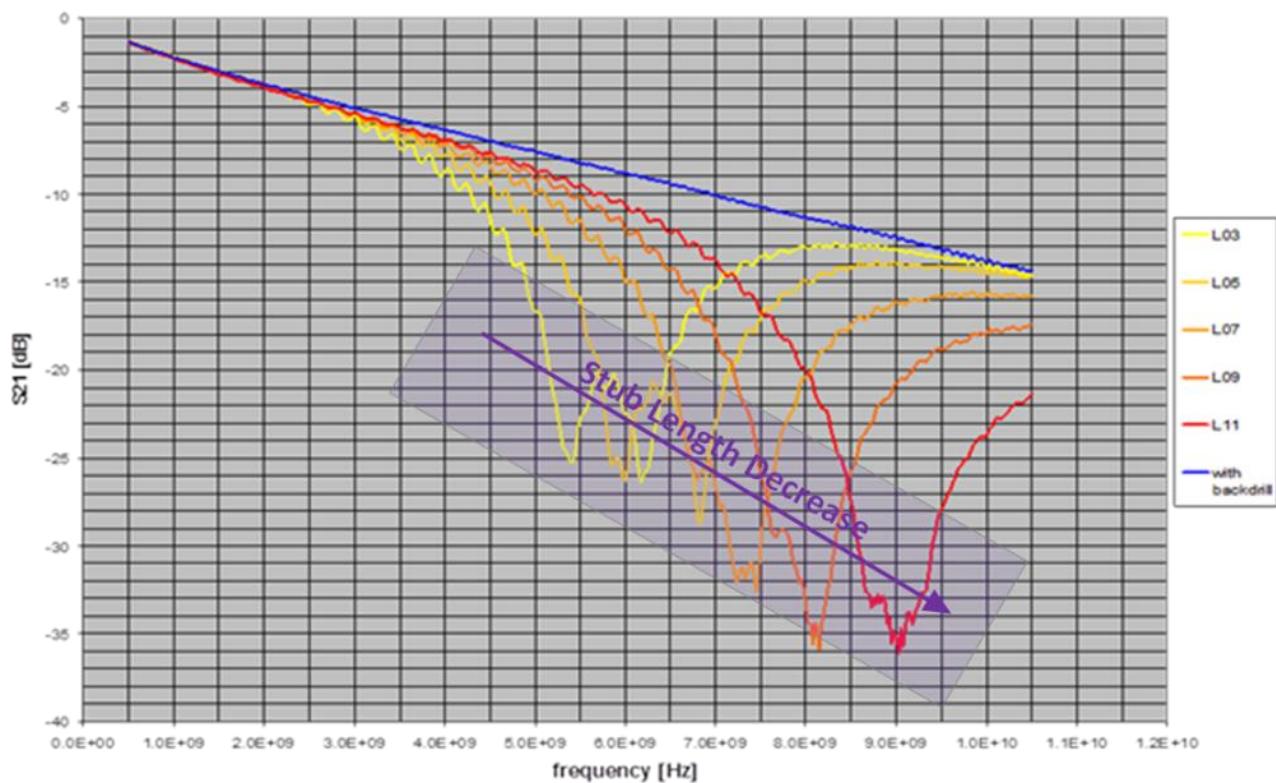
If the Back-end dielectric is less than 0.005 inches it is recommend to relieve the copper on the adjacent layer to prevent shorting at these drill locations. This can be done by adding a clearance on at the blind via locations as a safety step to prevent shorting. The clearance can have a reduced plane clearance at these locations, but if permitted it is recommend maintaining the same antipad diameter as with a thru holes of equal diameter.

### 7.11.4. PLATING ASPECT RATIO LIMITATIONS

The typical aspect ratio for blind via structures is 0.75:1 unless specified differently in the Capability Survey contained below. The reduction in aspect ratio has to do with the throwing power for the copper build-up inside blind holes. Due to this limitation a deeper drilled blind via will have higher potential of voiding at the base of the hole barrel.

## 7.12. BACK-DRILLING

Back-drilling is a method of removing the excess copper stub from a via or plated thru hole. Back-drilling has become more common due to the increase signal speed and the effect the via stub has on signal distortion, as discussed above.



The back-drilling process is done by drilling into a plated thru hole with a drill bit large enough to remove the copper. The back-drill bit should be small enough that it does not cause unplanned exposing copper on layers the back-drill passes through. Typically, back-drilling is done on high-speed signal and can be done from both the top and bottom side of the PCB at multiple depths. Caution should be taken to allow enough tolerance and spacing between connection layers and cut layers to prevent undesired opens by drilling too deep.

### 7.12.1. BACK-DRILL GUIDELINES

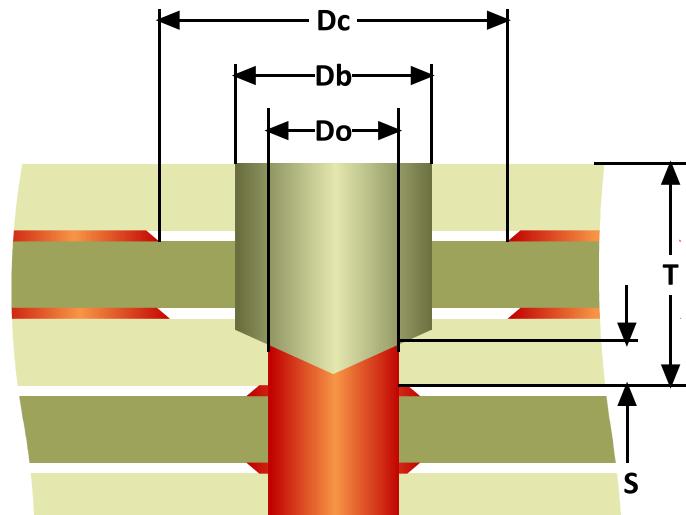
- T - Thickness from top to target layer
- S - Stub length
- Da - Diameter of antipad
- Db - Diameter of back-drilling
- Dc - Conductor to hole barrel spacing
- $Dc = (Da-Do)/2$
- Do - Diameter of original DHS

#### Back-drill Guidelines

**Do  $\geq$  10 mil**

**Db  $\geq$  Do + 6-8 mil**

**Dc  $\geq$  Db +12 mil**



### 7.12.2. DOCUMENTING BACK-DRILL REQUIREMENTS

Use unique drill files and drill charts to identify back-drilling requirements. Designate the layer to be cut (MC) and the layer that should not be cut (MNC). Layers between the MC and MNC layers are acceptable to be connected or open based on the depth tolerance capability.

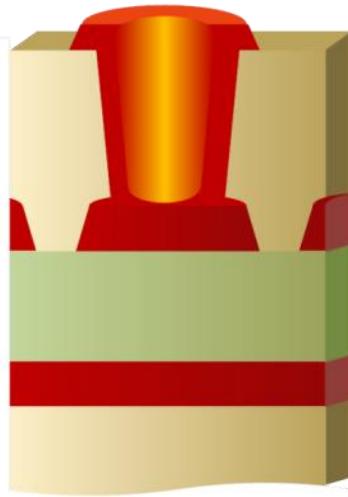
Back-drill from Bottom Side					
Symbol	Finished Hole Size	Type	Quantity	Tolerance	MC Layer / MNC Layer
+	0.018	Non-Plated	608	+/- 0.003	PWR7 / Signal3
◊	0.022	Non-Plated	1202	+/- 0.003	PWR7 / Signal3

Back-drill from Bottom Side					
Symbol	Finished Hole Size	Type	Quantity	Tolerance	MC Layer / MNC Layer
+	0.018	Non-Plated	43	+/- 0.003	GND16 / Signal12

## 8. LASER DRILLING

Laser drilling is a key attribute in today's commercial High Density Interconnect (HDI) designs. This process drills many small holes into a panel at a rapid rate. Laser drilling can be done in two methods with unique laser waveforms that provide different cutting or ablating process. We will not get into the mechanics of the drilling process, but only the design requirements, but it important to know that the two methods provide relatively the same finished effect. The most common laser via formation is done with a CO<sub>2</sub> Laser, which cuts quickly and cleanly through a variety of materials.

Laser drilling is a burning method of via formation, most Micro Via ( $\mu$ Via) holes are formed in a conical shape with the base of the via hole tapering down slightly. The deeper the drill penetrates into the dielectric the larger the diameter of the hole at the entry point will become.



## 8.1. $\mu$ VIA DRILL SIZES

$\mu$ Via drill sizes are dictated by the formation when cutting the dielectric and via pad diameter. Although, there are limitations in the minimal diameter for reliable plating, it is not uncommon to see a  $\mu$ Via drill size at 0.003-0.004 inches. Also it should be noted that the hole size can be larger, but a common limit in  $\mu$ Via drill diameter is about 0.012 inches. The maximum drill diameter is controlled by limiting factors in plating aspect ratio and excess dimpling in copper filled  $\mu$ Vias.

## 8.2. $\mu$ VIA PAD SIZES

When determining the pad size of the  $\mu$ Via use the following formula to best determine what size pad is required

$$\mu\text{Via Pad} = \mu\text{Via DHS} + 0.006$$

When processing  $\mu$ Via design constraints consider that the finished hole size will be filed with copper on most cases and that the DHS will be best determined by the pad size required for the packaging the small the pad size the smaller the DHS required.

Types of via formation such as Every Layer Interconnect and Stacked  $\mu$ Vias will be discussed in more detail in later sections.

## 8.3. $\mu$ VIA ASPECT RATIO

When plating  $\mu$ Via holes, follow the blind via guidelines for aspect ratio. The typical aspect ratio for blind via structures is 0.75:1 unless specified differently in the Capability Survey contained below.

## 9. VIA IN PAD PLATED OVER HOLE

Via in pad plated over holes (VIPPO) is the process of drilling the via hole into the SMT pad and plating this via over with copper to create a flat coplanar surface for soldering the lead to this pad. The filling process can be in both thru holes and blind via holes. VIPPO allows for increased routing channels on the surface of the board. When doing epoxy filling on thru holes it will also increase the base copper thickness and cause a little more robust design structures to be used

on the surface layers. When VIPPO is required for both PTH and  $\mu$ Via, epoxy filling these holes is a desired option to ensure minimal surface plating. It is not recommended to do both epoxy filling of through holes and solid copper filling of blind  $\mu$ Via holes as this will require additional plating an imaging process and increase the cost, along with limit the design geometries on the plated surface due to the additional copper thickness.

## 9.1. EPOXY FILL

Epoxy filling holes is the process of encapsulating the via with an epoxy resin that is a close CTE match to the base material. This is a selective process and will add cost and lead-time to the build. Epoxy filling of holes is done selectively with unique processes that accomplish these steps. First, the panel is drilled with only the holes that require filling. Second, the panel is then copper plated to create the adequate copper thickness in the hole for reliable interconnect. The holes are then filled with epoxy and cured. Post curing cleaning and planarization are done to remove the excess epoxy residue and then the filled holes are plated again to produce the copper cap over the non-conductive epoxy fill.

### 9.1.1. THROUGH HOLE

Through hole filling is a common practice and the most widely used requirement for the epoxy filling process. When filling thru holes consideration should be taken to ensure that the following requirements are met to achieve the best finished results.

- Smaller holes will fill with less dimpling. A common DHS for filling would be a 0.0098 inches / (0.25 mm) drill bit. Larger holes will be more susceptible to dimpling.
- Hole sizes should be limited in variance for filling. If a small hole 0.0098 and a larger hole 0.019 require filling then the probability of the 0.019 hole having excessive dimpling will be likely. Multek recommends all filled hole sizes be within 0.005 mils or less in size to ensure dimpling spec will be met. If dimpling is allowed on larger holes, then a variance of up to 0.012 inches is acceptable, but the larger holes will have in excess of over 0.002 inches of dimple in the via pad.
- It is recommended a copper cap be placed on the top of all epoxy filled through holes. This will ensure that during post fill processes the hole fill material is not compromised. Some processes post VIPPO will have a chemical process that can breakdown the epoxy or cause entrapment.
- See the individual plant capabilities in the below Capabilities Survey section for Epoxy Fill capabilities.

### 9.1.2. DIMPLING

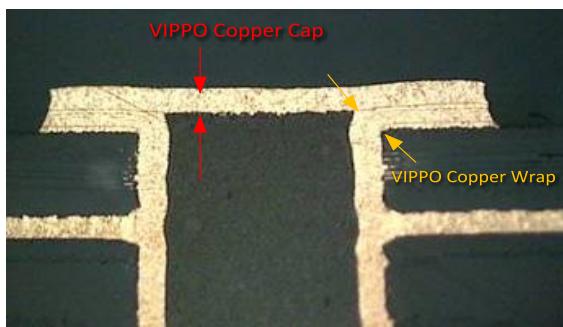
Dimpling is an unavoidable phenomenon of any hole filling process. Although the PCB manufacturer works to minimize the amount of dimpling on any VIPPO hole, it is unrealistic to spec a flat surface pad. The average dimpling of a VIPPO hole will be about 20% of the diameter of the DHS. Therefore, if you have a DHS of 0.010 inches then the anticipated dimple would be about 0.002 mils deep. Excessive dimpling can result in copper voids at these locations, which are not acceptable. With  $\mu$ Via diameter holes the amount of dimpling will be less, but anticipating a dimple 0.001 - 0.0005 inches. Often fixture probe marks are mistaken for dimpling due to the nature of the test process. Special attention to dimpling should be take on any wire-bonded pads, and noted on the drawing to ensure manufacturing inspects for these unique requirements.

### 9.1.3. COPPER WRAP

An important aspect of VIPPO reliability would be the copper wrap. The copper wrap refers to the thickness of the copper that wraps around the elbow of the hole barrel to the surface. Too thin of a copper wrap can result in quality issues during assembly with pad lifting, barrel cracks and other long-term reliability degradation. Multek recommends a minimum copper wrap of 0.0002 inches at the elbow to ensure a reliable VIPPO via.

### 9.1.4. COPPER CAP

The Copper Cap refers to the thickness of copper at the top of the VIPPO hole. This copper thickness is used to solder the lead to the SMT Pad. Multek recommends on through holes a cap thickness of 0.0008 inches and on  $\mu$ Vias a 0.0005 inch cap.



### 9.1.5. $\mu$ VIA

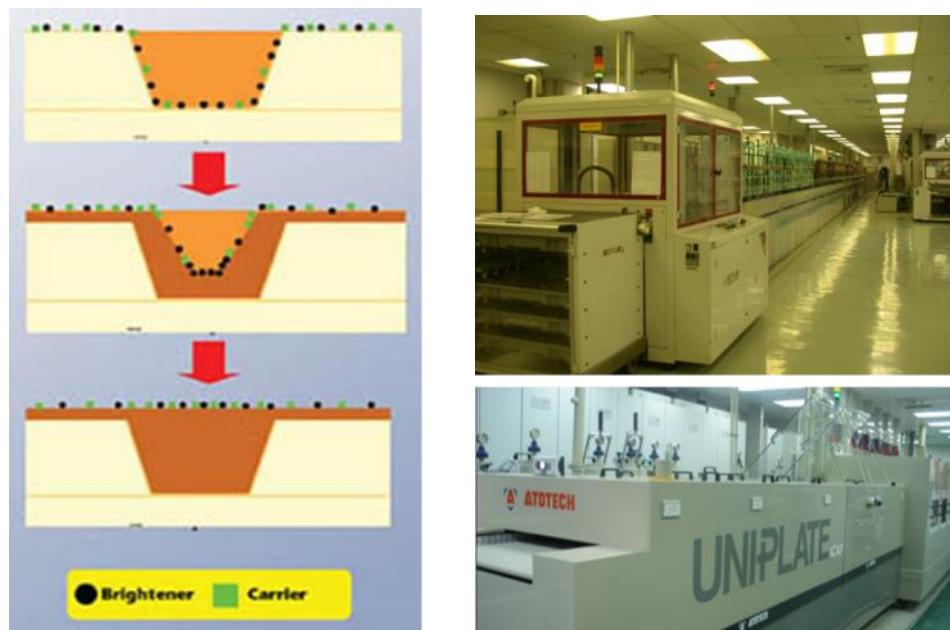
Filling a  $\mu$ Via is a similar process to the thru hole. It is recommended to fill  $\mu$ Vias with Epoxy when there is also thru hole filling requirements. It is not recommended to use epoxy filled  $\mu$ Vias in a stacked via method as laser drilling can easily perforate the copper cap and cause voiding or entrapment, that will result in potential outgassing when exposed to elevated temperatures during solder reflow.

## 9.2. CONDUCTIVE FILL

There are conductive fill materials often used their thermal conductivity properties. These are epoxy based resin systems loaded with metal particulate typically silver or copper. Although these materials have improved in processability (filling capability) over the last several years, they are still difficult to process and costly. The thermal benefits are minimal and often more thermal conductivity can be achieved in the thermal vias with minor increases in the copper thickness deposit in the hole. Multek does not offer these fills materials today but have other thermal solutions as described in section 18 Thermal Management Solutions for High Power Components.

## 9.3. COPPER FILLED

Another method of filling holes in a VIPPO process is Solid Copper Via Fill (SCVF). To proper copper fill the blind  $\mu$ Via the drill sizes of 0.005 inches or less. This process is done by introducing the drilled panel to a special plating bath that has ability to plate up the inside of the small holes faster than the surface. Copper concentrates into the hole barrels and a suppressing chemistry prevents the surface from plating. Due to this suppressing chemistry it will prevent larger through hole diameters from plating, and it is recommended to not combine PTH and  $\mu$ Via copper fill within the same designs when possible.



### 9.3.1. $\mu$ VIA

Copper filled  $\mu$ Vias are a common practice in today's commercial market. Micro Vias allow for increased routing density due to the reduced size, and the fact that they are blind and open routing space on adjacent layers to the vias. Copper filled  $\mu$ Vias are also used for VIPPO applications drilling directly into the SMT pad and opening the surface layers up for additional routing. Most packages utilizing a pitch below 0.8mm will require  $\mu$ Via drilling.

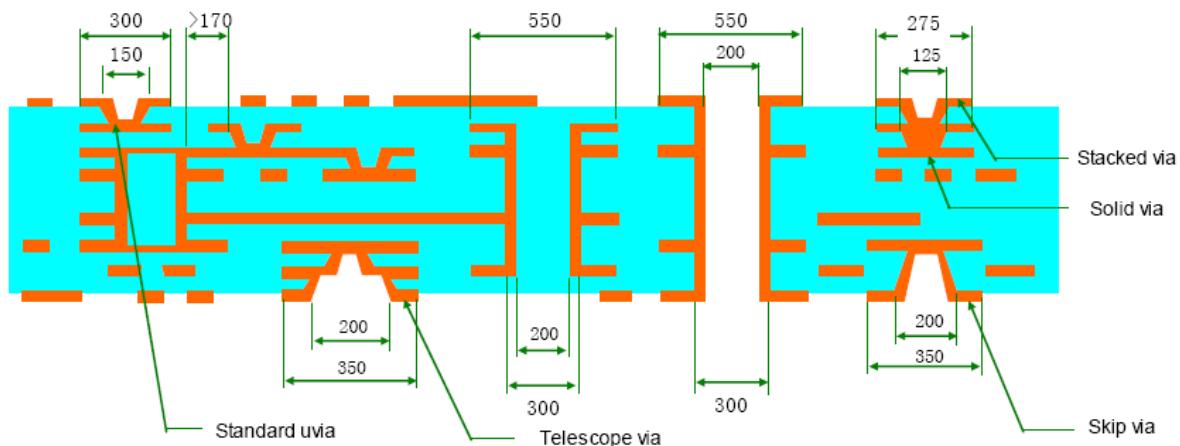
### 9.3.2. STACKED $\mu$ VIA

Stacked  $\mu$ Via are just as it states. This process is drills vias in one on top of the other in adjacent layers creating a stack of  $\mu$ Vias in the panel. It is recommended to only use copper filled  $\mu$ Vias when staking. Stacked  $\mu$ Vias can be combined with both Buried and thru hole technology, but it is recommended to eliminate any thru hole components to prevent excessive copper thickness during the multiple plating steps.

### 9.3.3. ELIC

Every Layer Interconnect or (ELIC) is a method of using stacked  $\mu$ Vias on every layer. This process starts with an ultra-thin core that has  $\mu$ Vias drilled and solid copper filled as the base. From that point, a build-up method is done, drilling and filling  $\mu$ Vias as required on both sides. This allows for the unique process of starting and ending any routing requirement on any layer. It opens up routing channels and provides the ability to reduce the overall thickness of the PCB. ELIC design guidelines follow the same structures as stacked  $\mu$ Via, but provides higher internal routing density due to the elimination of buried thru hole vias in the initial sub buildup, and having to put holes in layers that are not required for interconnect to these specific layers.

### 9.3.4. HDI DESIGN GUIDELINES



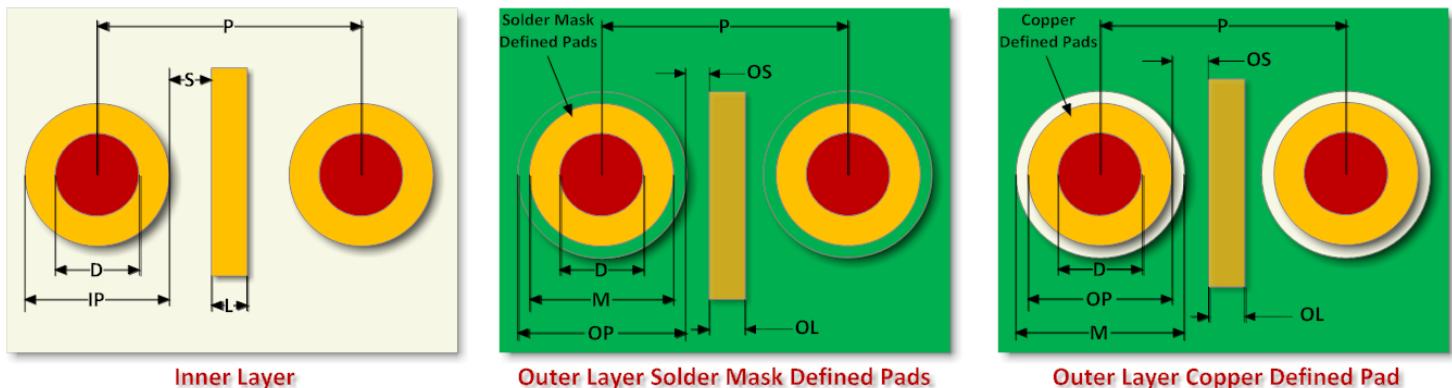
#### Design Rule:

	Drill size (um)		Pad size (um)	
	Standard	Minimum	Standard	Minimum
Standard via	150	100	300	250
Solid via	125	100	275	250
Skip via	200	N/A	350	N/A
Telescope via	200	N/A	350	N/A
Through via	300 & 275	250 & 200	550 & 525	500 & 450
Buried via	300 & 275	250 & 200	550 & 525	500 & 450

#### Notes:

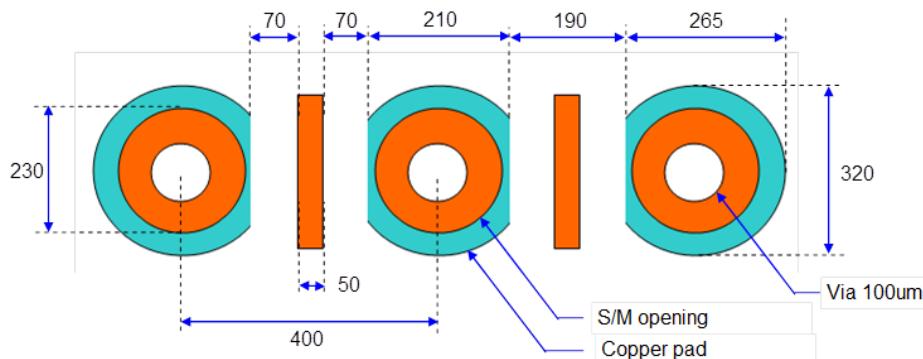
1. HDI build up material is preferred to be 1080 prepreg. 106 prepreg and RCC are also available.
2. Uvia to buried via spacing should be >170um to have better reliability.

### 9.3.5. BGA PITCH DETAILS



Pitch	P	D	IP	S	L	OP	M	OS	OL
0.5mm (Mask Defined)	500	125	275	75	75	350	250	-	-
0.5mm (Copper Defined)	500	125	275	75	75	250	340	90	70
0.4mm (Mask Defined)	400	100	230	60	50	320	220	-	-
0.4mm (Copper Defined)	400	100	230	60	50	230	280	-	-
0.3mm (Mask Defined)	300	75	150	50	50	250	200	-	-

## 9.3.6. SOLDER MASK SHAVED PADS EXAMPLE 0.4MM



## 10. SOLDER MASK COATING

Solder Mask is a polymer or epoxy coating placed on the surface of the PCB to protect the conductive areas from damage and unwanted shorts during the soldering processes, post fabrication. One of the most tedious and time consuming aspects during the front-end CAM Tooling process is solder mask cleanup. Many issues arise during the solder mask Design Rule Checks including: mask on pads, solder mask slivers and via plugging. This section will illustrate the most desired methods for designing solder mask features to help eliminate 90% of all solder mask issues. There is a varieties of colors supported for solder mask, but it is recommended when dealing with a production order to utilize green as the standard. Green mask is used in over 90% of all fabricated PCB today, which helps create process efficiencies and reduce cost. If the product is running in high volumes, then other color options are available, understanding that the UL certification for mask is required and one off color selections could affect the capabilities to UL a product in production, without added cost for qualification. Green has historically been the color of choice due to the ease of inspection for both human and automated equipment. Blue, Black and Red are also commonly used colors.

### 10.1. APPLICATION METHOD

Solder mask is applied in a vertical or horizontal screen coating, spraying or film coating methods. There are imageable and non-imageable mask, with Liquid Photo Imageable (LPI) the most common method of application today.

#### 10.1.1. LPI MASK

LPI mask is applied to the entire surface of the panel covering all pads traces and holes. The image of the required mask openings is transferred to the surface of the panel using UV light Film photolithography process or Direct Lasers Imaging (LDI). The light from the imaging device causes the mask to partially cure and harden. The areas not exposed by light remain soft and removed during the developing process, exposing the solderable surfaces.

Screen Coating of solder mask uses a mesh screen applied to the surface of the panel. Mask passes through the mesh to the surface of the PCB with a high-pressure squeegee process. This method applies a thin controlled coating of mask on the surface of the PCB.

Spray coating or mask is just as it sounds. Panels pass through a chamber that contains fluid head spray nozzles that apply a uniformed coating of mask over the surface of the PCB. This process is more conforming to the surface, but applies a thicker less planar coating of mask to the surface of the panel.

Film coating is a rare process of coating the surface of the PCB with a Dryfilm mask and then following standard LPI photo imaging processes. This mask has a tendency to be much thicker and not desirable for denser package assembly. Multek does not offer Dryfilm solder mask at any of their facilities.

## 10.2. REGISTRATION

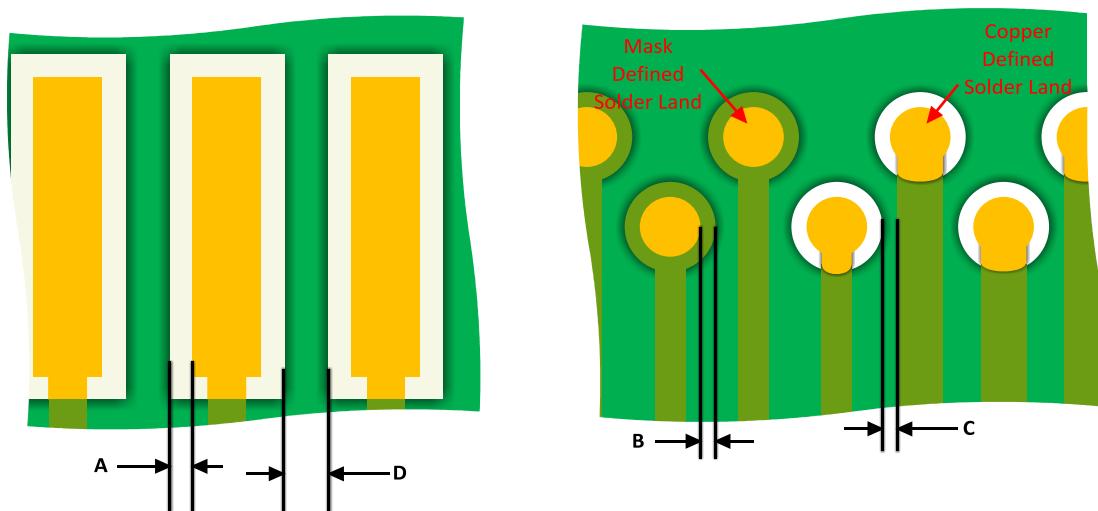
Standard registration for solder mask is +/- 0.0025 inches, which will require an annular ring of 0.0025 inches around the desired solder pad. Different Multek campuses have the ability to hold tighter tolerance of registration, so please reference the capability survey below to refine the registration for a specific design.

## 10.3. MASK DEFINED LAND PATTERN IN LARGE COPPER AREAS

Many designs will have large copper areas that have multiple solder mask defined SMT locations. These pads will have a larger copper solder area than the isolated copper pads within the same package. Adjustment to these pads is recommended to ensure unified solder pad dimensions. Many library pad stacks will use a generic clearance on SMT pads not knowing if isolated locations in future will use ground fill to connect these pads together. This can cause assembly issues with reduction in solder volume on smaller pad.

## 10.4. SOLDER MASK WEB

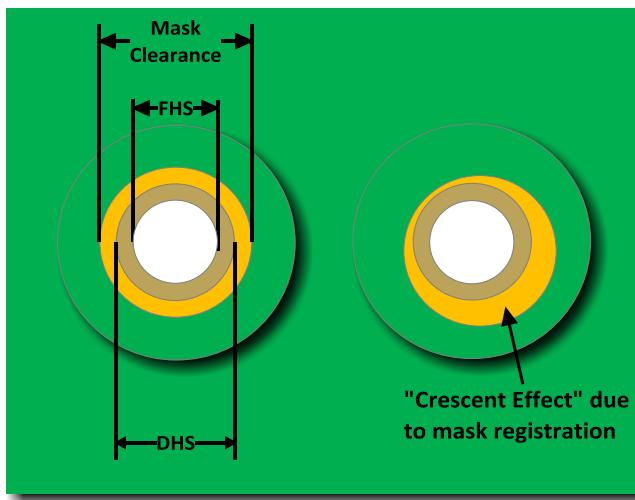
Solder mask web references the thin deposit between SMT pads that create the barrier to prevent solder from bridging between pads and creating a short. The solder mask web is also referenced as solder mask dam. Imaging methods and resolution affect the minimum width and length of a solder mask web.



Category	Standard Production Capability		Advance Production Capability	
	inches	µm	inches	µm
A. Mask Annular Ring	0.003	75.0	0.0015	38.0
B. Mask Defined Pad Coverage	0.003	75.0	0.002	51.0
C. Copper Coverage	0.003	75.0	0.002	51.0
D. Mask Web between SMT	0.0045	115.0	0.0035	90.0

## 10.5. VIA ENCROACHMENT

One of the largest challenges in the solder mask process is the removal and curing of mask inside holes. When mask cures inside holes and partially plugs a hole, it can lead to fluid entrapment inside these holes. This entrapment can later lead to assembly issues related to outgassing or corrosion. It is recommended by Multek that all thru hole vias be relieved from having solder mask cover them completely. A common practice is to encroach the mask to the via hole, and partially cover the via pad. This will increase the mask coverage at via locations to adjacent nets to prevent shorting, but will allow for cleaning and surface finish solutions to pass through the hole without entrapping and causing future reliability issues.

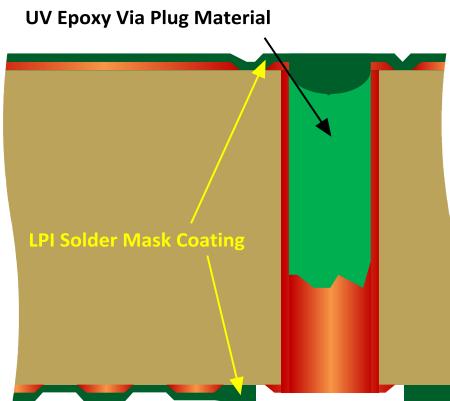


$$\text{Mask Clearance} = \text{FHS} + 6 \text{ mils}$$

## 10.6. VIA PLUGGING

Via plugging is primarily performed to ensure that there was enough vacuum hold down on the PCB during electrical test at the OEM. Today, via plugging is now required to prevent solder from flowing into these small holes, thus potentially “starving” SMT devices from obtaining the full amount of solder required for a strong solder joint.

Via plugging is a two stage process. A stencil or screen is designed from the OEM’s data and laid over the PCB. The board is then screen printed using either the stencil or screen to ensure that the holes are filled. Once this operation is performed, the “plugged” side of the board is then coated with solder mask and pre-dried. After this procedure, the second side of the board is coated with mask. It is essential that only one side of the board be plugged to prevent entrapment of chemicals and prevent “out-gassing” during the SMT assembly process. It is highly recommended that the non-component side of the PCB be plugged. Plugging the component side could cause fine pitch components, BGA’s and small discrete components not to seat flush on the surface, thus causing them to either skew from the lands or have insufficient solder. Below is just one of many ways that vias can be plugged.



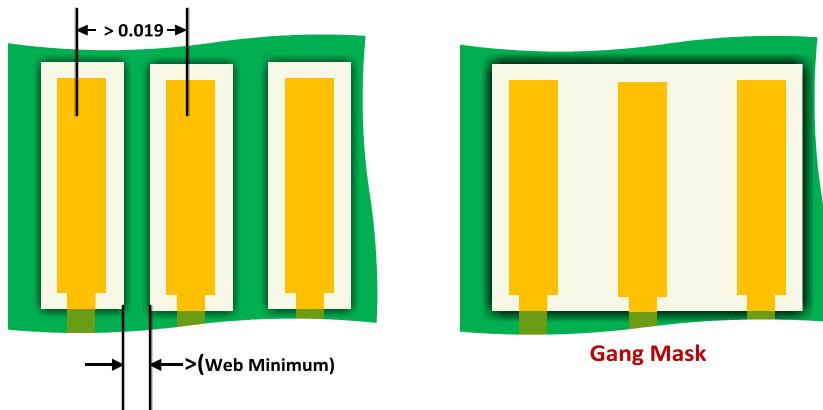
In many via plug applications, the via pad will be completely isolated from other copper features on the surface. In other cases, the via to be plugged will be separated from a solder pad by a solder mask dam as shown above. The reason for this dam is to prevent the solder from flowing away from the pad during the assembly re-flow process, thus allowing the solder to remain on the pad, proving a secure solder joint. A .003" solder mask web/dam is recommended between the solderable pad and the via. BGA pitch < 1.0mm should be reviewed to insure reliable solder joints.

## 10.7. VIA CAPPING

Via Capping is the process of applying a Solder Mask cap over a via pad to cap the surface of the pad and prevent any foreign materials from the opposite side migrating through the via. This process of Via Capping uses a UV or Epoxy based mask before the LPI process. Other forms of Via Cap would involve just covering the vias with LPI from one side. Multek recommends not Cap the vias from both sides of the PCB, as this could result in solution entrapment in post mask processes. Via Capping will not provide 100% coverage of a via hole, as the capping material will void at times during the curing process.

## 10.8. GANG MASK CLEARANCE

When mask web spacing becomes too thin to ensure proper adhesion, Gang Mask Relief is recommended. This is typically required on any SMT pitch less than 0.019. The Capability Survey at the end of this document references the minimum web widths available. Gang Mask options can be performed during the PCB Tooling process, but it is recommended these mask modifications to be done during design. At minimum, a drawing note detail the permission to gang relief, as needed, for smaller pitched packages. Any reduction in mask clearance, below production standards, to increase Mask Web between SMT Pads will result in mask encroachment onto the solderable surface. This should be done with caution as to not affect post fabrication assembly yields.



## 11. LEGEND IMAGING

Legend Imaging is the process of applying nomenclature on the surface of the PCB that indicates key component locations, polarity, part level markings and vendor traceability markings. With the density of PCBs ever increasing, it is becoming more and more difficult to place nomenclature on a PCB.

### 11.1. METHODS

The primary method of applying legend is with a silk-screening process. During the silk-screening process a stencil is applied to a meshed screening frame and ink is forced through the mesh onto the surface of the panel in the stencil openings. Alternatively, an Inkjet printer, common in practice of a desktop is used. The inkjet method applies the image to the surface of the panel through an imaging head as it passes over the panel. All silkscreen inks are epoxy based and cured via a post application baking process. Due to the nature of this these processes different density and resolution are available, but it should be noted that the inkjet method allows for more dynamic imaging and lot code serialization as the panels are uniquely imaged and allows for dynamic text variables to be used for serialization.

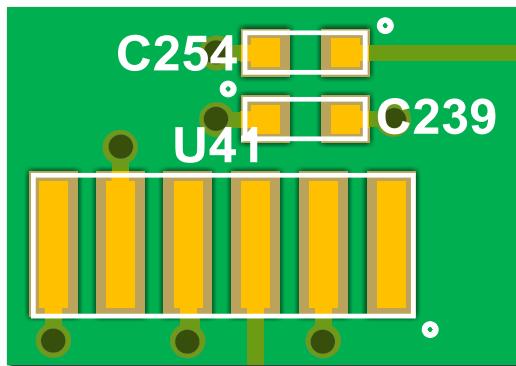
### 11.2. CAPABILITIES AND STROKE WIDTHS

Where vias are tented/plugged the silkscreen text may be placed directly over the via. Where the vias are open, silkscreen must be placed a minimum of .005" from the via hole. The Min. Text stroke width is .006 inches with letter spacing .005 inches minimum.

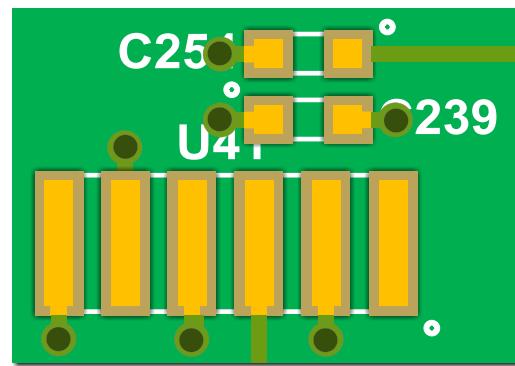
### 11.3. CLIPPING

Legend markings placed near or on top of a solderable surface will be clip free of ink to prevent soldering issues with ink marking or bleed onto these surfaces. This clipping process can result in illegible markings on dense designs and designers should take care during the layout process to ensure markings are free of solderable areas. Multek will clip all silkscreen up to 0.005 inches away from solderable surfaces. Extensive labor is involved in moving markings and that will require additional tooling time and cost if done. Advance notification on documentation should outline these requirements as needed. Standard operating procedures will be to clip without notification to the customer. Legible nomenclature is the responsibility of the designer, not manufacturing. Designers should ensure all critical component and part markings are free of soldering location or surface metal exposed in the solder mask layers.

Silkscreen Image as Designed



Silkscreen Image after Clipping



## 12. SURFACE FINISHES

There are many varieties of surface finishes offered today. Many finishes have both benefits and liabilities. Careful consideration to cost and post fabrication assembly requirements should be considered when selecting a finish to meet the needs of the specific design. The primary method of applying surface finish would be through a plating or coating process, each with unique process requirements and benefits. Most finishes are Solder Mask over Bare Copper (SMOBC), with the finish applied to exposed copper surfaces. The less common practice is a full body plating method, which applies the surface finish to all of the outer layer copper surfaces before solder mask is applied. .

Vertical dip tanks or in-line horizontal system are used to apply surface finishes. Surface finishes promote and protect the conductor area of the PCB for the Assembly process and to prevent oxidation and surface contact reliability, which bare copper cannot achieve over time. Multek recommends using OSP when possible for both cost and solder joint reliability, but will not take liability for the proper selection of finish to meet the design requirements. Multek encourages our customers to contact the engineering resources in their area to go over the details of finish requirements to ensure achieving all post fabrication requirements.

An Ideal Surface Finish will be:

- Solderable
- Coplanar
- Reliable for In Circuit Test
- Lead-Free (RoHS and WEEE compatible and compliant)
- Contact Resistance (Compression Connection)
- Daughter Card Edge Fingers, Button Pads and Ground Rails
- Tarnish Resistance
- Wear Resistance
- Chemical Resistant
- Good for Wire Bonding
  - Gold & Aluminum
- Compatible for other surface finishes
- Handle multiple solder reflow cycles
- Work with multiple component types
- Cost Effective
- Reliability

- Shock, Vibration and Thermal Cycling

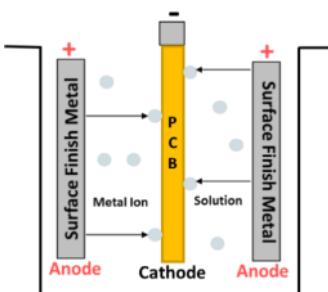
## 12.1. PLATING METHODS

### 12.1.1. ELECTROLYTIC PLATING

Electrolytic Plating is achieved by passing an electric current through a solution (Electrolyte) containing dissolved metal ions allowing the metal to deposit on the conductive surface of the PWB.

Electrolytic Plating requires:

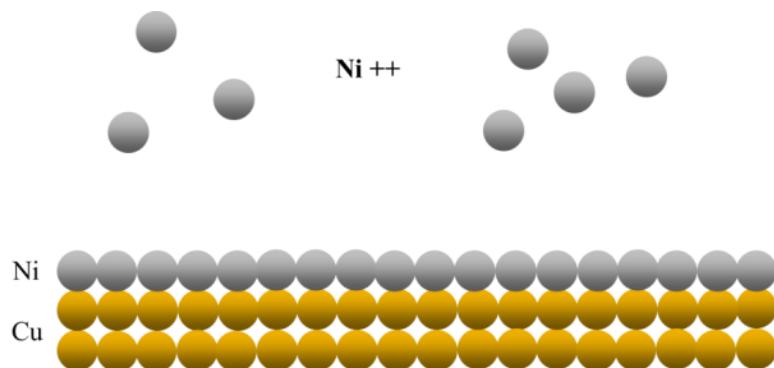
- Anode
- Cathode
- Electrolyte
- Metal Ion



The PWB serves as the cathode, connected to negative polarity of the rectifier. The Anode connects to the positive polarity of the rectifier. The metal ions in the plating bath reduced at the conductive surface of the PWB building up the metal thickness. The Voltage, Amperage, Temperature, Time, and Purity of the solutions determine the properties and amount of the deposit.

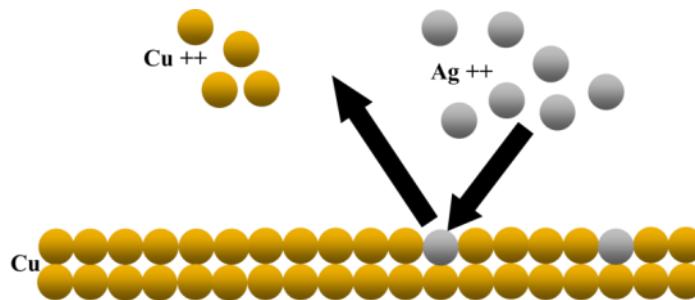
### 12.1.2. ELECTROLESS PLATING

Electroless plating is just as it sounds, it has no rectification requirement and no external electrons are required. Electroless plating utilizes a chemical reducing agent to supply the electrons needed for metal deposition. Hydrogen is released by the reducing agent, oxidized, creating a negative charge to the PCB surface. A catalyst will deposited to the copper surface to facilitate the deposition. The plating starts once introduced to the bath and will deposit continues upon reaching limitation of ionic exchange, but never truly finish deposition until removed from the bath. Electroless Finishes have a tendency to be more uniformed in deposition as they are not current density dependent. Generally, they are also harder and more brittle depositions than electroplated finishes.



## 12.1.3. IMMERSION FINISHES

Immersion Finishes are similar to Electroless Finishes. The common difference is the ionic exchange of a molecule on the surface of the panel with the surface finish metal. Immersion finishes are self-limiting on deposition thickness and will eventually stop plating the finish metal.



Galvanic Displacement – A simple exchange of Copper and Silver Atoms. No Reducing Agent is required.

## 12.1.4. COATING FINISH

Not all surface finishes are applied through a plating process. There are a number of surface finishes, which are considered coatings. In these applications, the exposed copper is cleaned through a micro-etch process to remove any oxides and residues. The cleaned copper surface is coated with either solder (HASL) or a protective sacrificial coating that will dissolve always during the assembly process. A typical coating and Multek's preferred surface finish offering is an OSP coating.

## 12.2. MOST COMMON SURFACE FINISH TYPES

### 12.2.1. OSP (ORGANIC SOLDERABILITY PRESERVATIVE)

Advantages	Disadvantages
<ul style="list-style-type: none"><li><input checked="" type="checkbox"/> Sacrificial coating</li><li><input checked="" type="checkbox"/> High reliability for SAC based solder joints</li><li><input checked="" type="checkbox"/> Flat, coplanar pads</li><li><input checked="" type="checkbox"/> Re-workable by PCB supplier</li><li><input checked="" type="checkbox"/> Fair Shelf Life</li><li><input checked="" type="checkbox"/> Cost effective process</li><li><input checked="" type="checkbox"/> Easy to control process</li><li><input checked="" type="checkbox"/> High temperature OSP's are available</li></ul>	<ul style="list-style-type: none"><li><input checked="" type="checkbox"/> Limited heat cycle capability</li><li><input checked="" type="checkbox"/> PCBA process control critical</li><li><input checked="" type="checkbox"/> Having exposed Cu after PCBA In Circuit Test (ICT) may be a concern</li><li><input checked="" type="checkbox"/> Handling sensitive</li><li><input checked="" type="checkbox"/> Overall "tighter" process window required for assembly</li></ul>

### 12.2.2. IMMERSION AG (IMMERSION SILVER)

Advantages	Disadvantages
<ul style="list-style-type: none"><li><input checked="" type="checkbox"/> Sacrificial coating</li><li><input checked="" type="checkbox"/> High solder joint reliability with Cu Sn inter-metallic</li><li><input checked="" type="checkbox"/> Flat, coplanar pads</li></ul>	<ul style="list-style-type: none"><li><input checked="" type="checkbox"/> Adjustments necessary for press fit technology (high friction coefficient)</li><li><input checked="" type="checkbox"/> Anti-tarnishing is critical to control</li><li><input checked="" type="checkbox"/> Likes to build oxides</li></ul>

<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Consistent coating thickness</li> <li><input checked="" type="checkbox"/> Withstands multiple heat cycles</li> <li><input checked="" type="checkbox"/> Good shelf life</li> <li><input checked="" type="checkbox"/> Best wet ability of all alternatives</li> <li><input checked="" type="checkbox"/> Easy to repair (PCBA)</li> <li><input checked="" type="checkbox"/> Easy to probe at ICT</li> <li><input checked="" type="checkbox"/> Relatively simple process at PCB manufacturing</li> </ul>	<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Issues with process interruptions</li> <li><input checked="" type="checkbox"/> Likes to diffuses (and migrate)</li> <li><input checked="" type="checkbox"/> Handling Sensitive           <ul style="list-style-type: none"> <li>○ Color and look</li> </ul> </li> </ul>
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## 12.2.3. IMMERSION SN (IMMERSION TIN)

Advantages	Disadvantages
<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Flat, coplanar pads</li> <li><input checked="" type="checkbox"/> Very easy solder able</li> <li><input checked="" type="checkbox"/> High reliability with Cu Sn IMC</li> <li><input checked="" type="checkbox"/> Works well at ICT</li> <li><input checked="" type="checkbox"/> Same metal as CuSnAg alloy (does not change alloy ratio much)</li> <li><input checked="" type="checkbox"/> Well suited and proven for press fit technology</li> <li><input checked="" type="checkbox"/> Relatively inexpensive</li> </ul>	<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Anti-tarnishing is critical to control</li> <li><input checked="" type="checkbox"/> Rinsing is highly critical</li> <li><input checked="" type="checkbox"/> Likes to build oxides</li> <li><input checked="" type="checkbox"/> Diffuses into the copper</li> <li><input checked="" type="checkbox"/> Grows inter-metallic (<math>0.1\mu\text{m}/2</math> months) at RT and with every heat cycle</li> <li><input checked="" type="checkbox"/> Fewer heat cycles possible due to intermetallic growth</li> <li><input checked="" type="checkbox"/> Fear of Sn Whiskers</li> </ul>

## 12.2.4. ENIG (ELECTROLESS NICKEL/IMMERSION GOLD)

Advantages	Disadvantages
<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Flat planar pads</li> <li><input checked="" type="checkbox"/> Withstands multiple heat cycles</li> <li><input checked="" type="checkbox"/> Good shelf life</li> <li><input checked="" type="checkbox"/> Easily solderable</li> <li><input checked="" type="checkbox"/> Easy to repair on PCBA</li> <li><input checked="" type="checkbox"/> High barrel reliability</li> <li><input checked="" type="checkbox"/> Easy to use for ICT</li> <li><input checked="" type="checkbox"/> Not handling sensitive</li> <li><input checked="" type="checkbox"/> Wide process window</li> <li><input checked="" type="checkbox"/> Flexible Nickel</li> <li><input checked="" type="checkbox"/> Possible use for Aluminum Wire Bonding</li> </ul>	<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Expensive</li> <li><input checked="" type="checkbox"/> Process Chemistry requires control of numerous parameters.</li> <li><input checked="" type="checkbox"/> Contamination / Corrosion potential</li> <li><input checked="" type="checkbox"/> Brittle Fracture for BGA type packages (under mechanical load)</li> <li><input checked="" type="checkbox"/> May not be suited for high speed signals (skin effect of Ni)</li> <li><input checked="" type="checkbox"/> Adjustments necessary for Press Fit technology</li> <li><input checked="" type="checkbox"/> Ni interface between solder and Cu surface</li> <li><input checked="" type="checkbox"/> Solder Joint Embrittlement related to excessive Au content</li> </ul>

## 12.2.5. SN-Pb HASL (HOT AIR SOLDER LEVEL)

Advantages	Disadvantages
<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> “Nothing Solders Like Solder”</li> <li><input checked="" type="checkbox"/> Easily Applied</li> <li><input checked="" type="checkbox"/> Lengthy Industry Experience</li> <li><input checked="" type="checkbox"/> Easily Reworked</li> <li><input checked="" type="checkbox"/> Multiple Thermal Excursions</li> </ul>	<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Co-Planarity Difference</li> <li><input checked="" type="checkbox"/> Inconsistent Coating Thickness</li> <li><input checked="" type="checkbox"/> Contains Lead</li> <li><input checked="" type="checkbox"/> Not Suited for High Aspect Ratios</li> <li><input checked="" type="checkbox"/> Not Suited for fine-pitch SMT and</li> </ul>

<input checked="" type="checkbox"/> Good Bond Strength <input checked="" type="checkbox"/> Long Shelf Life <input checked="" type="checkbox"/> Easy Visual Inspection <input checked="" type="checkbox"/> Cu/Sn solder joint	BGA Packages <input checked="" type="checkbox"/> PWB Dimensional Stability Issues <input checked="" type="checkbox"/> Bridging Problems on Fine Pitch <input checked="" type="checkbox"/> Subjects the PCB to Thermal Shock
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## 12.2.6. SN-Ag HASL (LEAD-FREE HOT AIR SOLDER LEVEL)

Advantages	Disadvantages
<input checked="" type="checkbox"/> Easily Applied <input checked="" type="checkbox"/> Familiar HASL Dynamics <input checked="" type="checkbox"/> Multiple Thermal Excursions <input checked="" type="checkbox"/> Good Bond Strength <input checked="" type="checkbox"/> Long Shelf Life <input checked="" type="checkbox"/> Easy Visual Inspection <input checked="" type="checkbox"/> Cu / Sn Solder joint <input checked="" type="checkbox"/> Cost effective for lower technology product	<input checked="" type="checkbox"/> Extreme Thermal Excursions Application <input checked="" type="checkbox"/> Co-Planarity difference <input checked="" type="checkbox"/> Inconsistent coating thicknesses <input checked="" type="checkbox"/> Not suited for high aspect ratios <input checked="" type="checkbox"/> May not be suited for fine-pitch SMT and BGA packages <input checked="" type="checkbox"/> PCB dimensional stability issues <input checked="" type="checkbox"/> Bridging problems on fine pitch <input checked="" type="checkbox"/> Copper feature dissolution <input checked="" type="checkbox"/> Grainy & dull appearance <input checked="" type="checkbox"/> More process controls required

## 12.2.7. ELECTROLYTIC NI /Au (ELECTROLYTIC NICKEL / GOLD) – HARD GOLD

Advantages	Disadvantages
<input checked="" type="checkbox"/> Flat, coplanar pads <input checked="" type="checkbox"/> Very easy solder able <input checked="" type="checkbox"/> Works well at ICT <input checked="" type="checkbox"/> Very easy to rework (PCBA) <input checked="" type="checkbox"/> Very long shelf life <input checked="" type="checkbox"/> Long and proven track record for high end products	<input checked="" type="checkbox"/> Limitation is aspect ratio <input checked="" type="checkbox"/> Limitation in line spacing at about 4-5 mil (100-125 µm) <input checked="" type="checkbox"/> Gold is expensive <input checked="" type="checkbox"/> Ni interface between solder and Cu surfaces Solder Joint Embrittlement related to excessive Au content

## 12.2.8. SOFT GOLD

Advantages	Disadvantages
<input checked="" type="checkbox"/> Flat planar pads <input checked="" type="checkbox"/> Thicker Gold deposit <input checked="" type="checkbox"/> Good for Gold Wire Bonding <input checked="" type="checkbox"/> Highest Purity of Gold <input checked="" type="checkbox"/> Withstands multiple heat cycles <input checked="" type="checkbox"/> Good shelf life <input checked="" type="checkbox"/> Easy to use for ICT	<input checked="" type="checkbox"/> Expensive <input checked="" type="checkbox"/> Selective Image Process required <input checked="" type="checkbox"/> Not for Contact resistant <input checked="" type="checkbox"/> Process Chemistry is difficult to control <input checked="" type="checkbox"/> Solder Joint Embrittlement related to excessive Au content <input checked="" type="checkbox"/> Demarcation points could cause etch-out opens.

## 12.2.9. FLASH GOLD

Advantages	Disadvantages
<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Flat planar pads</li> <li><input checked="" type="checkbox"/> Thinner deposit</li> <li><input checked="" type="checkbox"/> Good for Aluminum Wire Bonding</li> <li><input checked="" type="checkbox"/> Highest Purity of Gold</li> <li><input checked="" type="checkbox"/> Withstands multiple heat cycles</li> <li><input checked="" type="checkbox"/> Easy to use for ICT</li> </ul>	<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Expensive</li> <li><input checked="" type="checkbox"/> Selective imaging process</li> <li><input checked="" type="checkbox"/> Not for Contact resistant</li> <li><input checked="" type="checkbox"/> Process Chemistry is difficult to control</li> <li><input checked="" type="checkbox"/> Solder Joint Embrittlement related to excessive Au content</li> <li><input checked="" type="checkbox"/> Demarcation points could cause etch-out opens.</li> </ul>

## 12.2.10. ENEPIG (ELECTROLESS NICKEL / ELECTROLESS PALLADIUM / IMMERSION GOLD)

Advantages	Disadvantages
<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Gold and Aluminum wire bondable</li> <li><input checked="" type="checkbox"/> Good solderability (also in lead-free assembly)</li> <li><input checked="" type="checkbox"/> Replacement / galvanic deposition of Palladium on the electroless Nickel.</li> <li><input checked="" type="checkbox"/> Palladium bath is less sensitive to impurities than with ENEPIG</li> <li><input checked="" type="checkbox"/> Faster processing time than ENEPIG</li> <li><input checked="" type="checkbox"/> Wider process window than ENEPIG</li> <li><input checked="" type="checkbox"/> Thinner Palladium deposit 0.3-0.5 um (1-2 microinches)</li> <li><input checked="" type="checkbox"/> Lower cost than ENEPIG</li> </ul>	<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Not common in the industry</li> <li><input checked="" type="checkbox"/> Does not have the history of the other finishes.</li> </ul>

## 12.3. CARBON INK

Common process for keypad resistance and other applications requiring contact resistance without tarnishing. Design implementation is lower technology and requires robust geometries due to bleeding and registration requirements. Multek supports this process, but we recommend contacting Engineering support for assistance on design constraints.

## 12.4. MULTIPLE SURFACE FINISHES

To help address design and mechanical requires the fabricator can apply multiple finishes. The most common additive finish would be Hard Electrolytic Gold, used for Edge Connectors and Grounding locations that are not reflowed during assembly. The Electrolytic Gold will require bussing to the plating bar. To avoid exposed metal on the surface of the PCB, the design should rout buss bars internally connecting them to a common point outside the PCB profile. Alternative methods of post plating etching the surface buss bars is capable, but will have a significant cost increase due to the multiple selective imaging and etching processes to achieve the desired finish results. Multek recommend you contact your local engineering support to discuss options when needing recessed selective Gold plating.

Common Combinations:

- Hard Gold / OSP

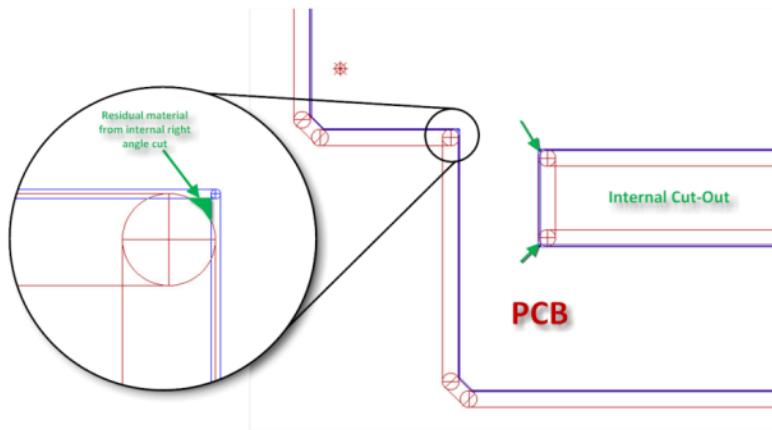
- Hard Gold / Immersion Silver
- Hard Gold / ENIG

## 13. MECHANICAL ROUTING, SCORING AND BEVELING

The mechanical process of de-panelizing the shippable PCB or shipped Array of PCB is done through a form of mechanical cutting. This is done on a NC Routing unit that will cut the parts from the larger master production panel. Scoring and other milling process can be used to help with the post assembly depopulation, but all production panels will need to be routed to produce the final shipped parts.

### 13.1. ROUTING CAPABILITIES

Routing or the cutting of the part from a production panel requires the use of cutting bits that come in standard diameters. The Diameter of a standard router bit is 0.125, 0.093, 0.062 and 0.031. The radius of the standard router bit will provide the internal cut radius available for right angles. Since round router bits are used for cutting a part, there is never an opportunity to achieve a 90° internal cut. Utilize the largest router bit available to help with efficiencies at this process. A router bit smaller than 0.093 inches will require a slower table and head movement to cut and affect the efficiencies and cost of the process.



Routing machine tolerance will affect the accuracy of the routing and ensuring copper features do not get too close to the board edge will prevent possible exposed copper. When considering routing tolerance there are standards that can be widely accepted, but there is also more precision equipment that use CCD optical alignment and precision spindle movement to limit the impact of such tolerances.

### 13.2. CONTROL DEPTH ROUTING AND MILLING

Control Depth Routing will cut cavities or allow for milling down the thickness of the laminate in localized areas. This process is not able to mill down large portions of the PCB, but selectively for recess cavities and reducing the thickness on the edge of parts.

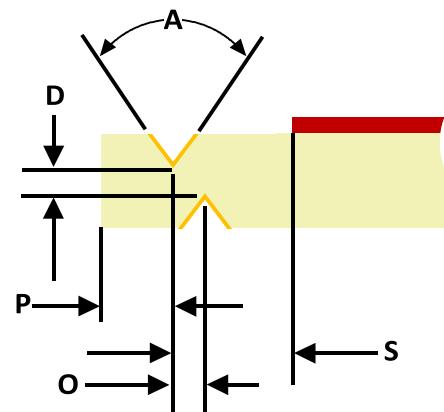
### 13.3. SCORING CAPABILITIES

Scoring is a process of cutting a v-groove into the surface of the panel to allow for ease of depopulation of the board from a production array panel after assembly. V-Groove Scoring is done by two major methods, both Mechanical cutting. The most common method for scoring is Blade Cutting. Blade cutting will pass a score cut through the entire panel and can only be done in 90° single horizontal and vertical cuts. Start and stop cuts on production panels is controlled within approximately 0.5-1.0" inches, depending on the cutting machines

capabilities. CNC mill scoring with a special v-groove bit is the second most common method. Using a CNC router to score panels is a time consuming and more expensive cutting method, but does allow for much more precision. It is critical to understand the breaking, or depopulation of the scored board from the shipped array panel can be a violent process. Any components soldered close to the part edge could have solder joint reliability issues. Blade scoring is the most cost effective method for retaining individual PCBs into a Panel, and most Assembly Houses would recommend this method as default when acceptable.

	Parameter	Standard Inches	Standard $\mu\text{m}$
A	Scoring Cut Angle	25°, 30°, 45° & 60°	
D	Material Web	0.045 - 0.015	1200.0 – 380.0
P	X & Y Position Tolerance	+/- 0.003	+/- 75.0
O	Off-set Tolerance	+/- 0.005	+/- 125.0
S	* Cu Pull Back	0.025	635.0
	Jump Score Start /Stop Position	+/- 0.030	+/- 760.0

\* Copper pull back is dependent on score depth

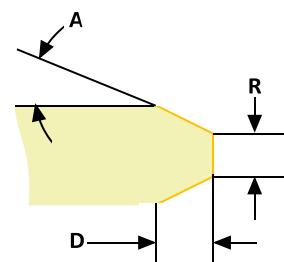


## 13.4. BEVELING CAPABILITIES

Beveling places a chamfer or tapered cut on the edge of a PCB. Beveling is done on card edge locations that require insertion into the connector for mating. The beveling process uses blades or milling machines that have specific angled cuts. When documenting beveling requirements, it is critical to ensure the depth of the cut is along with the angle. Too deep of a cut can affect how the PCB seats into the connector. A shallow bevel or missing bevels could cause connector damage by bending or compressing connector pins during insertion.

When planning for a bevel on larger PCB it is recommended to butterfly or have the edge connectors face the outside of the panel so the cuts of the edge can be done in manufacturing more cost effective. On smaller parts, utilization of CNC equipment is required to do bevels on multiple up parts were the fingers do not face the outside edge of the panel.

	Parameter	Standard Inches	Standard $\mu\text{m}$
A	Bevel Angle	20°, 30° & 45°	
D	Bevel Dimension Tolerance	+/- 0.005	+/- 125.0
R	Remaining web	<i>This dimension is controlled by the score depth and angle requirements.</i>	



## 13.5. TOOLING REQUIREMENTS

Multek requires a non-plated tooling hole of .062 (1.55mm) or greater for tolling purposes in machining process. These holes are used to pin mount to riser plates for all CNC processes after the primary drilling. Larger finished PCB sizes require larger diameter tooling holes up to but not limited to 0.125 (3.20mm). If there is no useable tooling holes present in the final design, then during the DFM process holes with specific location and size

required for production will be requested. If shipping the PCB in panel form Tooling Holes will be added to the panel break-a-way rails.

## 13.6. PANELIZATION / ARRAY CONFIGURATION AND RECOMMENDATION

Shipped panel arrays are complex and Multek recommends involving the key members of the manufacturing process to determine the best panel configuration for each design.

Multek recommends multiple PCB shipped panels allow defective parts to be X'ed out and shipped within a separate sorted package. Although this is rare, it could save up to 20% in scrap cost allowing for shipping panels with X-outs. Standard practice is 20% per panel array or 2 parts per array, whichever is larger. No shipped lot will contain more than 10% of the shipped panels with X-out. The logic behind X-outs will prevent cost for scrapping good boards within an array. Careful attention to markings and fiducial part recognition can be done to help improve bypass logic during assembly.

Key attributes to consider when developing a panel scheme for a design:

- PCB Fab production utilization
- Tab locations
- Panel flex or bow during pick and place or post fab thermal process
- Component placement in relationship to supporting scoring or rout-n-retain depopulation methods
- Overhanging component and the impact to spacing between parts and frame clearances
- Added frame material for additional support
- Overall panel size required by post fabrication assembly equipment

*Multek recommends referencing the following Flextronics's DFx Guidelines for panelization schemes.*

*General Design Guideline for Panel Drawings (Document #DFX-ZH-0-003-09).*

## 14. ELECTRICAL TESTING

PCB Fab testing is primarily considered a point-to-point, Level 1 test of the finished PCB. This process is done at the completion of the fab, but can also be implemented, as a Quality Assurance step throughout manufacturing, as deemed required by production engineering. This test will provide continuity testing between the extreme end-points of every net. Intermediate points are bypassed during the testing process, as they are redundant points of contact. More advanced testing also is available and detailed in the following section.

Testing Charges are independent cost outside of the PCB piece price. Being strategic with your testing strategy can save money over multiple builds. If a current prototype build is planned to go through revision or any form of design change, then it is recommended to utilize flying probe testing, which is less expensive on lower order quantities. For Flying Probe tests, there is a lot charge per build but much less than fixture cost. If the design is mature and no change is planned after a pilot or pre-production release, it is recommended to utilize Fixture Testing, as this is a one-time charge for the design and build of the test fixture. Once a fixture is constructed, it can be used for follow on builds.

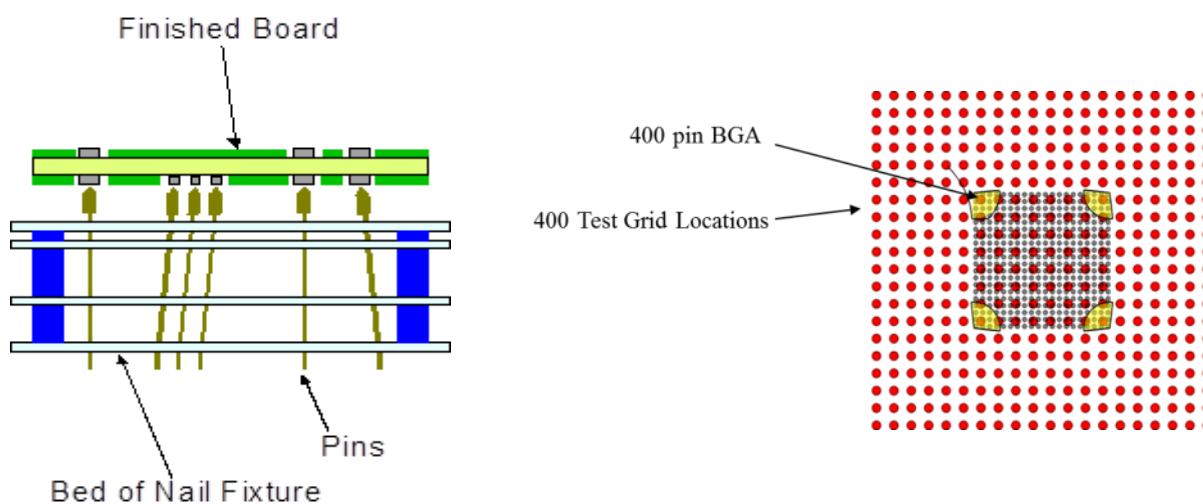
### 14.1. TESTING METHODS

Bare-board testing is considered a Phase I testing method, that verifies the point to point conductivity of each net on the finished PCB. This process is typically done on two types of systems, Pin Grid testers and Flying Probe Testers. Additional testing detailed below such as 4 Wire, LE, Impedance, Set2DLL/SPP and HiPot testing can be

done, but many of these are not production verification test and done in sample levels only with additional cost associated. For more detail on advance test capabilities, please contact engineering support at Multek.

## 14.2. FIXTURE TESTING

Fixture testing is the process of producing custom fixtures that have pins designed to interface with the PCB and are deflected to grid locations on the tester bed. Single and Double sided testers are used to test the point-to-point connectivity of each PCB before shipping. Typical grid locations are set to a pitch defined by the pogo-pin definition. Most testers operate on a 2.0mm or 0.100 inch pitch. On designs with HDI requirements, fixture testing may have limitations on the ability to have enough grid locations based on the density of the IO requiring testing in the package. If this becomes an issue Flying Probe testing becomes the preferred test method.



## 14.3. FLYING PROBE

Flying Probe test is a fixtureless test method that is commonly used for small order quantities, prototyping and along with Fixture testing when the pitch and component density is too high for standard 100% fixture testing.

Flying probe test utilizes microprobes and sophisticated movement mechanisms to probe both sides of the surface of the PCB simultaneously for continuity defects. Different probing devices will use different methods of testing to ensure speed and accuracy. Modern flying probe testing is as accurate as fixture testing with less labor time in fixture design and construction. Different brands of flying probe tester will come with advanced test capabilities such as 4 Wire - Kelvin Probe, LE Testing, High Speed Impedance Testing, Phase Differential Testing, DC Resistance Testing, High Voltage Testing and Optimized Continuity Testing. For additional details on Multek's vast Flying Probe Testing Capabilities, please contact your local FAE or Sales Associate.

## 14.4. 4 WIRE – KELVIN PROBE TESTING

4-Wire resistance testing is a measurement technique that is used to measure very low resistance values. In a normal 2-wire resistance measurement setup, the resistance of the wires between the ohmmeter and the device being measured are included in the measurements. In a 4-wire resistance setup, there are 4 wires that connect to the device being measured. A special program inside the ohmmeter then removes the resistance of the 4 wires from the measurement. Using the 4-wire resistance measurement technique, only the resistance of the device being measured is displayed/recorded.

## 14.5. LE / LATENT DEFECT TESTING

LE Testing is an advance technology potential defect validation system. The test provides the ability to pick up changes in resistance as a result of increased current induced temperature. This test can potentially find micro-crack traces, hole barrels and other factors that could result in long-term defects potential. This testing process is done on a Flying Probe type tester, and is not conducive for production processing at this time. Any LE Testing will have addition testing cost and additional lead-time added to the process cycle time. LE Testing is currently supported at Multek within Higher Reliability product and done on a Sample basis for ensure process predictability.

## 14.6. IMPEDANCE TESTING

Characteristic impedance is typically measured using a TDR (Time Domain Reflectometer). The characteristic impedance is an electrical property of a transmission line. It is dependent on the electrical properties of the materials used to construct the transmission line (for example, the dielectric constant of insulating material surrounding the conductors) and the physical geometry of the transmission line (for example, trace widths and thickness of the dielectric material). It is usually expressed in ohms. A common characteristic impedance for single ended transmission lines is 50 ohms. A common characteristic impedance for a differential pair transmission line is 100 ohms.

## 14.7. HiPOT TESTING

High pot testing is conducted on finished raw PWB's to insure isolation between all power / ground planes. Testing may be conducted with respect to current leakage or megohms resistance between biased layers. The typical voltage applied to the bare board is 500V. With smaller dielectrics and the use of buried capacitance cores, voltages applied to the board are lowered so as not to damage these thin core materials. Currently Multek HiPot tests all buried capacitance cores prior to processing.

## 14.8. SET2DIL AND SPP TESTING

The Intel developed SET2DIL (Single Ended TDR two Differential Insertion Loss) and the IBM developed SPP (Short Pulse Propagation) test methods are two specialized test methods that use a TDT (Time Domain Thru) measurement to extract frequency domain information about a transmission line. Both test methods consist of two parts. In the first part, a TDT measurement is made of a specially constructed transmission line. In the second part, the TDT measurements are converted (using a sophisticated conversion algorithm) into their frequency domain equivalents (for example dB loss at a particular frequency). A special designed tester is used to make these measurements. These test methods are typically used to establish the loss performance of a new design and not as an ongoing process control tool.

# 15. PACKAGING & SHIPPING

## 15.1. DELIVERABLES

Deliverables are part of the shipping package that contains required documentation and Certification of Compliance. Multek will provide a wide range of reports and analysis to support shipments. Extensive analysis is done on regular bases to qualify process control and compliant to industry standards. Addition reports such as ISO Certificates, Part Number Qualification Report, Certificate of Compliance to IPC Standards, First Article Report and RoHS Compliance certificates are available upon request.

It is important to communicate all deliverable requirements, to ensure compliance. Additional Cost may be associated to extensive deliverable requirements.

## 15.2. POST FABRICATION LAB ANALYSIS

Other more complex documentation and deliverables that require extra lab analysis or outside validation are available. Multek does have extensive Lab support to both unique facility and independent to the different divisions within Multek. Utilizing these resources is highly recommended, and additional details on these support functions are available in Engineering Services section later in this document.

It is important to communicate a full scope of work detailing all requirements. Additional Cost may be associated to more complex and labor intensive analysis work.

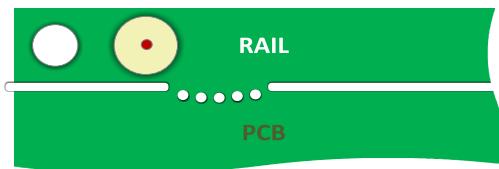
## 15.3. PACKAGING METHODS

Packaging methods are unique to the specific shipping requirements. Multek does make request to help eliminate potential issues that can compromise the product during shipping. Multek will use ESD packaging both Pink Vacuum Sealed Shrink-wrap and Nickel ESD bags. Both standard and “Silver Saver” Slip Sheet Paper is used to separate individual PCBs, which ensure bulk packaging does not cause surface damage. Humidity sensors and desiccant packs are standard packaging requirements.

Multek ships the individual PCB in bulk packaging as default, not individually bagged. The packaging requirement is based on the size and weight of the PCB. All packages are shrink-wrapped and vacuum sealed to ensure minimal environmental exposure during transit. Due to the potential of additional shipping cost, custom packaging requirements should be documented and confirmed by Multek.

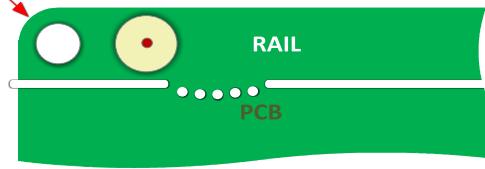
Multek recommends rounding all sharp corners of the PCB with a minor radius. Removing the sharp corners will prevent the PCB from piercing the environmental packaging during transit and degrade the reliability of the shipped content.

Standard shipped board or panel edge



Recommended edge rounding

Round Sharp Corners on outer edges



## 15.4. SHELF LIFE AND HANDLING

All PCBs have a shelf life. Two major issues influence shelf life, moisture uptake in the material and surface finish oxidation. Both of these issues will occur over time as the PCB is exposed to open environment, specifically with varying humidity and temperature changes.

Multek's recommended surface finishes shelf life for the applicable finish. The shelf life for such finish is compromised when the package has been opened, or the temperature and humidity controls have not been met for proper storage.

Surface Finish	Shelf Life in Months
Hot Air Solder Level – Pb (HASL)	12
Organic Surface Preservative (OSP)	12
Electroless Ni, Immersion Au (ENIG)	12
Electrolytic Ni, Electrolytic Au (ENEGL)	12
Electroless Ni, Electroless Pd, Immersion Au	12
Selective ENIG / OSP	12
Immersion Ag	6
Immersion Sn	6
Bondable Au	6

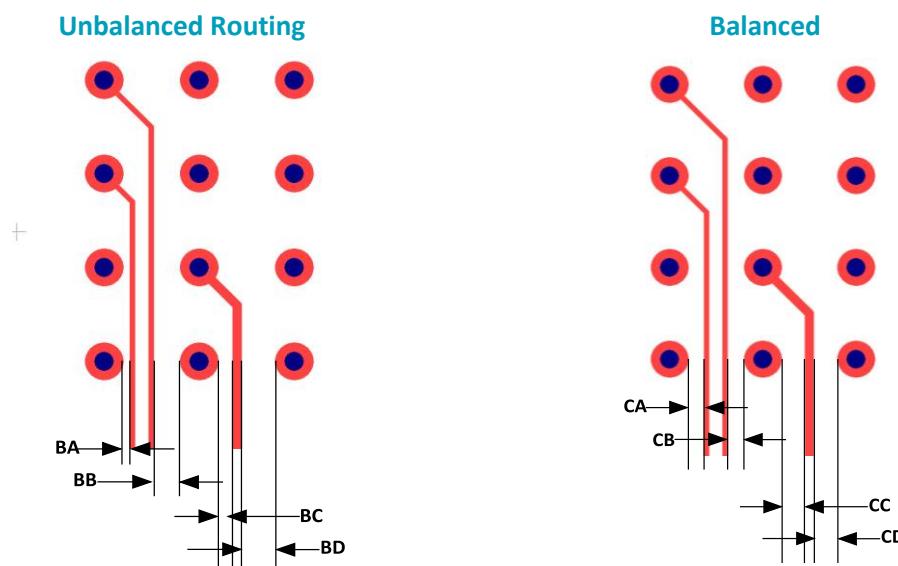
- Recommended storage to ensure no shelf life compromise is 21°C, +/- 3°
- Humidity controls are 50% +/- 10%.
- In the event a surface finish other than those outlined above is used, a Multek FAE representative can verify the shelf life.

## 16. TECHNIQUES TO IMPROVE YIELDS AND AVOID PITFALLS

### 16.1. ROUTING SCHEMES FOR HIGHER YIELDS

Routing for higher yields is a challenge for most designs. The packages used in any specific design will drive the routing technology required for the PCB. Below are common rules to apply when determining the routing rules for layout.

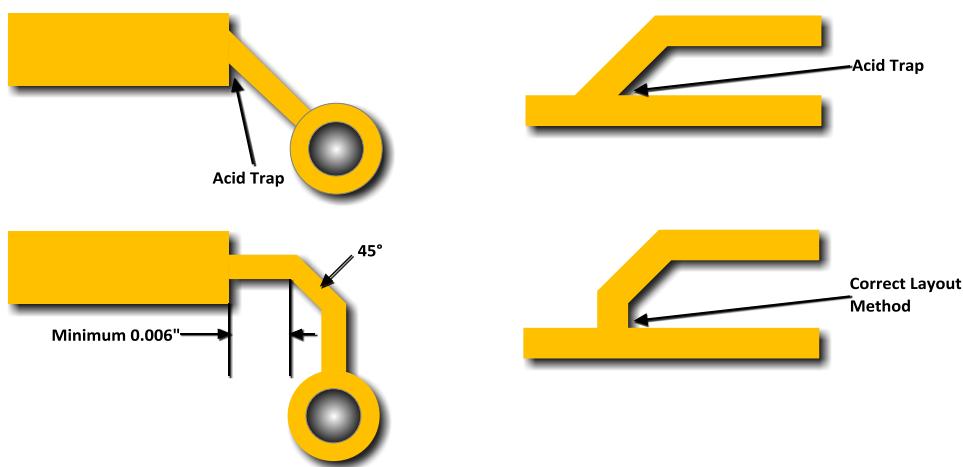
- Consider routing critical traces on the inner layers whenever possible. Surface copper has a tendency to be slightly less predictable in etch tolerance and thickness.
- Spacing is more critical to fabrication than trace width. Remember that PCB Fabrication is more about the copper you do not want, and then the copper you do want. If compromises need to be made it is important to consider not affecting the spacing between copper features as much as the line width.
- Utilize the most robust line width, as the design will support. Even though you may need 0.003 inch traces between BGA pads, you may want to consider increasing the line widths to a more robust width once you have routed outside the package. Although it may not help with the overall cost in relationship to technology drivers, it could improve yields and proved cost saving related to higher yield down the road.
- It is a common practice to route traces at the minimum DRC of an adjacent pad. It is recommended that, the single trace be routed equidistant between the two pads. This will eliminate the potential for shorting, which in turn will increase yields. Below left depicts a design that is utilizing the minimum DRC for routing two traces between Vias. The right design illustrates routing using line to line centering between pads. The second scenario will produce higher yields with less chance of shorting.



Spacing BA and BB should Equal as detailed in CA and CB.  
Spacing BC and BD should Equal as detailed in CC and CD.

## 16.2. ACID TRAPS

Any angle in a trace that is < 90 degrees has the potential for collecting and holding chemicals from the many chemical processes used in the manufacture of printed circuit boards. These acute angles can trap etchants or other chemicals that could produce defects on the PCB over. There also is a potential concern of small sharp pieces of photoresist lifting off these areas and re-depositing on the PCB image, creating either a short or open hence affecting yields. It should be a rule that traces are to be 45 degrees or greater in all designs with angles of greater than 90 degrees. Below is a typical acid trap.

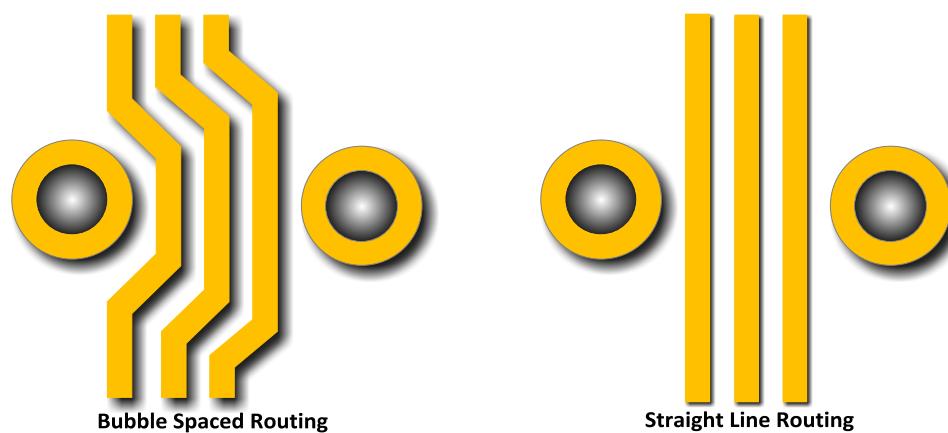


It is not recommended to route a trace out of another trace, but when required routing a secondary trace from the original, always use a 90° routed trace when exiting.

## 16.3. BUBBLE SPACED ROUTING

When routing through dense areas, do not allow the traces to be “bubble spaced”.

Do not allow the minimum DRC to “bubble” the traces around vias. It is highly recommended that the traces be re-routed so as they pass between the vias in a straight line. The fewer the bends in the traces, the less likely a yield issue will arise with opens or shorts.

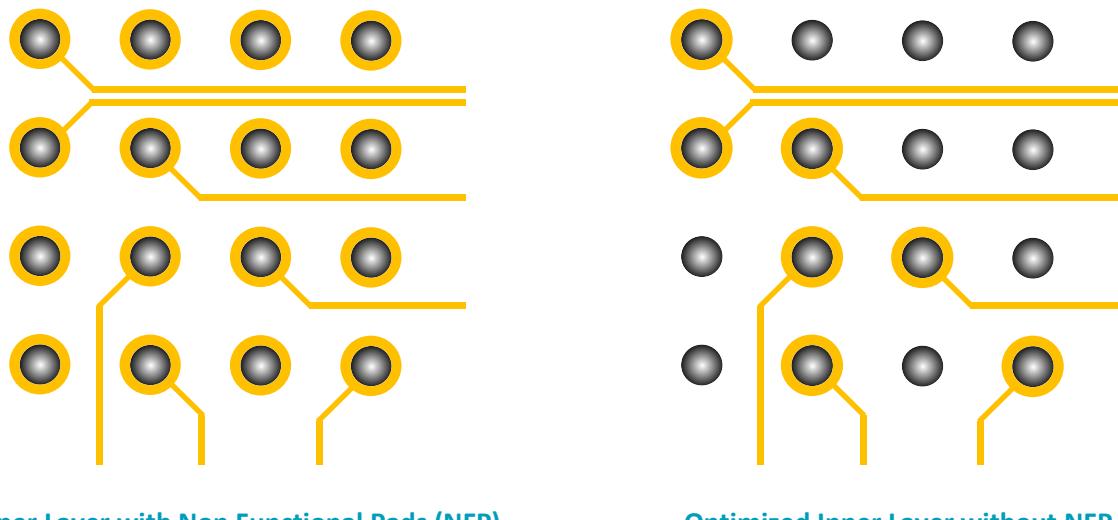


## 16.4. NFP REMOVAL

When fabricating PCBs, there always exists the possibility of traces shorting to pads during the plotting and plating or etching processes. The removal of non-functional pads on the inner layers will lessen the possibility of this occurrence, thus potentially increasing overall yields. The removal of non-functional pads from the outer layers of buried via boards is not possible due to the construction of the PCB.

In addition, the removal of the copper on these layers increases the life of the drill bit, as there is less copper to drill through. Non-functional copper pads have a tendency to “spin” causing plating issues in the hole where there is no functional reason to having the pad there. The yields are higher with the non-functional pads removed.

This can be performed either at the OEM during the artwork generation or at the PCB facility during the front end process. It is preferred that the customer remove these non-functional pads.



## 16.5. ADDING NFP FOR THICKER PCB AND BACKPANELS

On High aspect ratio designs, Multek recommended not removing all the NFP from the design. Including NFP on internal layers provides for higher reliable hole barrels and prevents hole separation and other thermal related stress defects. On larger diameter drilled holes > 2.0mm and all Press-Fit holes, we recommend leaving or adding NFP on the designs. This practice will promote better copper adhesion to the hole wall. Leaving the NFP on the design will allow for manufacturing to optimize the locations pads are required, to ensure the highest of hole wall integrity and focus of not increasing cost for drilling due to the reduction of holes drilled per bit.

## 16.6. ADDING COPPER FOR DRILLED SLOTS AND EDGE PLATING

As with high aspect ratio drilled holes, plating required on the edge of boards and on internal slots or cutouts should have copper added to the inner layers. Whether it is functional copper, tied to a Plane, or non-functional, this additional copper will support the adhesion of the copper plating to the sidewall of the routed slot or board edge. If no copper is added, the part can blister and peal during elevated thermal cycles during assembly.

## 16.7. COPPER BALANCE

There should be a balance of copper across any given layer. As detailed in the below graphic, during the etching process in order to completely remove most of the copper from the left side of this sample, the fine pitch lines that are isolated will be over-etched. This situation could greatly reduce yields on the PCB.



To fix this issue a “thieving pattern” should be added to the layer by the designer to balance the layer. This should be performed by the designer so as to produce the IL with the required hole clearances.

This could be accomplished by adding solid sections of copper (usually tied to ground) or using a pad pattern (such as 30 mil round pads on 50 mil centers). Do not use a cross hatching or checkerboard patterns. These patterns will produce many locations with slivers of copper and photoresist that dramatically reduce the yields.

### 16.7.1. THIEVING

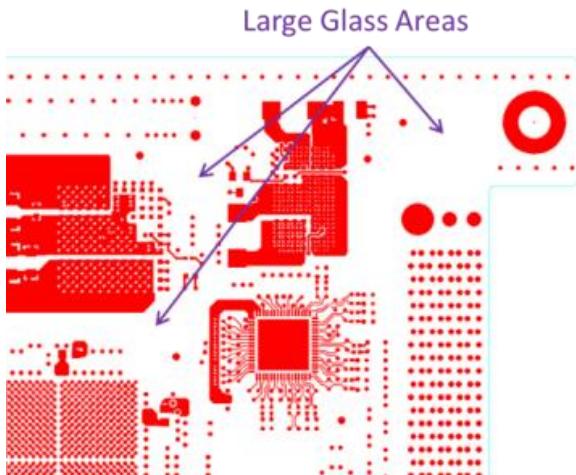
PCB designs containing isolated features create problems in manufacturing. Isolated features attract more copper during the plating process due to a higher current density. The result of this is over-plated features, i.e. pads, lines, fiducials which means the board may not conform to our customer's plating specification, and we will suffer from solder mask coverage problems (over the high lines). To overcome this, thieving should be added on any design containing isolated features or fine lines where spaces are .006" or less.

Typically, any thieving request will be asked during DFM. When documented on the fabrication drawing or customer specification Multek will typically share the thieving pattern with the customer to ensure it meets with their requirements.

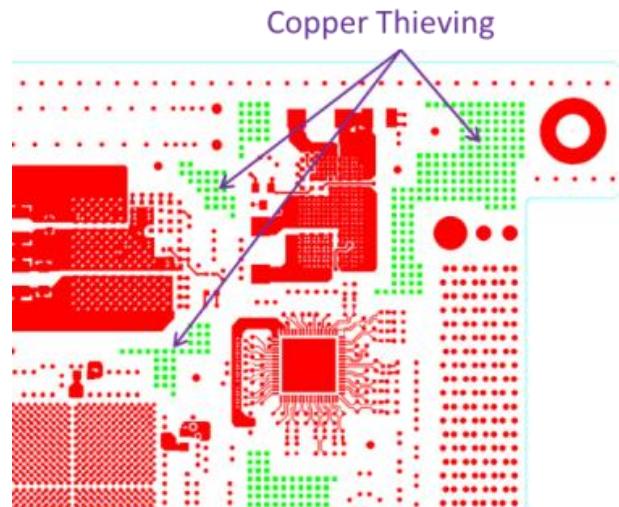
## Recommended Thieving Pattern:

- Square pattern with 0.0255 (0.63mm) pad on 0.040 (1.00mm) pitch
- Keep out can be anywhere from 0.100 (2.54mm) to 0.250 (6.35) from copper features.
- On internal layers, specifically signal layers, Multek will take into consideration adjacent trace layers and ensure no thieving overlaps traces on adjacent layers.
- Plane layers should add thieving if they have low-pressure areas and/or have large areas of missing copper.
- Multek will add thieving to all break-a-way rails.

Surface Layer Before Copper Balance



Surface Layer After Copper Balance

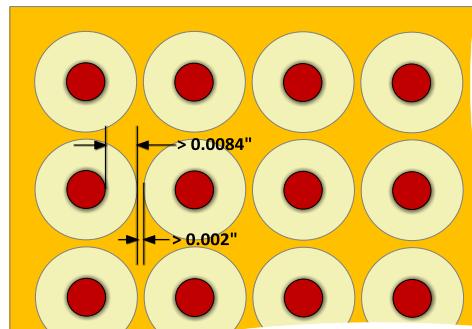


## 16.7.2. MIXED SIGNAL/PLANE LAYER

When designing an inner layer with traces on the same layer as a plane, the Cu thickness ideally should be 1/2 oz. Cu to a max of 1 oz. Cu. Copper areas should be balanced so as to reduce the risk of over etching.

## 16.8. PLANE SLIVERS

With PCBs becoming denser and via sizes becoming drastically smaller, designers are now able to place vias closer together and reduce layer count. It is important to note that in doing so, problems can occur on plane layers with respect to the proximity of via to via. Even though the vias pass the DRC rules check on the CAD platform, the design of the antipad (clearance) could result in slivers occurring between the clearances causing fabrication problems.



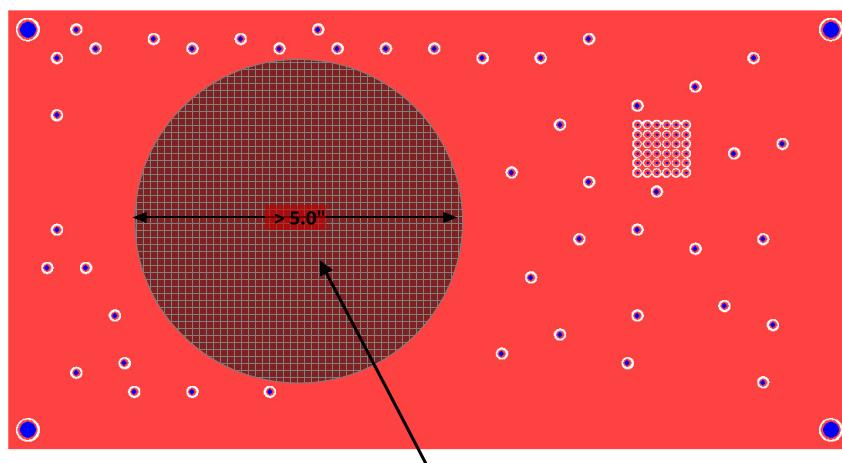
It is common in designs to have the antipad .020" larger than the DHS. This will allow for adequate spacing of copper from the drilled hole to prevent potential plane shorting due to registration tolerances. It is important to recall registration tolerance on signal pads will allow for break-out. As a result of potential break-out the plane clearance will need to be large enough to not short to the drilled hole. Having adequate material from a hole barrel to the voltage planes is also critical to prevent CAF and other reliability issues related to material breakdown during drilling along the glass bundles.

Careful attention should also be made to ensure that the copper volume meets power requirements and that the diameter of the antipad clearance does not reduce the copper web below minimum acceptable width.

With sub 1mm designs it is necessary to leave sufficient copper in the plane so as to provide a reference for the signal on the layer above and below.

## 16.9. UN-PIERCED COPPER

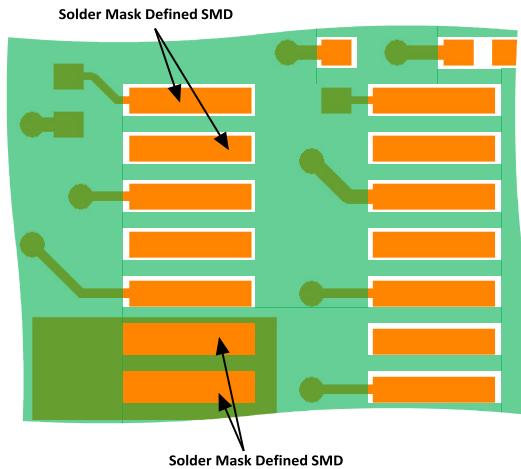
On large PCBs, especially back-panels, designers are utilizing more and more power planes embedded within the board. It should be understood that UL-796 has a requirement that ALL copper planes should have a plated-thru hole within specific areas on the plane. The figure below is an example of a copper plane that has no PTH within a 5.00" area.



Within this 5.0" diameter UL-796 requires the copper to have at minimum 1 drilled plated hole 0.042 in diameter. The allowed factor for un-pierced copper is a unique UL value for all Fabrication facilities.

## 16.10. SOLDER MASK DEFINED SMT AND NON-SOLDER MASK DEFINED SMT

When using both Copper defined SMT pads and Mask Defined SMT pads on the same package within the layout, it is critical to ensure the copper volume of the solder pad does not jeopardize the solder joint reliability. During design large copper fill areas could cover and fill between copper defined SMT pad in the same net. This copper fill could increase the solder pad significantly. Oversized SMT pads could prevent a reliable solder joint, by reducing the total solder volume at these locations. Careful attention to reduce these masks clearances down to reflect the proper solder pad size is recommended, specifically for small SMD pads and BGA packages under 0.65 mm.

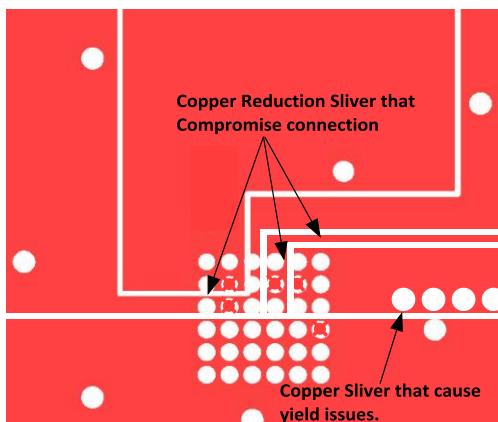


## 16.11. SLIVER REMOVAL

Slivers arise on large fill areas that often leave small gaps due to inadequate copper poor algorithms in design software. Poor routing practices cause slivers when loop-back routing occurs leaving tiny gaps between the trace and the pad. These slivers are harmless electrically to the design for most cases, but can produce issues in manufacturing of the PCB. Slivers are too small for etch and plating resist to image properly and then adhere to the surface of the panel. During manufacturing, these small resist slivers could break-down or lift from the panel. This would result in opens or shorts depending on the design, creating yield issues and increasing cost.

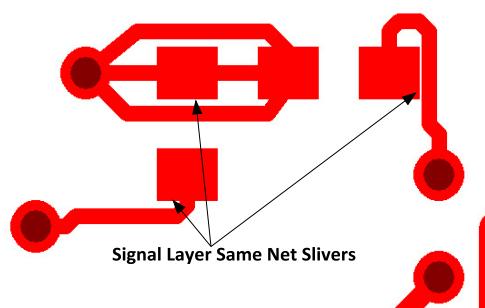
During the tooling process, Multek will optimize the data files removing any sliver less than 0.004 inches in width that are on the same net.

## Copper Plane Slivers



*Plane Slivers will require opening up copper to create a more robust connection. Careful attention to split plane routing should be done to prevent sliver shorts and open locations.*

## Signal Layer Sliver



*Same Net Slivers are common. During the Tooling process, Multek can fill in the slivers with copper to ensure no issues of photo resist breakdown and lifting occurs, causing unforeseen yield issues.*

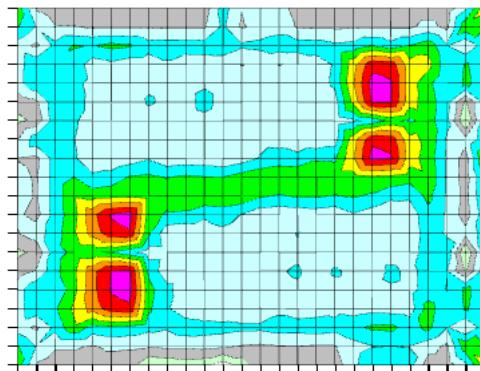
### 16.12. LARGE CUT OUT ISOLATED AREAS.

Large areas of copper relieved from the PCB can result in various defects during fabrication. If the relieved area is large and focused on one section of the panel, this can result in potential warpage causing a bow or twist to the panel. This may not be seen on the finished PCB before shipping, as thermal excursions during assembly and the removal of support rails could reveal an issue post fabrication.

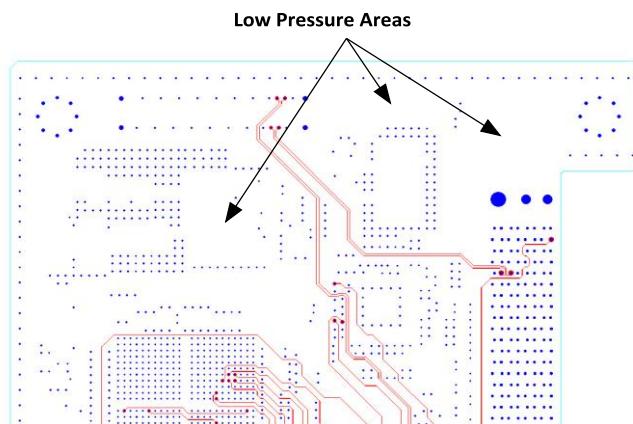
Small areas with copper removed in like locations on repeated layers within the design stack, could result in low-pressure areas. These low-pressure areas will have a disparity in thickness in the panel and could see lamination voids occur. These voids could result in thermal related defects during assembly or worse long term reliability issues. If low pressure areas are a concern, Multek will request a copper thieving pattern to be added density back into the stack for better planarity and resin distribution. Multek will run Topology simulations on stack-ups designs that represent potential issues for low-pressure areas. These areas are seen below in the sample as darker in color. The Higher the variance in color, the more likely low-pressure reliability issues will occur.

Low Pressure Areas shows troubled areas in brighter pink-orange color range. These areas are susceptible to poor resin fill, causing voiding and press thickness variance.

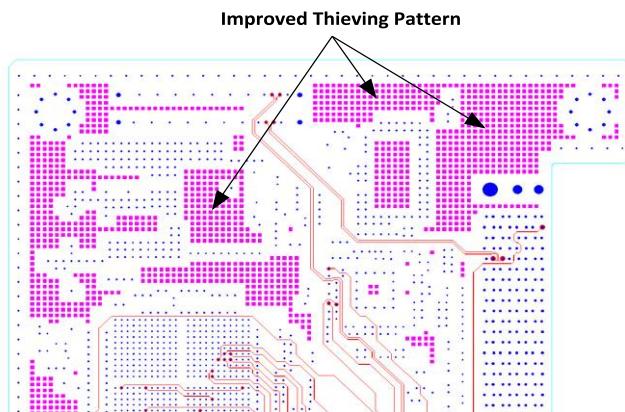
*Topology Mapping of copper density through the layers:*



Typical Internal Layer with low copper density



After Thieving



## 17. SIGNAL INTEGRITY

Signal Integrity deals with those aspects of a PCB interconnect (traces + vias) that have the potential to attenuate and distort a signal that passes through that interconnect. An ideal interconnect does not attenuate or distort the signal. However, all practical interconnects attenuate and distort a signal to a certain extent. The goal of Signal Integrity is to minimize the attenuation and distortion to an acceptable level.

Attenuation and distortion are dependent on the materials used to construct the interconnect (dielectrics and conductors) and the geometry of the interconnect (vertical vias and horizontal traces configured as transmission lines). Any loss mechanism that varies with frequency also introduces signal distortion. Since most interconnect losses are frequency dependent, most interconnects both attenuate and distort a signal that passes through that interconnect.

The table below lists some examples of material and geometry parameters that can attenuate and distort a signal.

Parameter	Introduces Signal Loss	Introduces Signal Distortion	Desired Property
Via Stub Length	X	X	Shorter is better.
Dielectric Losses	X	X	Lower Df (loss tangent) is better.
Copper Losses	X	X	Wider trace width is better. Smoother copper surface is better.
Glass Weave	X	X	More uniform/homogeneous glass weave is better.
Characteristic Impedance	X	X	Smaller deviation from nominal is better.

In many practical interconnects, chip packages and connectors also attenuate and distort signals that pass through them. In these cases, selection of the interconnect materials and transmission line geometries used in the PCB must be based on computer models of all the components that are used in the interconnect - not just the PCB portion.

## 17.1. CONTROLLED IMPEDANCE

When Multek receives a board designed for controlled impedance, several key characteristics must be verified to ensure manufacturing ease and high yields. Some of the major characteristics that must be determined are impedance type, feature size, dielectric material, copper weight, line widths, layer count and TDR test methods.

Modifications can be made to account for tight designs. In reality, there are limits to every process; even when adjustments can be made, they incur additional costs that are eventually passed on to the customer. The goal should be to work through all variables initially so that a manufacturable and cost-effective board is produced. The customer must be involved on the front end with the issues that impact manufacturing to ensure that the board delivered meets all the pre-set requirements.

Controlled impedance lines may be designed in many different configurations. The most common are microstrip and stripline structures. Variations of these basic forms include microstrip with and without solder mask, embedded microstrip, differential microstrip, and guarded microstrip. Stripline structures may be configured as single stripline, dual (offset) stripline, differential stripline, broadside-coupled differential stripline, and guarded variations of the above constructions.

The fabrication drawing should always contain an impedance chart specifying the line widths, line widths and spaces for differential impedance, reference layers and desired impedance with tolerance. Below is a typical Impedance chart.

## 17.2. CONTROLLED IMPEDANCE TOLERANCE TABLE

When impedance is specified, the nominal trace width and nominal dielectric thickness may be adjusted slightly to center the impedance within the specification range. This overcomes any differences between the modeled impedance and the actual measured impedance.

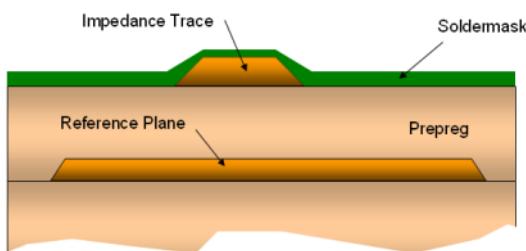
Layer	Line Width	Line Space	Reference Layer	Impedance	Differential Impedance	Tolerance
L1	.005"	N/A	L3	50 Ohms	N/A	+/- 10%
L2	.008"	N/A	L3	50 Ohms	N/A	+/- 10%
L2	.005"	.005"	L3	N/A	100 Ohms	+/- 10%

L4	.005"	N/A	L3 & L5	50 Ohms	N/A	+/- 10%
L6	.005"	.008"	L5 & L7	N/A	100 Ohms	+/- 10%
L8	.004"	N/A	L7 & L9	40 Ohms	N/A	+/- 10%
L10	.005"	N/A	L9	50 Ohms	N/A	+/- 10%

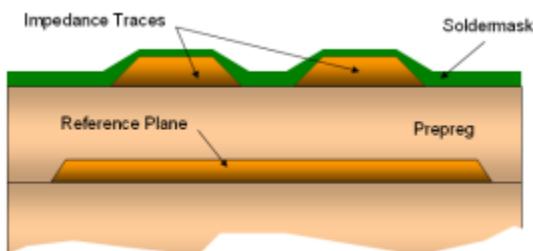
## 17.1. IMPEDANCE STRUCTURES

Below are samples of common structures used for controlled impedance.

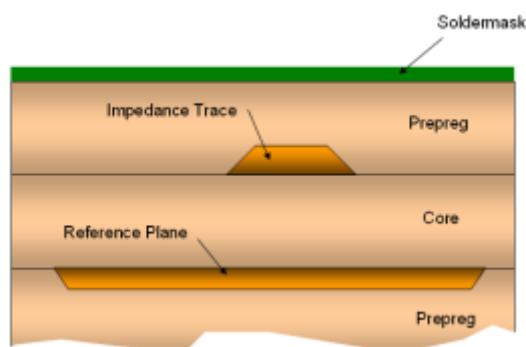
## 17.2. MICROSTRIP CONFIGURATION



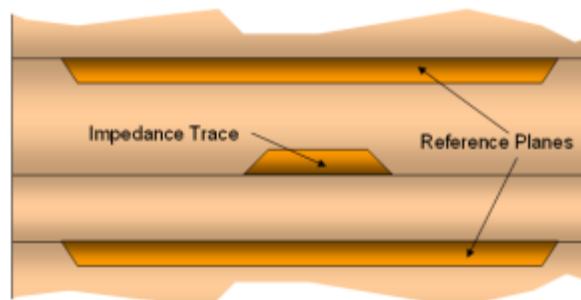
## 17.3. DIFFERENTIAL MICROSTRIP



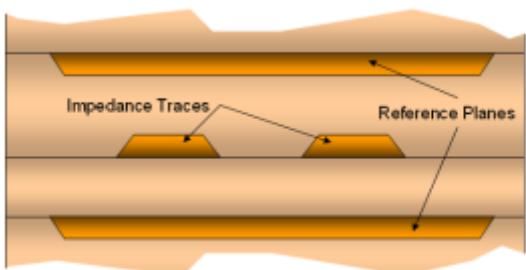
## 17.4. EMBEDDED MICROSTRIP



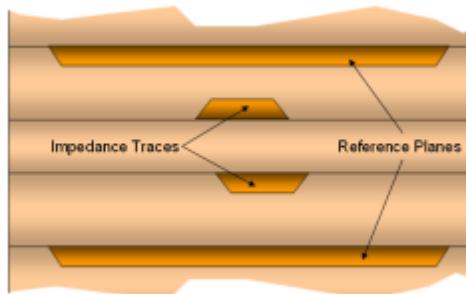
## 17.5. SINGLE STRIPLINE



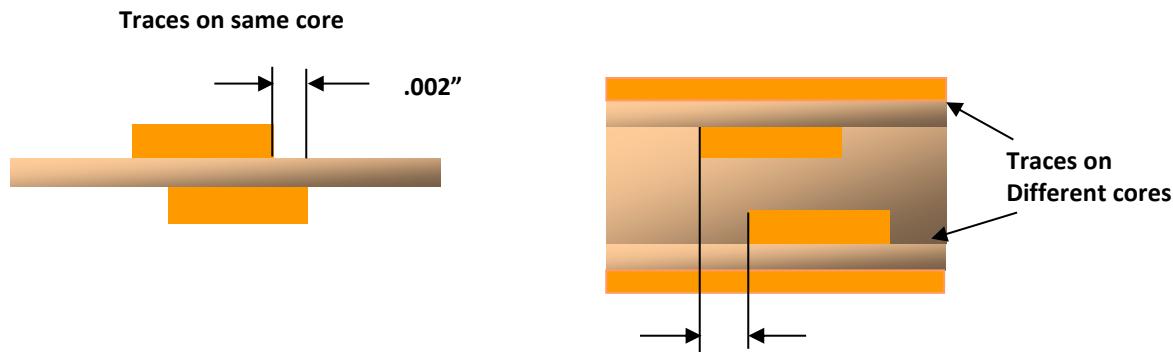
## 17.6. DIFFERENTIAL STRIPLINE (EDGE COUPLED)



## 17.7. DIFFERENTIAL STRIPLINE (BROADSIDE COUPLED)



## 17.8. BROADSIDE COUPLED IMPEDANCE EXAMPLES



The dielectric between the two signals becomes critical. Natural variation of this dielectric may create an imbalance in the differential impedance along the entire trace and in localized sections of the trace. In addition, layer to layer shift (variation in registration) may cause deviations in the differential impedance because of a change in the overlap between the circuits. This shift can be up to 2 mils if the broadside pairs are on the same core. This shift can be up to 3 mils if the broadside pairs are on different cores. Lastly, the natural variation in the trace widths on the two different layers of the broadside pair will cause a reduction in the overlap, causing high variation in the resulting impedance. If you intend on using broadside coupled pairs adhere to the following:

1. Use as WIDE a line as possible to cut down on the impedance variation caused by registration and etch process variation.
2. Place the reference planes on layers adjacent to the broadside pair traces.
3. Place the two layers of the pair are on the same core.  
This will help to reduce impedance variation caused by cumulative layer to layer and manufacturing tolerances.
4. Try to allow as wide an impedance tolerance as possible as a tight tolerance could reduce yields.

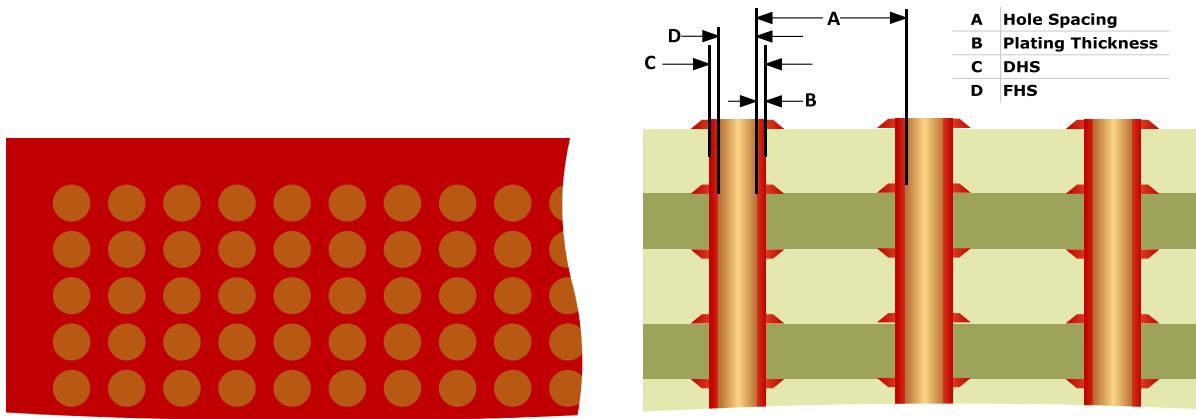
Multek uses time domain reflectometry, TDR, for testing impedance on PCB's. Testing is normally conducted from a coupon located on the production panel. The coupon is designed to reflect the same geometry of the PCB with respect to dielectric thickness, copper weights, and line widths, and configuration.

TDR reports are available and sent with all controlled impedance orders if requested.

## 18. THERMAL MANAGEMENT SOLUTIONS FOR HIGH POWER COMPONENTS

The key goal of thermal management is to provide a high thermal conductivity path from thermal sources to the ambient environment. If the mechanical design constraints allow for placement of a heat sink directly on the thermal source, this has highest thermal conductivity and is the recommended approach. If the mechanical design does not allow a heat sink to be placed directly on the component, heat can also be dissipated through to the opposite side of the PCB (z-axis) or in the XY plane of the PCB. Because of the larger distances in the XY direction as compared to the Z-axis, dissipating heat through the thickness of the PCB to a case or heat-sink on the opposite side of the PCB is preferred. In order to increase the z-axis thermal conductivity of a PCB, via farms (tightly packed via arrays) or coins (metal slugs embedded into the PCB) can be designed and manufactured in the PCB.

		Standard	Advanced
Hole Spacing (from drill to drill) (Dimension A)		0,35mm (min)	0,25mm (min)
Plating thickness in vias (Dimension B)	Std board	0,020mm (min)	0,035mm (min)
	Hybrid material	0,020mm (min)	0,025mm (min)
Drill size with tolerance (Dimension C)	Board thks <1,0mm	0,30mm (+/-0,025mm)	0,25mm (+/-0,025mm)
	1,0mm<=Board thks<2,0mm	0,35mm (+/-0,025mm)	0,30mm (+/-0,025mm)
	2,0mm<=Board thks<2,5mm	0,40mm (+/-0,025mm)	0,35mm (+/-0,025mm)
Finished hole diameter with tolerance (Dimension D)		(D-0,05mm) (+0/-0,10mm)	(D-0,05mm) (+0/-0,075mm)
Plugged via size (Dimension C)	by VCP (applicable for PCB with 2 sides assembly)	<=0,6mm	
	by screen print (applicable for PCB with 1 side assembly)	0,3mm, 0,35mm (Recommended), 0,40mm	
Only one via size?	by VCP	No, can design different via size for plugging in one PCB	
	by screen print	No, can design 2 via sizes for plugging in one PCB, size difference between the 2 vias should be <=0,05mm	
Limit the number of filled and over plated vias		No	
Selective over plating		Yes (By D/F tenting)	



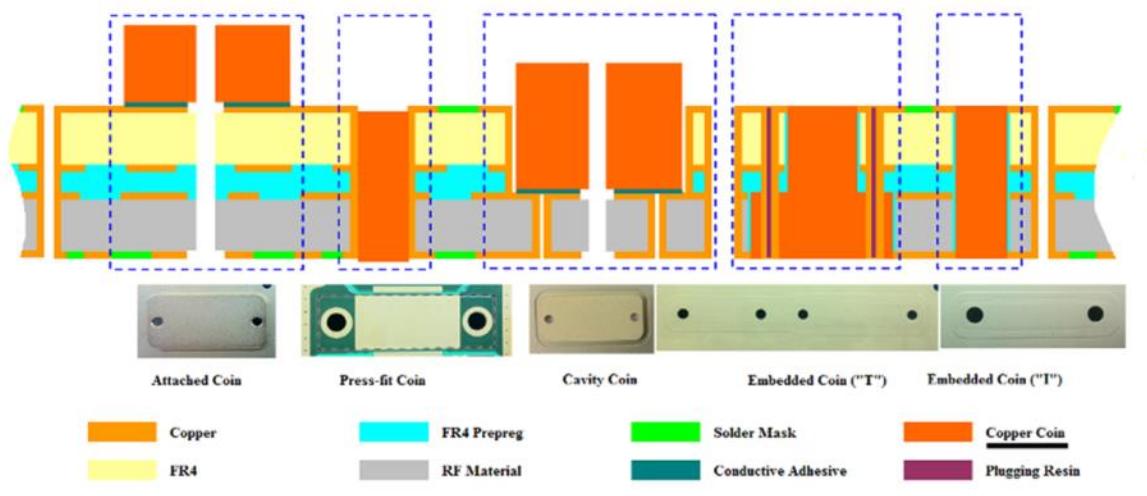
## 19. THERMAL MANAGEMENT OF HIGH POWER NETS

In the case of high-current nets, we advise designers to increase the cross-sectional area of these nets as much as possible by increasing the copper thickness and width of the layer. Please see IPC-2221A Appendix B for more information regarding recommended current handling capabilities of nets. In addition, thermal vias to the impacted area can be used to increase thermal conductivity to the remainder of the board.

## 20. COIN TECHNOLOGY

Coin technology is the embedding or attaching of a metal slug or coin to the PCB for thermal dissipation. There are multiple methods for this technology and the primary focus is to provide a higher than average metal volume to help pull heat from a solder device utilizing the PCB surface and internal plane layers along with other contact areas to dissipate heat from high thermal devices, such as RF amplifiers. It is common for Thermal Coin Management processes to utilize RF Materials and/or specialty Hybrid constructions. Coin technology builds with have additional tooling steps and NRE cost to cover the required tools, jigs and templates used for this process.

Multek offers five methods of Coin Technology; Attached Coin, Press-Fit Coin, Cavity Coin, Embedded "T" Coin and Embedded "I" Coin. These types of technology have unique requirements. We encourage the designer to contact your local FAE early in the design stage to assist in developing the optimal solution.

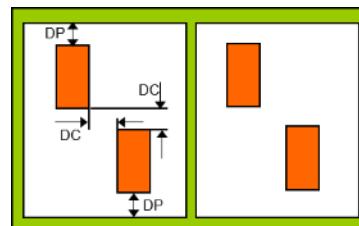
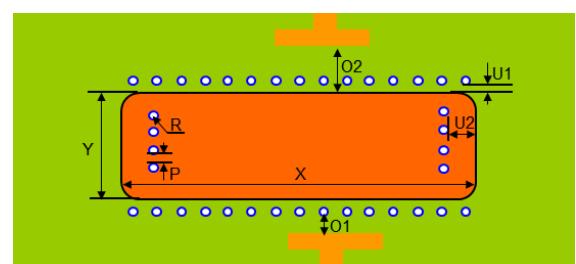
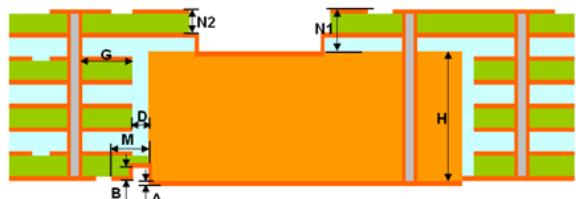


## 20.1. ATTACHED COIN DESIGN GUIDELINES

Attached Coin technology will follow standard PCB Fab Guidelines with a post fabrication process of attaching a metal coin or pallet to the surface of the board with a conductive adhesive material.

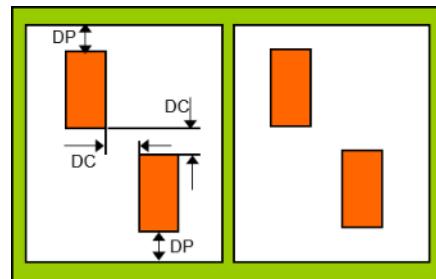
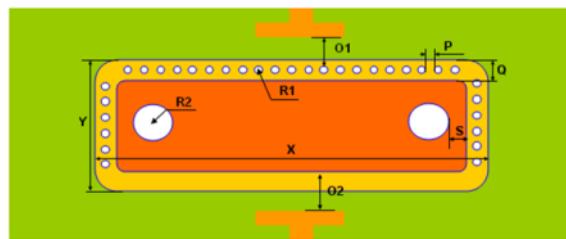
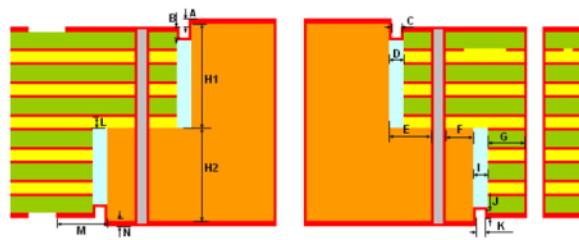
## 20.2. FULLY EMBEDDED COIN DESIGN GUIDELINES

Mark	Description	Requirement / mm
A	Coin depression	+/- 0.03
B	Gap	< 0.02
D	Boundary between coin and laminate	0.15
G	Cavity edge to hole wall	> 0.53
H	Coin thickness	0.6 ~ 1.8
M	Pad	> 0.3
N1	Milling depth	> 0.2
N2	Milling depth (if need)	> 0.2
O1	Circuitry to thermal hole pad	>/= 0.125
O2	Circuitry to coin	0.4
P	On coin thermal hole wall spacing	> 0.8
R	On coin thermal hole size	>/= 0.8
U1	Thermal hole wall to coin distance	>/= G1+D
U2	On coin thermal hole wall to coin distance	>/= 1/2 R
X	Coin size	8~120
Y	Coin size	8~60
DC	Coin to coin	>/= 2*(H+N1)
DP	Coin to PCB edge	>/= 2*(H+N1)



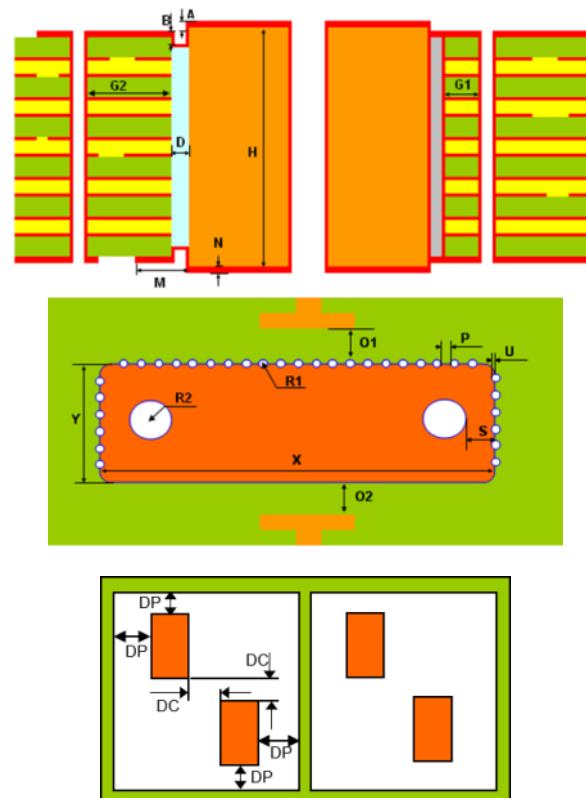
### 20.3. EMBEDDED "T" COIN DESIGN GUIDELINES

Mark	Description	Requirement / mm
A	Coin depression	+/- 0.03
B	Gap on top side	< 0.02
C	Gap on top side	< 0.02
D	Boundary between coin and laminate	< 0.15
E	Coin edge to hole wall	> 0.4
F	Coin edge to hole wall	> 0.3
G	Cavity edge to hole wall	> 0.53
H1	Coin top thickness	0.35 ~ 1.8
H2	Coin base thickness	0.35 ~ 0.6
I	Boundary between coin and laminate	< 0.15
J	Gap on bottom side	< 0.02
K	Gap on bottom side	< 0.02
L	Dielectric thickness	> 0.08
M	Pad	> 0.3
N	Coin protrusion	0 ~ 0.04
O1	Circuitry to thermal hole pad	>/= 0.125
O2	Circuitry to coin top side	0.4
P	Hole wall spacing	> 0.6
Q	Coin base width	> 1.5
R1	Hole size	0.4 ~ 0.8 (AR with coin base </= 1)
R2	Hole size	> 3.0
S	Hole wall to coin distance	> 1
X	Coin size	8 ~ 120
Y	Coin size	8 ~ 60
DC	Coin to coin	>/= 2*(H1+H2)
DP	Coin to PCB edge	>/= 2*(H1+H2)



## 20.4. EMBEDDED "I" COIN DESIGN GUIDELINES

Mark	Description	Requirement / mm
<b>A</b>	Coin depression	+/- 0.03
<b>B</b>	Gap	< 0.02
<b>D</b>	Boundary between coin and laminate	0.15
<b>G1</b>	Hole wall to hole wall	>0.38
<b>G2</b>	Cavity edge to hole wall	>0.53
<b>H</b>	Coin thickness	0.6~2.4
<b>M</b>	Pad	>0.3
<b>N</b>	Coin protrusion	0~0.04
<b>O1</b>	Circuitry to thermal hole pad	>/= 0.125
<b>O2</b>	Circuitry to coin	0.4
<b>P</b>	Hole wall spacing	>0.6
<b>R1</b>	Thermal hole size	0.6
<b>R2</b>	Assembly hole size	>3.0
<b>S</b>	Hole wall to coin distance	>2
<b>U</b>	Hole wall to coin distance	1/2 R1
<b>X</b>	Coin size	8~120
<b>Y</b>	Coin size	8~60
<b>DC</b>	Coin to coin	>/= 2*H
<b>DP</b>	Coin to PCB edge	>/= 2*H



## 21. ENGINEERING SERVICES

Multek offers a wide range of engineering services to meet our customer's ever-growing needs. These services provide Best-In-Class Customer Support, Technology Leadership, Supply Chain Optimization and Manufacturing Excellence. Along with the experienced Global Sales Staff, the Engineering Support teams are Key to achieving industry best customer satisfaction.

### 21.1. FIELD APPLICATION ENGINEERING SUPPORT (FAE)

Strategically located in key geographical areas, Multek provides Field Application Engineering support to work with customers on strategies to support both current and future design requirements. The Multek FAE team is the customer conduit to the factory.

Support functions Include:

- Technical Sales Support for the Multek Global Account Managers (GAM) and Business Development Managers (BDM) teams to address customer technology needs.
- Provide a conduit between manufacturing and customer during project development to ensure success
- Provide early preliminary Design Review to help optimize customer's designs for manufacturing with a focus on Produceability, Performance and Cost.
- Assist Customers as a technical resource in selection of design standards, material options, volume production capabilities and industry standard practices.

- Do full comprehensive Design Reviews and provide feedback to customers on product production readiness, meeting performance requirements with a focus on optimize the design for success in manufacturing.
- Assist as a communication liaison between the customer and manufacturing sites, within a customer's strategic geo locations. This enables Multek to provide critical engineering support with a focuses on culture, language and time zone to help eliminate excessive back and forth and time to delays in a global market.
- Communicate the customer current and future technology requirements to manufacturing, which assist in driving production technology to meet today's evolving market challenges.

## 21.2. MANUFACTURING ENGINEERING SUPPORT (ME)

The ME team, located at each fabrication facility is responsible for ensure the customer engineering efforts are supported directly at the facility. The ME team is responsible for all Tooling and Preproduction Analysis, Stack-up and material selections, communication with Production Control, Inside Sales and Process Engineering to ensure all key production attributes are met and work with customer on production ready product to ensure the highest level of quality and engineering support.

## 21.3. AMD LAB

Multek provides a wide service of analytical support for our customers. In line with that commitment is the state of the art AMD Lab on our China Campus. The AMD lab is one of the most advance labs within any PCB Fabrication facility in the world. This is why many of our top OEM customers have certified the AMD Lab to support their continued engineering efforts and provide reliable and state of the art support. This lab is geared to provide fast-response, high quality analytical services geared towards conducting

- Failure Analysis
- Reliability Testing
- Material and Emerging Technology Evaluation
- Process Characterization & Variation Reduction.

Equipment List	
Scanning Electron Microscopy	Liquid to Liquid Thermal Shock Chamber (LLTS)
EDX Microanalysis	Data Logger
Au/Pd Sputter Coating System	Temperature / Humidity Chambers
Carbon Coating System	Fast Temperature Change Rate Chamber (ATC)
FT-IR Microscopy	Digital Sampling Oscilloscope
X-Ray Inspection System	High Resistance Meters
SERA	High Resistance Decade Box
Wetting Balance	Precision LCR Meter
Analytical Balance	Data Acquisition / Switch Units
DSC, TMA, TGA, Rheometer	DC Power Supplies
Interconnect Stress Tester (IST)	Stereo Microscopes
Infra Red Thermal Imaging	Digital Camera
DC Power Supply	UV Microscope (Brightfield / Darkfield)
Load Frame	Brightfield Microscope
½" JDC Precision Sample Cutter	Diamond Saw
Vacuum Impregnation	Grinding and Polishing

Reflow Oven	Dynamic Bend Testers
Thermal Profiling System	Solder Pot

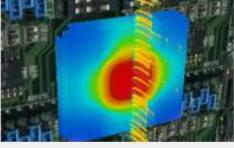
The AMD Lab is committed to being an important part of Multek's Corporate Quality Policy and strives in contributing to maintain Multek's position at the technological forefront of the PCB industry.

## 21.4. ADE GROUP

The Advance Development team within Multek is the Engineers working on the next generation process, equipment, materials and chemistry strategies at the factory level. New and emerging technologies that drive today's production advances are developed and implemented through the AED Group. Working side by side with the individual production facilities engineering teams, this group works to make the needs of tomorrow part of the offering for today.

## 21.5. INTERCONNECT TECHNOLOGY CENTER (ITC)

The Interconnect Technology Center (ITC) is a fully equipped Printed Circuit Analysis and Reliability Laboratory. ITC extends advance technology offerings to our customers by developing the Next Generation Printed Circuits Technology, Testing Methods and Designs. The ITC provides collaborative, analytical, reliability, failure and design analysis. The ITC will involve intense collaboration with our customers and many of the projects are shared resources of mutual benefit or as a fee basis service.

DESIGN & RAPID PROTOTYPING	ELECTRICAL TEST	ANALYTICAL LAB & ADVANCED MATERIALS	RELIABILITY, STANDARDS & FA	MODELING & SIMULATION
 A photograph showing a close-up of an orange flexible printed circuit board (FPC) being processed on a rapid prototyping machine.	 A photograph of a yellow electrical test fixture holding a component, likely a chip or package, used for automated testing.	 A photograph of a thermal analysis instrument, possibly a TGA or DMA, showing a sample being tested in a furnace-like chamber.	 A photograph of a cleanroom environment where technicians in white protective suits are working on a large piece of equipment, likely a reliability test chamber.	 A screenshot of a computer monitor displaying a 3D finite element model of a circuit board with heat flow or stress distribution visualized in red and blue colors.

**Design:** FPC, R-Flex, Rigid PCB, DFM  
**Proof of Concept**  
**Rapid Prototyping**  
Local, Advanced TTM

**Electrical Testing**  
Embedded Component, Continuity, Process Effects/ Materials Selection  
**Signal Integrity**  
VNA (S-parameter)  
TDR/TDT  
SET2DIL, SPP  
 $D_k$ ,  $D_f$ ,  $Z_0$   
PLTS De-Embedding

**Thermal Properties:**  
TGA, TMA, DMA  
**Cure/Flow Properties:**  
Rheometry, Viscosity, DSC, FTIR  
**Mechanical Properties:**  
Tensile, Bend, Fatigue  
**Optical Interconnects**

**Industry Standards:**  
JEDEC/IPC/ASTM  
**Reliability Testing**  
HAST/ TC/ TS/ MSL/ Reflow/ TTD/ Peel Strength/ CAF/ SIR/ Surface Roughness  
**Failure Analysis**  
SEM/EDX, CSAM, X-Section/ Optical Microscope

**Electrical/ Mechanical/ Thermal Simulation/ Modelling**  
Verification Testing, Test Vehicles  
**Optical Interconnects**  
**Signal Integrity**  
ADS  
Channel simulation  
3D Planar MOM  
EMPro  
3D FEM  
3D FDTD

## 22. NPI TO MASS PRODUCTION TRANSITION

During the NPI process done outside the Mass Production facility, it is critical to consider the key attributes of the production facility when designing or disposition DFM input from a prototype fabricator. Most companies that specialize in small prototype quantities do not consider the implication of high volume production to their process review. Below are key attributes to keep ensuring a smooth transition from Prototype to production.

## **22.1. IS THE DESIGN WITHIN THE PRODUCTION FACILITIES CAPACITIES**

Often production facilities will have much higher capacity lines that are often automated and developed for efficient throughput and cost. When designs are outside these production capabilities then special engineering efforts or production line configurations need to be made to ensure production compliance. By staying within production capabilities, you will be utilizing the most cost effective and reliable process. Often at small run prototype facilities, the production lines are not automated and in-line conveyorized systems. They can be easily altered and process changes can be done dynamically lot to lot panel to panel. Although the flexibility is good in development, it can be troublesome for production if it falls outside of the capabilities.

## **22.2. MATERIAL SELECTION**

Material option available at the prototype facility may be vast, but different geographies may have different material options. Keeping in mind the bulk cost of most production parts is the raw material planning for the production material selection should be done early in the design phase. Working to ensure the prototype is built on the production-targeted material is critical. This will ensure that the part is more representative of the finished production part and a large variable of material is selection does not result in production reliability or performance differences. Keep in mind that some materials available in Asia are not available in other regions of the world, and often glass and resin content for the same global material brand may be different based on the raw material suppliers manufacturing location and raw material resources in that region.

## **22.3. SURFACE FINISH**

Utilizing the production facilities desired surface finish would help determine both PCB Fab and Assembly process results to ensure robust manufacturing and the highest levels of quality of the finished product. Cost of surface finish in production is another key attribute in determining overall PCB cost, and should be considered early in the design phase.

## **22.4. YIELD OPTIMIZATION**

A common issue that arises when transitioning from prototype to production is related to the capabilities of building a product in proto, but not having the capabilities in production. Prototype manufacturing is engineering intensive with relation to cycle time and setup changes, due to small lot size. Most panel quantities are low and can be specialty processed through technically challenging manufacturing steps. Large yield loss in prototype will not be evident in the cost and cycle time model as in production. Materials to account for yield loss are not as high a cost value in prototype, labor is king. Production yield optimization will have a large impact on cost and every advantage is taken by production to make designs robust and high yielding.

## 23. MATERIAL CROSS REFERENCE

### 23.1. MULTEK'S PREFERRED MATERIAL OFFERING

Multek has a wide selection of materials to meet your PCB fabrication needs. Often we recommend materials that have historically been a high performing or cost competitive alternative. The below table is compiled to show the options available. Multek recommends that you contact your local FAE support to discuss material options, as they are dynamic to the market demand and growing electrical needs.

**23.1.1. PREFERRED MATERIAL TABLE**

Laminate Designation	Suppliers	B1	B3	B4	B5
Halogen Free Handheld & Commercial Product	EMC Panasonic TUC NanYa	EM285	EM285 EM370(5) 1566WN for ELIC TU-747 NPGN-150 non ELIC	EM285 TU-747	N / A
Halogen Free Multilayer	EMC TUC Hitachi	EM285	N/A	EM285 EM370(5) TU-747	EM370(D) TU-862HF MCL-E-75G
Halogen Free Multilayer Higher Tg	EMC TUC Hitachi	EM370(D)	MCL-E-75G EM370	TU-862HF EM370(D)	EM370(D) MCL-E-75G TU-862HF
Handheld & Commercial Product Normal Tg	Shengyi ITEQ TUC	S1000 IT158	S1000	S1000 TU-622 LE	N / A
Multilayer Normal Tg	TUC Shengyi ITEQ Hitachi	TU-622 LE	N / A	S1000 TU-622 LE IT158	185HR S1000 IT180i
Multilayer ≤ 26 Layers High Tg	Hitachi Shengyi ITEQ EMC	HR-02 S1000-2 IT180A	N / A	HR-02 S1000-2	185HR IT-180i HR-02

Laminate Designation	Suppliers	B1	B3	B4	B5
<b>Multilayer &gt;26 Layers High Tg</b>	Panasonic Isola	N/A	N/A	NA	R1755V 370HR
<b>Multilayer Mid Loss Df ≤ 0.015</b>	EMC TUC ITEQ	EM370(D)	N/A	TU-862HF EM370(D)	IT-180i EM370(D) TU-862HF
<b>Multilayer Low loss Df ≤ 0.01</b>	Hitachi TUC Panasonic EMC	HE-679G	N/A	TU-872LK Megtron 4	EM828 TU-863 TU-872LK HE-679G(S) - Sequential
<b>Multilayer Ultra Low Loss Df ≤ 0.006</b>	Panasonic Hitachi Rogers	Megtron 6	N/A	RO4350B	IT-150DA Megtron 6

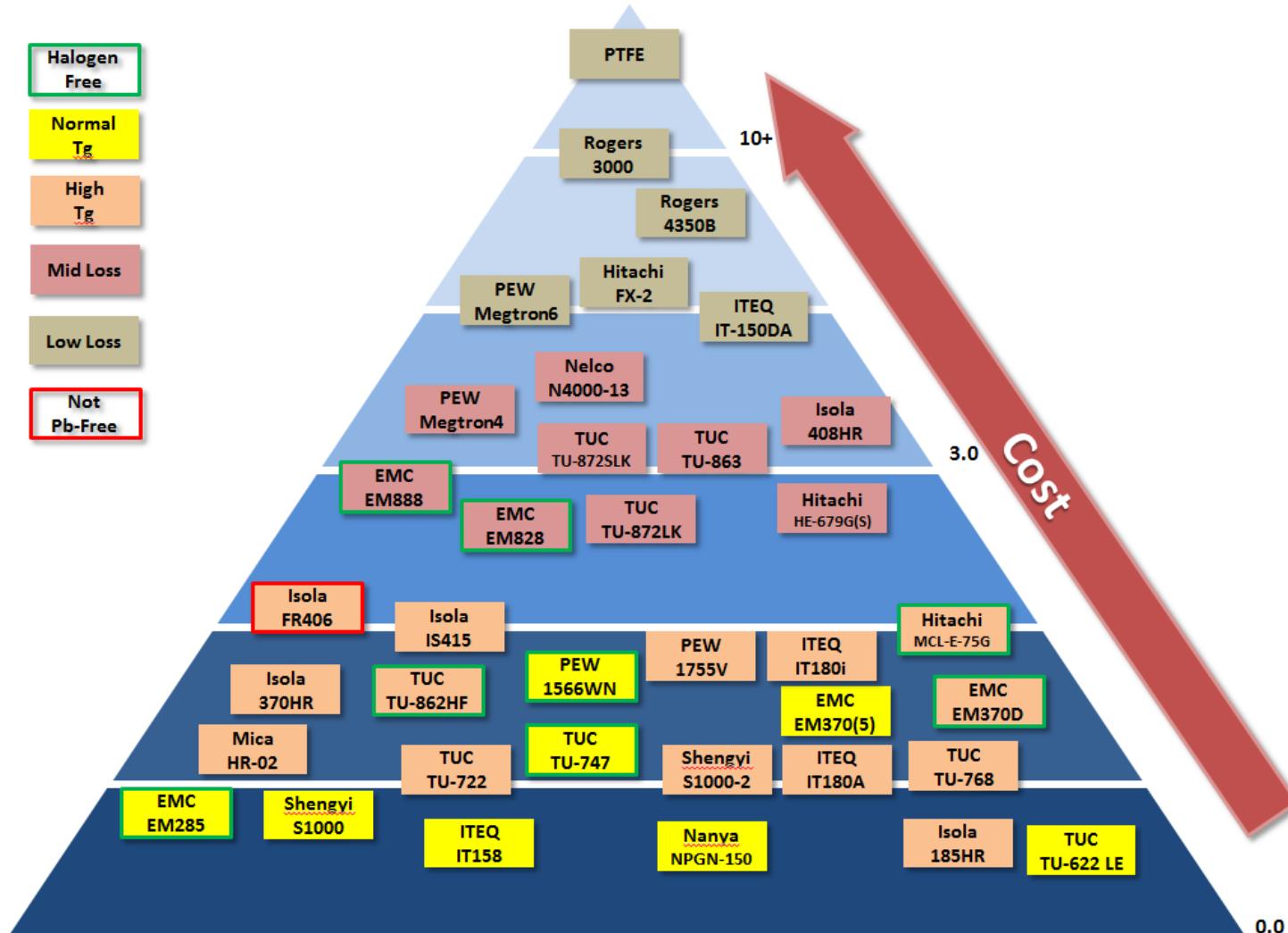
## 23.2. EXTENDED MATERIAL OFFERING

Multek offers materials outside our preferred list above. Please contact your FAE for a complete list of material offerings. The team will have access to data sheets and material cross reference documentation that may not publically available.

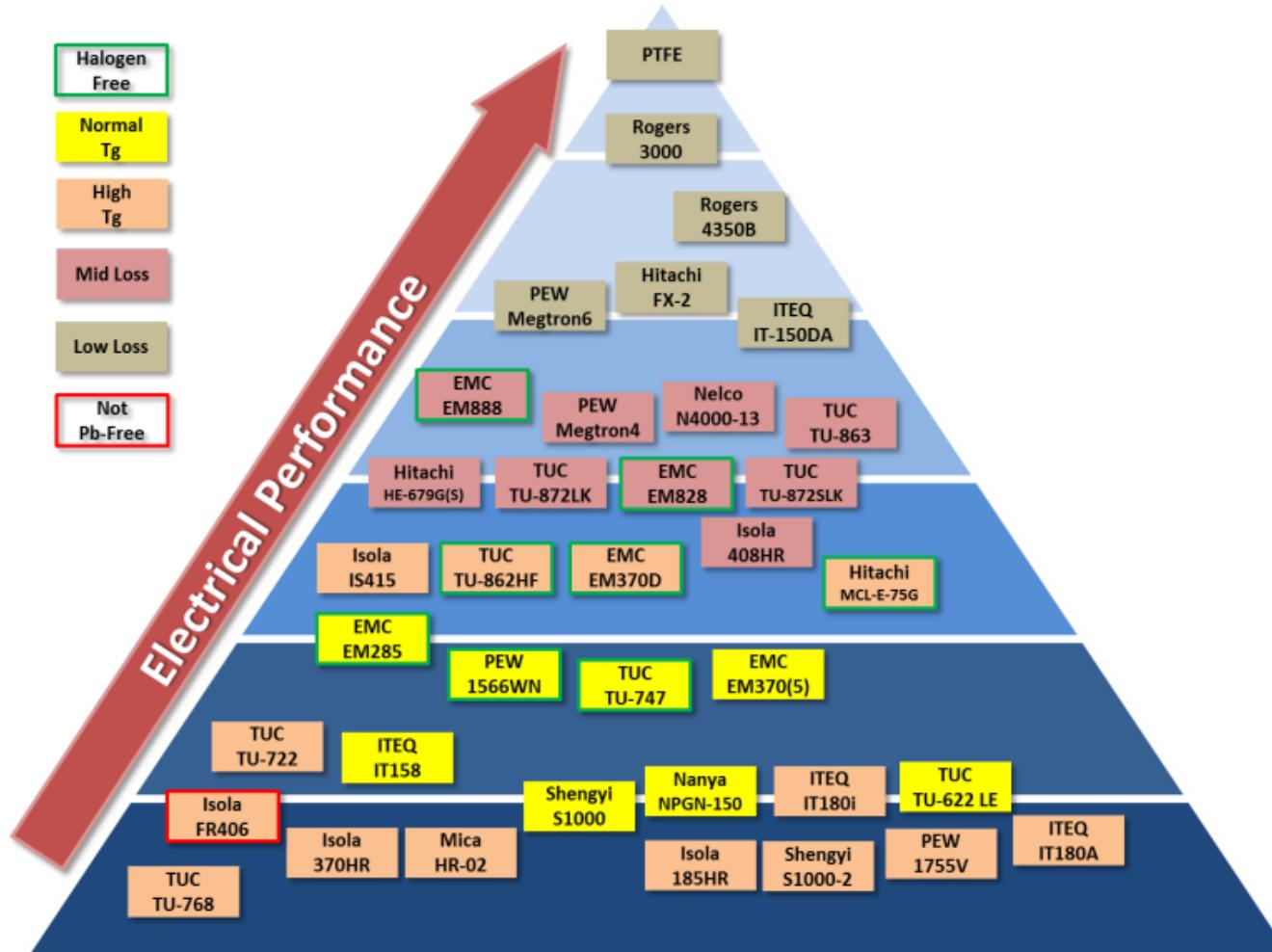
Your Sales support team can facilitate introductions to Material suppliers for more detailed discussions.

## 23.3. MATERIAL COST PYRAMID

### 23.3.1. COST PYRAMID



## 23.3.2. ELECTRICAL PERFORMANCE PYRAMID



## 23.4. MATERIAL REFERENCE SHEET

Multek FAE team can provide details information for all available material offerings. We would recommend visiting our website at [www.multek.com](http://www.multek.com) for additional reference documents.

## 24. FACILITIES CAPABILITIES SURVEY

Delivering PCB and FPC Solutions that enable our customer's success is Multek's Focus. Multek provides a Campus solution to meet the vast requirements of our customers PCB needs. Understanding that PCB Fabrication is a labor and equipment intensive process, Multek has focused our factories to have unique capabilities that offer the right equipment and technical staff to meet our customers diverse technology needs. The right facility building the right PCB helps control cost and ensure the highest level of quality to our customers.

### 24.1. MULTEK B1 CAPABILITIES

- Multilayer Production
- Thermal Manage Capabilities both Embedded and Attached Coin
- BBV & Sequential Lam
- HDI Capabilities / Solid Cu µVia Fill

		Multek Facility		Comments
		China B1		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	Comments
<b>Number of Conductive layers:</b>				
Standard 150 Tg Materials:	Layer Count Range	2-14	2-16	
High 170 Tg Materials:	Layer Count Range	2-14	2-16	
Mid Loss Materials (Df < 0.011):	Layer Count Range	2-14	2-16	
Low Loss Materials (Df < 0.007):	Layer Count Range	2-14	2-16	
Roger 3000 Series Materials (Hybrid):	Layer Count Range	N/A	2-6	
Roger 4000 Series Materials:	Layer Count Range	2-6	4-12	
PTFE materials:	Layer Count Range	N/A	2-6	
<b>Minimum Dielectric Thickness (Core):</b>				
Standard 150 Tg Materials:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
High 170 Tg Materials:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Mid Loss Materials (Df < 0.011):	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Low Loss Materials (Df < 0.007):	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Roger 3000 Series Materials (Hybrid):	Inches (mm)	0.004	0.003	
Roger 4000 Series Materials:	Inches (mm)	0.0100 (0.254)	0.008 (0.203)	
PTFE materials:	Inches (mm)	0.020	0.012	
<b>Minimum Dielectric Thickness (B-Stage):</b>				
Standard 150 Tg Materials:	(Glass Type) Nominal prepress Thickness	(1080 prepreg) 0.0025	(106 prepreg) 0.0018	
High 170 Tg Materials:	(Glass Type) Nominal prepress Thickness	(1080 prepreg) 0.0025	(106 prepreg) 0.0018	
Mid Loss Materials (Df < 0.011):	(Glass Type) Nominal prepress Thickness	(1080 prepreg) 0.0025	(106 prepreg) 0.0018	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B1		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Low Loss Materials (Df < 0.007):	(Glass Type) Nominal prepress Thickness	(1080 prepreg) 0.0025	(106 prepreg) 0.0018	
Roger 3000 Series Materials (Hybrid):	Yes / No	N/A	N/A	
Roger 4000 Series Materials:	(Glass Type) Nominal prepress Thickness	(2x1080 prepreg) 0.0066	(1080 prepreg) 0.004	
PTFE materials:	Yes / No	NO	NO	
Buried Capacitance:	Yes / No	NO	NO	
Buried Resistance:	Yes / No	NO	NO	
<b>Production Panel Details</b>				
Panel Size:	Inches (mm)	18 X 24 (463 x 616)	12 X 18 (307 x 463)	
		21 x 24 (539 x 616)	14 x 16 (359 x 410)	
		16x21 (410x539)	16 X 18 (410 x 463)	
Non Usable Border on Panel:	Inches (mm)	0.7 (17.78)	0.6 (15.24)	
Spacing Between Boards:(Routing Process):	Inches (mm)	0.12 (3.048)	0.1 (2.54)	
<b>Lamination Process</b>				
Maximum Overall Thickness:	Inches (mm)	0.104 (2.642)	0.1181 (3.0)	
Minimum Overall Thickness	Inches (mm)	0.016 (0.406)	0.012 (0.305)	
Flatness:(Inch/Inch):	Inches (mm)	0.010 (0.254)	0.007 (0.178)	
Overall Board Thickness Tolerance < 0.020":	+/- Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Overall Board Thickness Tolerance ~0.031":	+/- Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Overall Board Thickness Tolerance ~0.062":	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Overall Board Thickness Tolerance ~0.093":	+/- Inches (mm)	0.009 (0.229)	0.007 (0.178)	
Overall Board Thickness Tolerance ~0.125":	+/- Inches (mm)	N/A	N/A	
Overall Board Thickness Tolerance ~0.187":	+/- Inches (mm)	N/A	N/A	
HDI Structure Maximum:	n+n+n	1+n+1	2+n+2	
Maximum ELIC Layer Count:	Layer Count	N/A	N/A	
Thinnest plated core with a mechanical via :	Inches (mm)	0.010 (0.254)	0.008 (0.203)	
Thinnest Laser µVia Drilled Core:	Inches (mm)	N/A	N/A	
Maximum Number of Lamination Cycles:	Count	2	3	
Minimum Core Thickness for Build-up standard HDI with Plating:	Inches (mm)	0.01 (0.254)	0.08 (2.032)	
Minimum Core Thickness for ELIC with Solid Cu Via Plating:	Inches (mm)	N/A	N/A	
Maximum Core Thickness for ELIC with Solid Cu Via Plating:	Inches (mm)	N/A	N/A	
Maximum Dielectric Thickness for standard plated µVia:	Inches (mm)	0.003 (0.076)	0.004 (0.102)	
Maximum Dielectric Thickness for Solid Cu µVia	Inches (mm)	N/A	N/A	
<b>Circuit Etching</b>				
Minimum Conductor Width				

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

Description	Unit	Multek Facility		Comments
		High Volume Mass Production Capable	Advanced Capable Production	
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.003 (0.076)	0.003 (0.076)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Internal Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight ½ oz.:	Inches (mm)	0.003 (0.076)	0.003 (0.076)	
External Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
External Starting Copper Weight 2 oz.:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
External Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
External VIPPO Starting Copper Weight 1 oz.:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
External Cu μVia Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
External Epoxy μVia and Thru Hole Fill Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	
<b>Conductor Width Tolerance</b>				
Internal Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0007 (0.018)	
Internal Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
Internal Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.0015 (0.038)	0.0012 (0.03)	
Internal Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
External Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0007 (0.018)	
External Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
External Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.0015 (0.038)	0.0012 (0.03)	
External Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
External VIPPO Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.0015 (0.038)	0.0012 (0.03)	
External Cu μVia Fill Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0015 (0.038)	0.0012 (0.03)	
External Epoxy μVia and Thru Hole Fill Starting Copper Weight ½ oz.:	+/- Inches (mm)	N/A	N/A	
<b>Minimum Conductor Spacing (Airgap)</b>				
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.003 (0.076)	0.003 (0.076)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.006 (0.152)	0.006 (0.152)	
Internal Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight ½ oz.:	Inches (mm)	0.003 (0.076)	0.003 (0.076)	
External Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
External Starting Copper Weight 2 oz.:	Inches (mm)	0.006 (0.152)	0.006 (0.152)	
External Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
External VIPPO Starting Copper Weight 1 oz.:	Inches (mm)	0.006 (0.152)	0.006 (0.152)	
External Cu μVia Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	Inches (mm)	0.006 (0.152)	0.006 (0.152)	
External Epoxy μVia and Thru Hole Fill Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

Description	Unit	Multek Facility		Comments
		China B1		
<b>Spacing Tolerance</b>		<b>High Volume Mass Production Capable</b>	<b>Advanced Capable Production</b>	
Internal Starting Copper Weight $\frac{1}{2}$ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0007 (0.018)	
Internal Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
Internal Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.0015 (0.038)	0.0012 (0.03)	
Internal Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
External Starting Copper Weight $\frac{1}{2}$ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0007 (0.018)	
External Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
External Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.0015 (0.038)	0.0012 (0.03)	
External Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
<b>Trace Crest To Base Difference</b>				
Internal Starting Copper Weight $\frac{1}{2}$ oz.:	Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.0012 (0.03)	0.001 (0.025)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.002 (0.051)	0.0015 (0.038)	
External Starting Copper Weight $\frac{1}{2}$ oz.:	Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
External Starting Copper Weight 1 oz.:	Inches (mm)	0.0012 (0.03)	0.001 (0.025)	
External Starting Copper Weight 2 oz.:	Inches (mm)	0.002 (0.051)	0.0015 (0.038)	
Minimum Hole to copper feature (Via to adjacent trace):	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Minimum Copper to Edge of Board Spacing Internal:	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Minimum Copper to Edge of Board Spacing External:	Inches (mm)	0.008 (0.203)	0.007 (0.178)	
Internal Plane to Edge of board spacing:	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Minimum Etched Nomenclature Starting Copper Weight $\frac{1}{2}$ oz.:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Minimum Etched Nomenclature Starting Copper Weight 1 oz.:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Minimum Etched Nomenclature Starting Copper Weight 2 oz.:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	
Maximum Copper thickness per Inner Layer Core:	Oz.	1.0	2.0	
Maximum Copper thickness per Outer Layer Plated Surface:	Oz.	1.0	2.0	
<b>Via and Hole Drilling:</b>				
<b>Laser Drilling</b>				
Laser Drilling Capabilities:	Yes / No	YES		
Smallest Laser DHS:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
$\mu$ Via Pad Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.008 (0.203)	0.006 (0.152)	
$\mu$ Via Anti-Pad/Clearance Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.018 (0.457)	0.016 (0.406)	
Feature Location Tolerance within entire pad stack to Master Drill Pattern: (Layer to Layer Tolerance .020 Thick 0.004 DHS HDI/ELIC Build-up 18 x 24 Panel)	Inches (mm)	0.003	0.076	0.002 (0.051)
<b>Mechanical Drilling</b>				
Mechanical Via Pad Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.012 (0.305)	0.01 (0.254)	
Mechanical Via Anti-Pad/Clearance Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.020 (0.508)	0.018 (0.457)	
Smallest DHS 0.062 Thick Board:	Inches (mm)	0.0118 (0.3)	0.0098 (0.249)	
Smallest DHS 0.093 Thick Board:	Inches (mm)	0.0138 (0.351)	0.0118 (0.3)	
Smallest DHS 0.125 Thick Board:	Inches (mm)	N/A	N/A	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B1		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Smallest DHS 0.150 Thick Board:	Inches (mm)	N/A	N/A	
Smallest DHS 0.187 Thick Board:	Inches (mm)	N/A	N/A	
Smallest Non Plated Hole Size:(Finished)	Inches (um)	0.012 (0.305)	0.010 (0.249)	For print & etch process only.
Largest Plated Hole Size Drilled:(Finished)	Inches (mm)	0.1969 (5.001)	N/A	For print & etch process only.
Largest Non-Plated Hole Size Drilled:	DHS + X Inches (mm)	N/A	N/A	Drill size to select according to nominal value of FHS with tolerance.
Largest Tented Non-Plated Hole:	Inches (mm)	0.16 (4.064)	0.2 (5.08)	For print & etch process only.
Standard Plated Hole Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Press-Fit Plated Hole Tolerance:	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Non-plated Hole Tolerance:	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Minimum NPTH to Edge of Board Spacing:	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Drilled Hole Location Tolerance to Datum Zero: ( True Position across 18 x 24 ):	+/- Inches (mm)	0.004 (0.102)	0.003 (0.076)	
2nd Drill Hole Location Tolerance to Datum Zero: ( True Position across 18 x 24 panel )	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Front to Back Feature Location Tolerance: (Top to Bottom Tolerance Different Core 18 x 24 Panel)	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Front to Back Feature Location Tolerance : (Top to Bottom Tolerance Same Core 18 x 24 Panel)	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Feature Location Tolerance within entire pad stack to Master Drill Pattern: (Layer to Layer Tolerance 0.093 Thick 0.0098 Mechanical DHS 18 x 24 Panel)	Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Minimum Copper Pull-Back from NPT Hole on External Layers:	Inches (mm)	0.020 (0.508)	0.018 (0.457)	NPTH edge to copper Min Space: 10 mils standard.
Minimum Clearance from Internal Conductor to Non Plated Hole:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	NPTH edge to copper Min Space: 10 mils standard.
Minimum Clearance from External Conductor to Non Plated Hole:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	NPTH edge to copper Min Space: 10 mils standard.
Minimum Drilled Slot Width:	Inches (mm)	0.032 (0.8)	0.0157 (0.399)	Slot drill bit is limited to 0.4-2.0mm.
Minimum Drilled Slot Length to Width Ratio (Length: Width):	Ratio	2.5:1	2:1	
<b>Via In Pad Plated Over (VIPPO)</b>				
VIPPO Capability:	Yes / No	YES	YES	
VIPPO with filled µVia Capability:	Yes / No	YES	YES	
Smallest Epoxy Filled Drilled Hole Size:	Inches (mm)	0.008 (0.203)	0.008 (0.203)	
Largest Epoxy Filled Drilled Hole Size: ( 2 mil dimpling allowed )	Inches (mm)	0.022 (0.559)	0.024 (0.61)	
Largest gap in DHS with Epoxy Filled Holes: (without Dimpling > 2.0 mils)	Inches (mm)	0.004 (0.102)	0.006 (0.152)	
Smallest Epoxy Filled µVia Size:	Inches (mm)	0.005 (0.127)	0.0045 (0.114)	
<b>Mechanical Blind and Buried Via</b>				
Mechanical Blind Via Capabilities:	Yes / No	YES	YES	
Minimum Blind Mechanical DHS:	Inches (mm)	0.010 (0.254)	0.010 (0.254)	
Control Depth Blind Via Capability:	Yes / No	YES	YES	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B1		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Control Depth Drilling Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Mechanical Buried Via Capabilities:	Yes / No	YES	YES	
Minimum Buried Via DHS:	Inches (mm)	0.008 (0.203)	0.008 (0.203)	
<b>Back-Drilling</b>				
Back-Drilling Capability:	Yes / No	YES	YES	
Depth Control Distance:	Inches (mm)	0.004	0.003 (0.076)	
Back-Drilling Depth Tolerance:	+/- Inches (mm)	0.003	0.002	
<b>Copper Plating</b>				
DC Plating Capabilities:	Yes / No	YES	YES	
Pulse Plating Capabilities:	Yes / No	YES	YES	
Solid Copper $\mu$ Via Fill:	Yes / No	YES	YES	
Solid Copper Thru Hole Fill:	Yes / No	No	No	
Copper Only Aspect Ratio:	Thkns to DHS	8:1	9:1	Assume this is for Thru hole Aspect Ratio
$\mu$ Via Laser Drill Aspect Ratio:	Thkns to DHS	0.75:1	0.85:1	
Plated Board Edges Capability:	Yes / No	YES	YES	
Plated Internal Slots & Cut-outs Capability:	Yes / No	YES	YES	
Plated Milled Control Depth Milling:	Yes / No	YES	YES	
Plated C-Bore / C-Sink Holes:	Yes / No	YES	YES	
<b>Solder Mask</b>				
Solder Mask Types:	Types	Liquid Photo Imageable (LPI)	Liquid Photo Imageable (LPI)	
Solder Mask Colors	Colors	Green	Blue	
Minimum Solder Mask Clearance: (LPI - Liquid Photo Imageable):	Inches (mm)	0.003 (0.076)	0.002 (0.051)	Per Side
Pad size larger than NPTH:	Inches (mm)	0.01 (0.254)	0.006 (0.152)	Assume Pad Size here refer to S/M Opening
Over Surface Image:	Inches (mm)	0.003 (0.076)	0.002 (0.051)	Assume here refers to SMD Pad design & base material exposed is not allowed.
Web Between Surface Mount Pads:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	Assume Green or Blue S/M
Solder Mask Thickness Over Metal:	Inches (mm)	IPC Spec Coverage	0.0004 (0.01)	Assume this is refer to minimum S/M thickness over conductor
Clearance over Via diameter:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Pealable Mask Capability:	Yes / No	YES	YES	
Pealable Mask Registration:	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Pealable Mask Overhang:	Inches (mm)	0.025 (0.635)	0.02 (0.508)	
<b>Silk Screen / Legend Printing</b>				
Minimum Width Silk Screen Image:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Minimum spacing between Silk Screen Image:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Silk Screen Color Offering:	Colors	White	Yellow, Black	
<b>Mechanical Milling</b>				
Standard Router Bit Diameter:	Inches (mm)	.063 & (.16 & .079 2.0)	0.04 (1.016)	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B1		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Routed Profile Tolerance:(18"X 24" Panel)	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Routed Cutout Tolerance:(0.50" x 0.50")	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Minimum Internal Rout Radius:	Inches (mm)	0.032 (0.813)	0.02 (0.508)	
Minimum Routed Slot Diameter:	Inches (mm)	0.064 1.626	0.04 (1.016)	
Finger Tip Angle and Tolerance:	+/- Degree Inches	5°	4°	
Scoring Angles:	Degree	60° / 30° / 45°	25°	
Scoring Offset Tolerance:	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Scoring Remaining Web Thickness:	Inches (mm)	0.016 (0.406)	0.012 (0.305)	
Scoring Remaining Web Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Scoring True Position Tolerance:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Control Depth Routing Depth Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Counter Bore / Sink Depth Tolerance:	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Minimum routed slot width:	Inches (mm)	0.064 (1.626)	0.040 (1.016)	
<b>Testing</b>				
Minimum Test Continuity Resistance:	Ohms	20 Ohms	10 Ohms	
Maximum Test Voltage:	Volts	100V	250V	
Maximum Test Isolated Resistance:	Ohms	10m Ohms	50m Ohms	
Largest Test Bed Fixture:	Inches (mm)	19.2" X 19.2"		
Largest Test Bed Flying Probe:	Inches (mm)	18" X 24"		
Electrical Test Pitch for Flying Probe:	Inches (mm)	0.01 (0.254)	0.004 (0.102)	
Electrical Test Pitch for Fixture Test:	Inches (mm)	0.0256 (0.65)	0.02 (0.508)	
TDR Test Tolerance Single Ended 50-75 Ohms:	+/- tolerance	+/- 10%*	+/- 7.5%*	Design related
TDR Test Tolerance Single Ended > 75 Ohms:	+/- tolerance	+/- 10%*	+/- 7.5%*	Design related
TDR Test Tolerance Differential Pair < 101 Ohms:	+/- tolerance	+/- 10%*	+/- 7.5%*	Design related
TDR Test Tolerance Differential Pair > 100 Ohms:	+/- tolerance	+/- 10%*	+/- 7.5%*	Design related
High Pot Test Voltage:(AC or DC):		500 V	As Requested	
4 Wire Testing Capability:	Yes / No	YES	YES	
LD Testing Capability:	Yes / No	No	No	
SET2DIL Testing Capability:	Yes / No	No	No	
<b>Surface Finish</b>				
Organic Solder Preservative (OSP) Capability:	Yes / No	YES	YES	
Immersion Gold (ENIG) Capability:	Yes / No	YES	YES	
Immersion Silver (Ag) Capability:	Yes / No	YES	YES	
Electrolytic Hard Gold Capability:	Yes / No	YES	YES	
Thick Soft Gold Capability:	Yes / No	YES	YES	
Immersion Tin (Sn) Capability:	Yes / No	YES	YES	
Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) Capability:	Yes / No	YES*	YES*	Subcontract only
Lead Free Hot Air Solder Level (Pb-Free HASL) Capability:	Yes / No	NO	NO	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

Description	Unit	Multek Facility		Comments
		High Volume Mass Production Capable	Advanced Capable Production	
Aspect Ratio for OSP:	DHS : Overall Thickness	8:1	8.5:1	
Aspect Ratio for ENIG:	DHS : Overall Thickness	8:1	8.5:1	
Aspect Ratio for Immersion Ag:	DHS : Overall Thickness	8:1	8.5:1	
Aspect Ratio for Electrolytic Hard Gold:	DHS : Overall Thickness	5:1	5.5:1	
Aspect Ratio for Selective Thick Gold:	DHS : Overall Thickness	5:1	5.5:1	
Aspect Ratio for Immersion Sn:	DHS : Overall Thickness	8:1	8.5:1	
Aspect Ratio for ENEPIG:	DHS : Overall Thickness	TBA	TBA	Subcontract only
Aspect Ratio for Pb-Free HASL:	DHS : Overall Thickness	NO	NO	
Recommended Plating Thickness for OSP:	Inches (mm)	0.2 - 0.6um	0.2 - 0.6um	
Recommended Plating Thickness for ENIG:	Inches (mm)	Ni: 3-8um / Au: 0.03um min	Ni: 3-8um / Au: 0.03um min	
Recommended Plating Thickness for Immersion Ag:	Inches (mm)	0.15 - 0.3um	0.15 - 0.3um	
Recommended Plating Thickness for Electrolytic Hard Gold:	Inches (mm)	Ni: 5-15um/Au: 0.76um, 1.0um or 1.27um	Ni: 5-15um/Au: 0.76um, 1.0um or 1.27um	
Recommended Plating Thickness for Selective Thick Gold:	Inches (mm)	Ni: 5-15um/Au: 0.76um, 1.0um or 1.27um	Ni: 5-15um/Au: 0.76um, 1.0um or 1.27um	
Recommended Plating Thickness for Immersion Sn:	Inches (mm)	0.8um Min.	0.8um Min.	
Recommended Thickness (ENEPIG):	Inches (mm)	TBA	TBA	
Recommended Thickness for Pb-Free HASL:	Inches (mm)	NO	NO	

## 24.2. MULTEK B2 CAPABILITIES

- Multilayer FPC
- Rigid-Flex PCB
- 1 mil Thin Core
- FPC Assembly and SMT

*Due to the unique capabilities and requirements for Flexible and Rigid Flex Circuits, the Capabilities are contained in the Flexible Circuit Design Guidelines. Please contact your Sales or Technical Support contact for a copy of this document.*

## 24.3. MULTEK B3 CAPABILITIES

- Commercial HDI
- Solid Cu Via Fill
- ELIC / HDI
- Ultra-Fine Pitch
- Ultra-Fine Line and Space

Description	Unit	Multek Facility		Comments
		High Volume Mass Production Capable	Advanced Capable Production	
<b>Number of Conductive layers:</b>				
Standard 150 Tg Materials:	Layer Count Range	4-12	4-14	
High 170 Tg Materials:	Layer Count Range	4-12	4-14	
Mid Loss Materials (Df < 0.011):	Layer Count Range	N/A	N/A	
Low Loss Materials (Df < 0.007):	Layer Count Range	N/A	N/A	
Roger 3000 Series Materials (Hybrid):	Layer Count Range	N/A	N/A	
Roger 4000 Series Materials:	Layer Count Range	N/A	N/A	
PTFE materials:	Layer Count Range	N/A	N/A	
<b>Minimum Dielectric Thickness (Core):</b>				
Standard 150 Tg Materials:	Inches (mm)	0.002 (0.051)	0.002 (0.041)	
High 170 Tg Materials:	Inches (mm)	0.002 (0.051)	0.002 (0.041)	
Mid Loss Materials (Df < 0.011):	Inches (mm)	N/A	N/A	
Low Loss Materials (Df < 0.007):	Inches (mm)	N/A	N/A	
Roger 3000 Series Materials (Hybrid):	Inches (mm)	N/A	N/A	
Roger 4000 Series Materials:	Inches (mm)	N/A	N/A	
PTFE materials:	Inches (mm)	N/A	N/A	
<b>Minimum Dielectric Thickness (B-Stage):</b>				
Standard 150 Tg Materials:	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.002	(1037 prepreg) 0.0016	
High 170 Tg Materials:	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.002	(1037 prepreg) 0.0016	
Mid Loss Materials (Df < 0.011):	(Glass Type) Nominal prepress Thickness	N/A	N/A	
Low Loss Materials (Df < 0.007):	(Glass Type) Nominal prepress Thickness	N/A	N/A	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B3		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Roger 3000 Series Materials (Hybrid):	Yes / No	N/A	N/A	
Roger 4000 Series Materials:	(Glass Type) Nominal prepress Thickness	N/A	N/A	
PTFE materials:	Yes / No	N/A	N/A	
Buried Capacitance:	Yes / No	N/A	N/A	
Buried Resistance:	Yes / No	N/A	N/A	
<b>Production Panel Details</b>				
Panel Size:	Inches (mm)	18 X 24 (463 x 616)		
		20 x 24 (508 x 616)		
		21 x 24 (539 x 616)		
Non Usable Border on Panel:	Inches (mm)	0.7 (17.78)	0.6 (15.24)	
Spacing Between Boards:(Routing Process):	Inches (mm)	0.079 (2.007)	0.063 (1.6)	
<b>Lamination Process</b>				
Maximum Overall Thickness:	Inches (mm)	0.047 (1.194)	0.059 (1.499)	
Minimum Overall Thickness	Inches (mm)	0.012 (0.305)	0.01 (0.254)	
Flatness:(Inch/Inch):	Inches (mm)	0.010 (0.254)	0.007 (0.178)	
Overall Board Thickness Tolerance < 0.020":	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Overall Board Thickness Tolerance ~0.031":	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Overall Board Thickness Tolerance ~0.062":	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	Only for 60mil board thickness below
Overall Board Thickness Tolerance ~0.093":	+/- Inches (mm)	N/A	N/A	
Overall Board Thickness Tolerance ~0.125":	+/- Inches (mm)	N/A	N/A	
Overall Board Thickness Tolerance ~0.187":	+/- Inches (mm)	N/A	N/A	
HDI Structure Maximum:	n+n+n	4+n+4	5+n+5	
Maximum ELIC Layer Count:	Layer Count	12	14	
Thinnest plated core with a mechanical via :	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Thinnest Laser µVia Drilled Core:	Inches (mm)	0.003 (0.064)	0.002	
Maximum Number of Lamination Cycles:	Count	5	6	
Minimum Core Thickness for Build-up standard HDI with Plating:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Minimum Core Thickness for ELIC with Solid Cu Via Plating:	Inches (mm)	0.0025	0.002	
Maximum Core Thickness for ELIC with Solid Cu Via Plating:	Inches (mm)	0.003	0.004	
Maximum Dielectric Thickness for standard plated µVia:	Inches (mm)	0.003 (0.076)	0.004 (0.102)	
Maximum Dielectric Thickness for Solid Cu µVia	Inches (mm)	0.003 (0.076)	0.004 (0.102)	
<b>Circuit Etching</b>				
Minimum Conductor Width				

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

Description	Unit	Multek Facility		Comments
		High Volume Mass Production Capable	Advanced Capable Production	
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.002 (0.051)	0.0016 (0.041)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	N/A	N/A	
Internal Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight ½ oz.:	Inches (mm)	0.002 (0.051)	0.0016 (0.041)	
External Starting Copper Weight 1 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight 2 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	No VIPPO for Commercial HDI Design
External VIPPO Starting Copper Weight 1 oz.:	Inches (mm)	N/A	N/A	No VIPPO for Commercial HDI Design
External Cu μVia Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
External Epoxy μVia and Thru Hole Fill Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	
<b>Conductor Width Tolerance</b>				
Internal Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
Internal Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
Internal Starting Copper Weight 2 oz.:	+/- Inches (mm)	N/A	N/A	
Internal Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
External Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
External Starting Copper Weight 1 oz.:	+/- Inches (mm)	N/A	N/A	
External Starting Copper Weight 2 oz.:	+/- Inches (mm)	N/A	N/A	
External Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	+/- Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight 1 oz.:	+/- Inches (mm)	N/A	N/A	
External Cu μVia Fill Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
External Epoxy μVia and Thru Hole Fill Starting Copper Weight ½ oz.:	+/- Inches (mm)	N/A	N/A	
<b>Minimum Conductor Spacing (Airgap)</b>				
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.002 (0.051)	0.0018 (0.046)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	N/A	N/A	
Internal Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight ½ oz.:	Inches (mm)	0.0025 (0.064)	0.002 (0.051)	
External Starting Copper Weight 1 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight 2 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight 1 oz.:	Inches (mm)	N/A	N/A	
External Cu μVia Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B3		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
External Epoxy µVia and Thru Hole Fill Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	
<b>Spacing Tolerance</b>				
Internal Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
Internal Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
Internal Starting Copper Weight 2 oz.:	+/- Inches (mm)	N/A	N/A	
Internal Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
External Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
External Starting Copper Weight 1 oz.:	+/- Inches (mm)	N/A	N/A	
External Starting Copper Weight 2 oz.:	+/- Inches (mm)	N/A	N/A	
External Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
<b>Trace Crest To Base Difference</b>				
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight ½ oz.:	Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
External Starting Copper Weight 1 oz.:	Inches (mm)	N/A	N/A	
External Starting Copper Weight 2 oz.:	Inches (mm)	N/A	N/A	
Minimum Hole to copper feature (Via to adjacent trace):	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Minimum Copper to Edge of Board Spacing Internal:	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Minimum Copper to Edge of Board Spacing External:	Inches (mm)	0.008 (0.203)	0.007 (0.178)	
Internal Plane to Edge of board spacing:	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Minimum Etched Nomenclature Starting Copper Weight ½ oz.:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Minimum Etched Nomenclature Starting Copper Weight 1 oz.:	Inches (mm)	N/A	N/A	
Minimum Etched Nomenclature Starting Copper Weight 2 oz.:	Inches (mm)	N/A	N/A	
Maximum Copper thickness per Inner Layer Core:	Oz.	1.0	N/A	
Maximum Copper thickness per Outer Layer Plated Surface:	Oz.	1.0	N/A	
<b>Via and Hole Drilling:</b>				
<b>Laser Drilling</b>				
Laser Drilling Capabilities:	Yes / No	YES		
Smallest Laser DHS:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
µVia Pad Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.005 (0.127)	0.004 (0.102)	
µVia Anti-Pad/Clearance Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.011 (0.279)	0.009 (0.229)	
Feature Location Tolerance within entire pad stack to Master Drill Pattern: (Layer to Layer Tolerance .020 Thick 0.004 DHS HDI/ELIC Build-up 18 x 24 Panel)	Inches (mm)	0.003 0.064	0.002 (0.051)	
<b>Mechanical Drilling</b>				
Mechanical Via Pad Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.010 (0.254)	0.008 (0.203)	
Mechanical Via Anti-Pad/Clearance Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.016 (0.406)	0.014 (0.356)	
Smallest DHS 0.062 Thick Board:	Inches (mm)	0.0118 (0.3)	0.0098 (0.249)	Only for 60mil board thickness below

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B3		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Smallest DHS 0.093 Thick Board:	Inches (mm)	N/A	N/A	
Smallest DHS 0.125 Thick Board:	Inches (mm)	N/A	N/A	
Smallest DHS 0.150 Thick Board:	Inches (mm)	N/A	N/A	
Smallest DHS 0.187 Thick Board:	Inches (mm)	N/A	N/A	
Smallest Non Plated Hole Size:(Finished)	Inches (um)	0.012 (0.305)	0.010 (0.249)	For print & etch process only.
Largest Plated Hole Size Drilled:(Finished)	Inches (mm)	0.16 (4.064)	0.200 (5.08)	For print & etch process only.
Largest Non-Plated Hole Size Drilled:	DHS + X Inches (mm)	N/A	N/A	Drill size to select according to nominal value of FHS with tolerance.
Largest Tented Non-Plated Hole:	Inches (mm)	0.16 (4.064)	0.2 (5.08)	For print & etch process only.
Standard Plated Hole Tolerance:	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Press-Fit Plated Hole Tolerance:	+/- Inches (mm)	N/A	N/A	No press-fit design in B3
Non-plated Hole Tolerance:	+/- Inches (mm)	0.002 (0.051)	0.0016 (0.041)	
Minimum NPTH to Edge of Board Spacing:	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Drilled Hole Location Tolerance to Datum Zero: ( True Position across 18 x 24 ):	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
2nd Drill Hole Location Tolerance to Datum Zero: ( True Position across 18 x 24 panel )	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Front to Back Feature Location Tolerance: (Top to Bottom Tolerance Different Core 18 x 24 Panel)	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Front to Back Feature Location Tolerance : (Top to Bottom Tolerance Same Core 18 x 24 Panel)	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Feature Location Tolerance within entire pad stack to Master Drill Pattern: (Layer to Layer Tolerance 0.093 Thick 0.0098 Mechanical DHS 18 x 24 Panel)	Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Minimum Copper Pull-Back from NPT Hole on External Layers:	Inches (mm)	0.020 (0.508)	0.018 (0.457)	NPTH edge to copper Min Space: 10 mils standard.
Minimum Clearance from Internal Conductor to Non Plated Hole:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	NPTH edge to copper Min Space: 10 mils standard.
Minimum Clearance from External Conductor to Non Plated Hole:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	NPTH edge to copper Min Space: 10 mils standard.
Minimum Drilled Slot Width:	Inches (mm)	0.032 (0.8)	0.0197 (0.5)	Slot drill bit is limited to 0.5-2.0mm.
Minimum Drilled Slot Length to Width Ratio (Length:Width):	Ratio	3:1	2.5:1	
<b>Via In Pad Plated Over (VIPPO)</b>				
VIPPO Capability:	Yes / No	N/A	N/A	
VIPPO with filled $\mu$ Via Capability:	Yes / No	N/A	N/A	
Smallest Epoxy Filled Drilled Hole Size:	Inches (mm)	N/A	N/A	
Largest Epoxy Filled Drilled Hole Size: ( 2 mil dimpling allowed )	Inches (mm)	N/A	N/A	
Largest gap in DHS with Epoxy Filled Holes: (without Dimpling > 2.0 mils)	Inches (mm)	N/A	N/A	
Smallest Epoxy Filled $\mu$ Via Size:	Inches (mm)	N/A	N/A	
<b>Mechanical Blind and Buried Via</b>				

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B3		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Mechanical Blind Via Capabilities:	Yes / No	N/A	N/A	
Minimum Blind Mechanical DHS:	Inches (mm)	N/A	N/A	
Control Depth Blind Via Capability:	Yes / No	N/A	N/A	
Control Depth Drilling Tolerance:	+/- Inches (mm)	N/A	N/A	
Mechanical Buried Via Capabilities:	Yes / No	YES	YES	
Minimum Buried Via DHS:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	
<b>Back-Drilling</b>				
Back-Drilling Capability:	Yes / No	N/A	N/A	
Depth Control Distance:	Inches (mm)	N/A	N/A	
Back-Drilling Depth Tolerance:	+/- Inches (mm)	N/A	N/A	
<b>Copper Plating</b>				
DC Plating Capabilities:	Yes / No	YES	YES	
Pulse Plating Capabilities:	Yes / No	No	No	
Solid Copper $\mu$ Via Fill:	Yes / No	YES	YES	
Solid Copper Thru Hole Fill:	Yes / No	YES	YES	
Copper Only Aspect Ratio:	Thkns to DHS	8:1	8:1	Thru hole Aspect Ratio
$\mu$ Via Laser Drill Aspect Ratio:	Thkns to DHS	0.7:1	0.7:1	
Plated Board Edges Capability:	Yes / No	YES	YES	
Plated Internal Slots & Cut-outs Capability:	Yes / No	YES	YES	
Plated Milled Control Depth Milling:	Yes / No	YES	YES	
Plated C-Bore / C-Sink Holes:	Yes / No	YES	YES	
<b>Solder Mask</b>				
Solder Mask Types:	Types	Liquid Photo Imageable (LPI)	Liquid Photo Imageable (LPI)	
Solder Mask Colors	Colors	Green	Blue	
Minimum Solder Mask Clearance: (LPI - Liquid Photo Imageable):	Inches (mm)	0.0024 (0.061)	0.002 (0.051)	Per Side
Pad size larger than NPTH:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	Pad Size here refer to S/M Opening
Over Surface Image:	Inches (mm)	0.002 (0.051)	0.0016 (0.041)	Refers to SMD Pad design & base material exposed is not allowed.
Web Between Surface Mount Pads:	Inches (mm)	0.0032 (0.081)	0.0028 (0.071)	Green or Blue Only ME Approval for other Colors
Solder Mask Thickness Over Metal:	Inches (mm)	IPC Spec Coverage	0.0004 (0.01)	Refer to minimum S/M thickness over conductor
Clearance over Via diameter:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Pealable Mask Capability:	Yes / No	N/A	N/A	
Pealable Mask Registration:	+/- Inches (mm)	N/A	N/A	
Pealable Mask Overhang:	Inches (mm)	N/A	N/A	
<b>Silk Screen / Legend Printing</b>				
Minimum Width Silk Screen Image:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Minimum spacing between Silk Screen Image:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B3		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	Comments
Silk Screen Color Offering:	Colors	White	Yellow, Black	
<b>Mechanical Milling</b>				
Standard Router Bit Diameter:	Inches (mm)	0.047 & (1.2 & 0.04 1.0)	0.032 (0.813)	
Routed Profile Tolerance:(18"X 24" Panel)	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Routed Cutout Tolerance:(0.50" x 0.50")	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Minimum Internal Rout Radius:	Inches (mm)	0.02 (0.508)	0.016 (0.406)	
Minimum Routed Slot Diameter:	Inches (mm)	0.04 1.016	0.032 (0.813)	
Finger Tip Angle and Tolerance:	+/- Degree Inches	10°	5°	
Scoring Angles:	Degree	60° / 30° / 45°	25°	
Scoring Offset Tolerance:	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Scoring Remaining Web Thickness:	Inches (mm)	0.016 (0.406)	0.012 (0.305)	
Scoring Remaining Web Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Scoring True Position Tolerance:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Control Depth Routing Depth Tolerance:	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Counter Bore / Sink Depth Tolerance:	+/- Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Minimum routed slot width:	Inches (mm)	0.064 (1.626)	0.040 (1.016)	
<b>Testing</b>				
Minimum Test Continuity Resistance:	Ohms	20 Ohms	10 Ohms	
Maximum Test Voltage:	Volts	100V	250V	
Maximum Test Isolated Resistance:	Ohms	20m Ohms	50m Ohms	
Largest Test Bed Fixture:	Inches (mm)	12"x10"	16"x12"	
Largest Test Bed Flying Probe:	Inches (mm)	16"x22"	18"x24"	
Electrical Test Pitch for Flying Probe:	Inches (mm)	0.01 (0.254)	0.004 (0.102)	
Electrical Test Pitch for Fixture Test:	Inches (mm)	0.0256 (0.65)	0.02 (0.508)	
TDR Test Tolerance Single Ended 50-75 Ohms:	+/- tolerance	+/- 10%*	+/- 7.5%*	Design related
TDR Test Tolerance Single Ended > 75 Ohms:	+/- tolerance	+/- 10%*	+/- 7.5%*	Design related
TDR Test Tolerance Differential Pair < 101 Ohms:	+/- tolerance	+/- 10%*	+/- 7.5%*	Design related
TDR Test Tolerance Differential Pair > 100 Ohms:	+/- tolerance	+/- 10%*	+/- 7.5%*	Design related
High Pot Test Voltage:(AC or DC):		500 V	As Requested	
4 Wire Testing Capability:	Yes / No	YES	YES	
LD Testing Capability:	Yes / No	No	No	
SET2DIL Testing Capability:	Yes / No	No	No	
<b>Surface Finish</b>				
Organic Solder Preservative (OSP) Capability:	Yes / No	YES	YES	
Immersion Gold (ENIG) Capability:	Yes / No	YES	YES	
Immersion Silver (Ag) Capability:	Yes / No	YES	YES	
Electrolytic Hard Gold Capability:	Yes / No	N/A	N/A	

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

Description	Unit	Multek Facility		Comments
		High Volume Mass Production Capable	Advanced Capable Production	
Thick Soft Gold Capability:	Yes / No	N/A	N/A	
Immersion Tin (Sn) Capability:	Yes / No	YES	YES	
Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) Capability:	Yes / No	YES*	YES*	Subcontract only
Lead Free Hot Air Solder Level (Pb-Free HASL) Capability:	Yes / No	NO	NO	
Aspect Ratio for OSP:	DHS : Overall Thickness	7.5:1	8.5:1	
Aspect Ratio for ENIG:	DHS : Overall Thickness	7.5:1	8.5:1	
Aspect Ratio for Immersion Ag:	DHS : Overall Thickness	7.5:1	8.5:1	
Aspect Ratio for Electrolytic Hard Gold:	DHS : Overall Thickness	N/A	N/A	
Aspect Ratio for Selective Thick Gold:	DHS : Overall Thickness	N/A	N/A	
Aspect Ratio for Immersion Sn:	DHS : Overall Thickness	7.5:1	8.5:1	
Aspect Ratio for ENEPIG:	DHS : Overall Thickness	TBA	TBA	Subcontract only
Aspect Ratio for Pb-Free HASL:	DHS : Overall Thickness	NO	NO	
Recommended Plating Thickness for OSP:	Inches (mm)	0.2 - 0.6um	0.2 - 0.6um	
Recommended Plating Thickness for ENIG:	Inches (mm)	Ni: 3-8um / Au: 0.03um min	Ni: 3-8um / Au: 0.03um min	
Recommended Plating Thickness for Immersion Ag:	Inches (mm)	0.15 - 0.3um	0.15 - 0.3um	
Recommended Plating Thickness for Electrolytic Hard Gold:	Inches (mm)	N/A	N/A	
Recommended Plating Thickness for Selective Thick Gold:	Inches (mm)	N/A	N/A	
Recommended Plating Thickness for Immersion Sn:	Inches (mm)	0.8um Min.	0.8um Min.	
Recommended Thickness (ENEPIG):	Inches (mm)	TBA	TBA	
Recommended Thickness for Pb-Free HASL:	Inches (mm)	NO	NO	

## 24.4. MULTEK B4 CAPABILITIES

- Multilayer Production
- HDI Capabilities / Solid Cu  $\mu$ Via Fill
- VIPPO
- BBV Sequential Lamination
- QTA Support

		Multek Facility		Comments
		China B4		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
<b>Number of Conductive layers:</b>				
Standard 150 Tg Materials:	Layer Count Range	1 – 12	14	
High 170 Tg Materials:	Layer Count Range	1 – 12	14	
Mid Loss Materials (Df < 0.011):	Layer Count Range	1 – 12	14	
Low Loss Materials (Df < 0.007):	Layer Count Range	1 – 12	14	
Roger 3000 Series Materials (Hybrid):	Layer Count Range	N/A	N/A	
Roger 4000 Series Materials:	Layer Count Range	1 – 12	14	
PTFE materials:	Layer Count Range	N/A	N/A	
<b>Minimum Dielectric Thickness (Core):</b>				
Standard 150 Tg Materials:	Inches (mm)	0.004 (0.102)		
High 170 Tg Materials:	Inches (mm)	0.004 (0.102)		
Mid Loss Materials (Df < 0.011):	Inches (mm)	0.004 (0.102)		
Low Loss Materials (Df < 0.007):	Inches (mm)	0.004 (0.102)		
Roger 3000 Series Materials (Hybrid):	Inches (mm)	N/A		
Roger 4000 Series Materials:	Inches (mm)	0.0066 (0.168)		
PTFE materials:	Inches (mm)	N/A		
<b>Minimum Dielectric Thickness (B-Stage):</b>				
Standard 150 Tg Materials:	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.002		
High 170 Tg Materials:	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.002		
Mid Loss Materials (Df < 0.011):	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.0022		
Low Loss Materials (Df < 0.007):	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.002		
Roger 3000 Series Materials (Hybrid):	Yes / No	N/A		
Roger 4000 Series Materials:	(Glass Type) Nominal prepress Thickness	(2x1080 prepreg) 0.008		
PTFE materials:	Yes / No	NO		
Buried Capacitance:	Yes / No	NO		

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B4		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Buried Resistance:	Yes / No	NO		
<b>Production Panel Details</b>				
Panel Size:	Inches (mm)	18.00 X 24.00 (457 x 610)	12.00 X 18.00 (305 x 457)	
		20.00 X 24.00 (508 x 610)	16.00 x 24.00 (406 x 610)	
		21.00 X 24.00 (533 x 610)	12.00 x 24.00 (305 x 610)	
		16.00 X 21.00 (406 x 533)	16.00 X 18.00 (406 x 457)	
		16.00 X 20.00 (406 x 508)		
Non Usable Border on Panel:	Inches (mm)	0.625 (15.875)	0.394 (10.008)	
Spacing Between Boards:(Routing Process):	Inches (mm)	0.1 (2.54)	0.08 (2.032)	
<b>Lamination Process</b>				
Maximum Overall Thickness:	Inches (mm)	0.110 (2.794)	0.126 (3.2)	Advance Capability for double sided boards only
Minimum Overall Thickness	Inches (mm)	0.016 (0.406)		
Flatness:(Inch/Inch):	Inches (mm)	0.010 (0.254)	0.007 (0.178)	
Overall Board Thickness Tolerance < 0.020":	+/- Inches (mm)	0.004 (0.102)		
Overall Board Thickness Tolerance ~0.031":	+/- Inches (mm)	0.004 (0.102)		
Overall Board Thickness Tolerance ~0.062":	+/- Inches (mm)	0.006 (0.152)		
Overall Board Thickness Tolerance ~0.093":	+/- Inches (mm)	0.009 (0.229)		
Overall Board Thickness Tolerance ~0.125":	+/- Inches (mm)	0.012 (0.305)		
Overall Board Thickness Tolerance ~0.187":	+/- Inches (mm)	N/A		
HDI Structure Maximum:	n+n+n	1+n+1	2+n+2	
Maximum ELIC Layer Count:	Layer Count	N/A		
Thinnest plated core with a mechanical via :	Inches (mm)	0.010 (0.254)	0.007 (0.178)	
Thinnest Laser µVia Drilled Core:	Inches (mm)	0.002 (0.051)		
Maximum Number of Lamination Cycles:	Count	2	3	
Minimum Core Thickness for Build-up standard HDI with Plating:	Inches (mm)	0.031 (0.787)		
Minimum Core Thickness for ELIC with Solid Cu Via Plating:	Inches (mm)	N/A	N/A	
Maximum Core Thickness for ELIC with Solid Cu Via Plating:	Inches (mm)	N/A	N/A	
Maximum Dielectric Thickness for standard plated µVia:	Inches (mm)	0.005 (0.127)		
Maximum Dielectric Thickness for Solid Cu µVia	Inches (mm)	0.003 (0.076)		
<b>Circuit Etching</b>				
<b>Minimum Conductor Width</b>				
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.003 (0.076)		
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)		
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.006 (0.152)		

# Multek Design Guidelines – Rigid PCB Fabrication

Last Updated on: 1/13/2014

		Multek Facility				
		China B4				
Description	Unit	High Volume Mass Production Capable		Advanced Capable Production		Comments
Internal Starting Copper Weight 3 oz.:	Inches (mm)	0.007	(0.178)			
External Starting Copper Weight ½ oz.:	Inches (mm)	0.004	(0.102)	0.003	(0.076)	Cu Hole Wall < 20um / Advance Capability upon ME review.
External Starting Copper Weight 1 oz.:	Inches (mm)	0.005	(0.127)			
External Starting Copper Weight 2 oz.:	Inches (mm)	0.007	(0.178)			
External Starting Copper Weight 3 oz.:	Inches (mm)	0.009	(0.229)			
External VIPPO Starting Copper Weight ½ oz.:	Inches (mm)	0.005	(0.127)	0.004	(0.102)	Cu Hole Wall < 20um / Advance Capability upon ME review.
External VIPPO Starting Copper Weight 1 oz.:	Inches (mm)	0.006	(0.152)			
External Cu μVia Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.005	(0.127)			ME Review Required
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	Inches (mm)	0.0055	(0.14)			ME Review Required
External Epoxy μVia and Thru Hole Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.0055	(0.14)			ME Review Required
<b>Conductor Width Tolerance</b>						
Internal Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0012	(0.03)	0.001	(0.025)	Advance Capability upon ME review.
Internal Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.0015	(0.038)			
Internal Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.002	(0.051)			
Internal Starting Copper Weight 3 oz.:	+/- Inches (mm)	0.003	(0.076)			
External Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0015	(0.038)	0.001	(0.025)	Advance Capability upon ME review.
External Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.002	(0.051)			
External Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.003	(0.076)			
External Starting Copper Weight 3 oz.:	+/- Inches (mm)	0.004	(0.102)			
External VIPPO Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0015	(0.038)			
External VIPPO Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.002	(0.051)			
External Cu μVia Fill Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0015	(0.038)			ME Review Required
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.002	(0.051)			ME Review Required
External Epoxy μVia and Thru Hole Fill Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0015	(0.038)			ME Review Required
<b>Minimum Conductor Spacing (Airgap)</b>						
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.0035	(0.089)	0.003	(0.076)	Advance Capability upon ME review.
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.004	(0.102)			
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.006	(0.152)			
Internal Starting Copper Weight 3 oz.:	Inches (mm)	0.007	(0.178)			
External Starting Copper Weight ½ oz.:	Inches (mm)	0.004	(0.102)			
External Starting Copper Weight 1 oz.:	Inches (mm)	0.005	(0.127)			
External Starting Copper Weight 2 oz.:	Inches (mm)	0.007	(0.178)			
External Starting Copper Weight 3 oz.:	Inches (mm)	0.009	(0.229)			

		Multek Facility		Comments
		China B4		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
External VIPPO Starting Copper Weight ½ oz.:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	Advance Capability upon ME review.
External VIPPO Starting Copper Weight 1 oz.:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	Advance Capability upon ME review.
External Cu μVia Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.005 (0.127)		ME Review Required
External Cu μVia Fill with Thru Hole Starting Copper Weight ½ oz.:	Inches (mm)	0.0055 (0.14)		ME Review Required
External Epoxy μVia and Thru Hole Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.0055 (0.14)		ME Review Required
<b>Spacing Tolerance</b>				
Internal Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0012 (0.03)	0.001 (0.025)	
Internal Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.0015 (0.038)		
Internal Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.002 (0.051)		
Internal Starting Copper Weight 3 oz.:	+/- Inches (mm)	0.003 (0.076)		
External Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0015 (0.038)	0.001 (0.025)	
External Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.002 (0.051)		
External Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.003 (0.076)		
External Starting Copper Weight 3 oz.:	+/- Inches (mm)	0.004 (0.102)		
<b>Trace Crest To Base Difference</b>				
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.0005 (0.013)		
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.001 (0.025)		
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.001 (0.025)		
External Starting Copper Weight ½ oz.:	Inches (mm)	0.001 (0.025)		
External Starting Copper Weight 1 oz.:	Inches (mm)	0.001 (0.025)		
External Starting Copper Weight 2 oz.:	Inches (mm)	0.002 (0.051)		
Minimum Hole to copper feature (Via to adjacent trace):	Inches (mm)	0.01 (0.254)		
Minimum Copper to Edge of Board Spacing Internal:	Inches (mm)	0.015 (0.381)		
Minimum Copper to Edge of Board Spacing External:	Inches (mm)	0.01 (0.254)		
Internal Plane to Edge of board spacing:	Inches (mm)	0.015 (0.381)		
Minimum Etched Nomenclature Starting Copper Weight ½ oz.:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Minimum Etched Nomenclature Starting Copper Weight 1 oz.:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Minimum Etched Nomenclature Starting Copper Weight 2 oz.:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	
Maximum Copper thickness per Inner Layer Core:	Oz.	4.0	5.0	
Maximum Copper thickness per Outer Layer Plated Surface:	Oz.	4.0	5.0	
<b>Via and Hole Drilling:</b>				
<b>Laser Drilling</b>				
Laser Drilling Capabilities:	Yes / No	YES		
Smallest Laser DHS:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
μVia Pad Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.009 (0.229)	0.008 (0.203)	
μVia Anti-Pad/Clearance Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.020 (0.508)		
Feature Location Tolerance within entire pad stack to Master	Inches (mm)	0.010 (0.250)		

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		Multek Facility		Comments
		China B4		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Drill Pattern: (Layer to Layer Tolerance .020 Thick 0.004 DHS HDI/ELIC Build-up 18 x 24 Panel)				
<b>Mechanical Drilling</b>				
Mechanical Via Pad Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.009 (0.229)	0.008 (0.203)	
Mechanical Via Anti-Pad/Clearance Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.020 (0.508)	0.018 (0.457)	
Smallest DHS 0.062 Thick Board:	Inches (mm)	0.0098 (0.249)		
Smallest DHS 0.093 Thick Board:	Inches (mm)	0.0138 (0.351)		
Smallest DHS 0.125 Thick Board:	Inches (mm)	0.016 (0.406)		
Smallest DHS 0.150 Thick Board:	Inches (mm)	N/A		
Smallest DHS 0.187 Thick Board:	Inches (mm)	N/A		
Smallest Non Plated Hole Size:(Finished)	Inches (um)	0.012 (0.305)	0.010 (0.249)	HASL Aspect ratio Limits. ME Review required for HASL
Largest Plated Hole Size Drilled:(Finished)	Inches (mm)	0.236 (5.994)		
Largest Non-Plated Hole Size Drilled:	DHS + X Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Largest Tented Non-Plated Hole:	Inches (mm)	0.236 (5.994)	0.275 (6.985)	Advance Capability upon ME review.
Standard Plated Hole Tolerance:	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Press-Fit Plated Hole Tolerance:	+/- Inches (mm)	0.002 (0.051)		
Non-plated Hole Tolerance:	+/- Inches (mm)	0.002 (0.051)	0.0015 (0.038)	
Minimum NPTH to Edge of Board Spacing:	Inches (mm)	0.007 (0.178)		
Drilled Hole Location Tolerance to Datum Zero: ( True Position across 18 x 24 ):	+/- Inches (mm)	0.003 (0.076)		Define hole as datum zero
2nd Drill Hole Location Tolerance to Datum Zero: ( True Position across 18 x 24panel )	+/- Inches (mm)	0.004 (0.102)		Define hole as datum zero
Front to Back Feature Location Tolerance: (Top to Bottom Tolerance Different Core 18 x 24 Panel)	+/- Inches (mm)	0.005 (0.127)		
Front to Back Feature Location Tolerance : (Top to Bottom Tolerance Same Core 18 x 24 Panel)	+/- Inches (mm)	0.003 (0.076)		
Feature Location Tolerance within entire pad stack to Master Drill Pattern: (Layer to Layer Tolerance 0.093 Thick 0.0098 Mechanical DHS 18 x 24 Panel)	Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Minimum Copper Pull-Back from NPT Hole on External Layers:	Inches (mm)	0.007 (0.178)		
Minimum Clearance from Internal Conductor to Non Plated Hole:	Inches (mm)	0.010 (0.254)		
Minimum Clearance from External Conductor to Non Plated Hole:	Inches (mm)	0.007 (0.178)		
Minimum Drilled Slot Width:	Inches (mm)	0.022 (0.55)		
Minimum Drilled Slot Length to Width Ratio (Length: Width):	Ratio	2:1		
Via In Pad Plated Over (VIPPO)				

		Multek Facility		Comments
		China B4		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
VIPPO Capability:	Yes / No	YES		
VIPPO with filled $\mu$ Via Capability:	Yes / No	YES		
Smallest Epoxy Filled Drilled Hole Size:	Inches (mm)	0.012 (0.305)		
Largest Epoxy Filled Drilled Hole Size: (2 mil dimpling allowed)	Inches (mm)	0.016 (0.406)		
Largest gap in DHS with Epoxy Filled Holes: (without Dimpling > 2.0 mils)	Inches (mm)	0.004 (0.102)		
Smallest Epoxy Filled $\mu$ Via Size:	Inches (mm)	0.012 (0.305)		
<b>Mechanical Blind and Buried Via</b>				
Mechanical Blind Via Capabilities:	Yes / No	YES		
Minimum Blind Mechanical DHS:	Inches (mm)	0.010 (0.254)		Not depth control drill.
Control Depth Blind Via Capability:	Yes / No	YES		
Control Depth Drilling Tolerance:	+/- Inches (mm)	0.005 (0.127)		
Mechanical Buried Via Capabilities:	Yes / No	YES		
Minimum Buried Via DHS:	Inches (mm)	0.010 (0.254)		
<b>Back-Drilling</b>				
Back-Drilling Capability:	Yes / No	No		
Depth Control Distance:	Inches (mm)	N/A		
Back-Drilling Depth Tolerance:	+/- Inches (mm)	N/A		
<b>Copper Plating</b>				
DC Plating Capabilities:	Yes / No	Yes		
Pulse Plating Capabilities:	Yes / No	No		
Solid Copper $\mu$ Via Fill:	Yes / No	Yes		
Solid Copper Thru Hole Fill:	Yes / No	8:1	10 : 1	
Copper Only Aspect Ratio:	Thkns to DHS	0.75:1	1:1	
$\mu$ Via Laser Drill Aspect Ratio:	Thkns to DHS	1 : 1		
Plated Board Edges Capability:	Yes / No	Yes		
Plated Internal Slots & Cut-outs Capability:	Yes / No	Yes		
Plated Milled Control Depth Milling:	Yes / No	Yes		
Plated C-Bore / C-Sink Holes:	Yes / No	Yes		
<b>Solder Mask</b>				
Solder Mask Types:	Types	Liquid Photo Imageable (LPI)		
Solder Mask Colors	Colors	Green	Blue	
Minimum Solder Mask Clearance: (LPI - Liquid Photo Imageable):	Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Pad size larger than NPTH:	Inches (mm)	0.01 (0.254)		
Over Surface Image:	Inches (mm)	0.006 (0.152)	0.004 (0.102)	
Web Between Surface Mount Pads:	Inches (mm)	0.003 (0.076)		

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		Multek Facility		Comments
		China B4		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Solder Mask Thickness Over Metal:	Inches (mm)	0.0004 (0.01)	0.0007 (0.018)	
Clearance over Via diameter:	Inches (mm)	0.006 (0.152)	0.004 (0.102)	
Pealable Mask Capability:	Yes / No	YES		
Pealable Mask Registration:	+/- Inches (mm)	0.015 (0.381)		
Pealable Mask Overhang:	Inches (mm)	0.020 (0.508)		
<b>Silk Screen / Legend Printing</b>				
Minimum Width Silk Screen Image:	Inches (mm)	0.006 (0.152)		
Minimum spacing between Silk Screen Image:	Inches (mm)	0.008 (0.203)		
Silk Screen Color Offering:	Colors	White	Yellow, Black	
<b>Mechanical Milling</b>				
Standard Router Bit Diameter:	Inches (mm)	.063 & (1.60 & 0.0787 2.00)	0.0472 (1.2 0.0394 1.00 0.0315 0.8)	
Routed Profile Tolerance:(18"X 24" Panel)	+/- Inches (mm)	0.007 (0.178)	0.005 (0.127)	
Routed Cutout Tolerance:(0.50" x 0.50")	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Minimum Internal Rout Radius:	Inches (mm)	0.0236 (0.599)	0.016 (0.406)	
Minimum Routed Slot Diameter:	Inches (mm)	0.0472 (1.200)	0.0315 (0.8)	
Finger Tip Angle and Tolerance:	+/- Degree Inches	5°		
Scoring Angles:	Degree	30°	60° / 45°	
Scoring Offset Tolerance:	+/- Inches (mm)	0.004 (0.102)		
Scoring Remaining Web Thickness:	Inches (mm)	0.016 (0.406)	0.012 (0.305)	
Scoring Remaining Web Tolerance:	+/- Inches (mm)	0.004 (0.102)		
Scoring True Position Tolerance:	Inches (mm)	0.004 (0.102)		
Control Depth Routing Depth Tolerance:	+/- Inches (mm)	0.006 (0.152)		
Counter Bore / Sink Depth Tolerance:	+/- Inches (mm)	0.006 (0.152)		
Minimum routed slot width:	Inches (mm)	0.0315 (0.8)	0.024 (0.6)	
<b>Testing</b>				
Minimum Test Continuity Resistance:	Ohms	50 Ohms	20 Ohms	
Maximum Test Voltage:	Volts	200V		
Maximum Test Isolated Resistance:	Ohms	10m Ohms	20m Ohms	
Largest Test Bed Fixture:	Inches (mm)	16.2" X 22.1"	20" X 24.4"	
Largest Test Bed Flying Probe:	Inches (mm)	16.5 X 22.5	20 X 24	
Electrical Test Pitch for Flying Probe:	Inches (mm)	0.012 (0.305)	0.007 (0.178)	
Electrical Test Pitch for Fixture Test:	Inches (mm)	0.0157 (0.399)		
TDR Test Tolerance Single Ended 50-75 Ohms:	+/- tolerance	+/- 10%	+/- 7.5%*	
TDR Test Tolerance Single Ended > 75 Ohms:	+/- tolerance	+/- 10%	+/- 7.5%*	
TDR Test Tolerance Differential Pair < 101 Ohms:	+/- tolerance	+/- 10%	+/- 7.5%*	
TDR Test Tolerance Differential Pair > 100 Ohms:	+/- tolerance	+/- 10%	+/- 7.5%*	

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		Multek Facility		Comments
		China B4		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
High Pot Test Voltage:(AC or DC):		500 V	As Requested	
4 Wire Testing Capability:	Yes / No	No		
LD Testing Capability:	Yes / No	No		
SET2DIL Testing Capability:	Yes / No	No		
<b>Surface Finish</b>				
Organic Solder Preservative (OSP) Capability:	Yes / No	Yes		
Immersion Gold (ENIG) Capability:	Yes / No	Yes		
Immersion Silver (Ag) Capability:	Yes / No	Yes		
Electrolytic Hard Gold Capability:	Yes / No	Yes		
Thick Soft Gold Capability:	Yes / No	Yes		
Immersion Tin (Sn) Capability:	Yes / No	Yes		
Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) Capability:	Yes / No	No		
Lead Free Hot Air Solder Level (Pb-Free HASL) Capability:	Yes / No	Yes		
Aspect Ratio for OSP:	DHS : Overall Thickness	10		
Aspect Ratio for ENIG:	DHS : Overall Thickness	8		
Aspect Ratio for Immersion Ag:	DHS : Overall Thickness	13		
Aspect Ratio for Electrolytic Hard Gold:	DHS : Overall Thickness	6		
Aspect Ratio for Selective Thick Gold:	DHS : Overall Thickness	6		
Aspect Ratio for Immersion Sn:	DHS : Overall Thickness	10		
Aspect Ratio for ENEPIG:	DHS : Overall Thickness	N/A		
Aspect Ratio for Pb-Free HASL:	DHS : Overall Thickness	8		
Recommended Plating Thickness for OSP:	Inches (mm)	0.000008 (0.0002)		
Recommended Plating Thickness for ENIG:	Inches (mm)	0.000002 (0.00005)		
Recommended Plating Thickness for Immersion Ag:	Inches (mm)	0.000006 (0.00015)		
Recommended Plating Thickness for Electrolytic Hard Gold:	Inches (mm)	0.000002 (0.00005)		
Recommended Plating Thickness for Selective Thick Gold:	Inches (mm)	0.00002 (0.00051)		
Recommended Plating Thickness for Immersion Sn:	Inches (mm)	0.0000315 (0.0008)		
Recommended Thickness (ENEPIG):	Inches (mm)	N/A		
Recommended Thickness for Pb-Free HASL:	Inches (mm)	TBD		ME Review Required

## 24.5. MULTEK B5 CAPABILITIES

- Advance Technology Multilayer
- High Layer Count
- High Aspect Ratio Plating
- BBV and Sequential Lamination
- HDI / Cu Filled  $\mu$ Vias
- 4 Wire Testing & AVI
- VIPPO and Back-Drilling

		Multek Facility		Comments
		China B5		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
<b>Number of Conductive layers:</b>				
Standard 150 Tg Materials:	Layer Count Range	1 – 18	18 – 30	
High 170 Tg Materials:	Layer Count Range	1 – 18	18 – 30	
Mid Loss Materials ( $Df < 0.011$ ):	Layer Count Range	1 – 18	18 – 30	
Low Loss Materials ( $Df < 0.007$ ):	Layer Count Range	1 – 18	18 – 30	
Roger 3000 Series Materials (Hybrid):	Layer Count Range	N/A	N/A	
Roger 4000 Series Materials:	Layer Count Range	1 – 2	N/A	
PTFE materials:	Layer Count Range	1 – 2	N/A	
<b>Minimum Dielectric Thickness (Core):</b>				
Standard 150 Tg Materials:	Inches (mm)	0.002 (0.051)	0.002 (0.051)	
High 170 Tg Materials:	Inches (mm)	0.002 (0.051)	0.002 (0.051)	
Mid Loss Materials ( $Df < 0.011$ ):	Inches (mm)	0.002 (0.051)	0.002 (0.051)	
Low Loss Materials ( $Df < 0.007$ ):	Inches (mm)	0.002 (0.051)	0.002 (0.051)	
Roger 3000 Series Materials (Hybrid):	Inches (mm)	N/A	N/A	
Roger 4000 Series Materials:	Inches (mm)	0.0040 (0.102)	0.004 (0.102)	
PTFE materials:	Inches (mm)	0.020		
<b>Minimum Dielectric Thickness (B-Stage):</b>				
Standard 150 Tg Materials:	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.0018	(1067 prepreg) 0.0018	
High 170 Tg Materials:	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.0018	(1067 prepreg) 0.0018	
Mid Loss Materials ( $Df < 0.011$ ):	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.0018	(1067 prepreg) 0.0018	
Low Loss Materials ( $Df < 0.007$ ):	(Glass Type) Nominal prepress Thickness	(106 prepreg) 0.0018	(1035) prepreg) 0.0018	
Roger 3000 Series Materials (Hybrid):	Yes / No	N/A	N/A	
Roger 4000 Series Materials:	(Glass Type) Nominal prepress Thickness	N/A	N/A	
PTFE materials:	Yes / No	NO	NO	

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Last Updated on: 1/13/2014

		Multek Facility		Comments
		China B5		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Buried Capacitance:	Yes / No	NO	NO	
Buried Resistance:	Yes / No	NO	NO	
<b>Production Panel Details</b>				
Panel Size:	Inches (mm)	18.00 X 24.00 (457 x 610)	21.00 x 24.00 (533 x 610)	
			16.00 x 21.00 (406 x 533)	
			14.00 x 24.00 (356 x 610)	
			16.00 X 18.00 (406 x 457)	
			14.00 X 16.00 (356 x 406)	
Non Usable Border on Panel:	Inches (mm)	0.6 (15.24)	0.4 (10.16)	
Spacing Between Boards:(Routing Process):	Inches (mm)	0.1 (2.54)	0.08 (2.032)	
<b>Lamination Process</b>				
Maximum Overall Thickness:	Inches (mm)	0.236 (5.994)	0.236 (5.994)	
Minimum Overall Thickness	Inches (mm)	0.020 (0.508)	0.02 (0.508)	
Flatness:(Inch/Inch):	Inches (mm)	0.004 (0.102)	0.002 (0.051)	
Overall Board Thickness Tolerance < 0.020":	+/- Inches (mm)	N/A	N/A	
Overall Board Thickness Tolerance ~0.031":	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Overall Board Thickness Tolerance ~0.062":	+/- Inches (mm)	0.006 (0.152)	0.006 (0.152)	
Overall Board Thickness Tolerance ~0.093":	+/- Inches (mm)	0.009 (0.229)	0.007 (0.178)	
Overall Board Thickness Tolerance ~0.125":	+/- Inches (mm)	0.012 (0.305)	0.01 (0.254)	
Overall Board Thickness Tolerance ~0.187":	+/- Inches (mm)	0.019	0.015 (0.381)	
HDI Structure Maximum:	n+n+n	1+n+1	3+n+3	
Maximum ELIC Layer Count:	Layer Count	N/A	N/A	
Thinnest plated core with a mechanical via :	Inches (mm)	0.020 (0.508)	N/A	
Thinnest Laser µVia Drilled Core:	Inches (mm)	0.002 (0.051)	N/A	
Maximum Number of Lamination Cycles:	Count	2	3	
Minimum Core Thickness for Build-up standard HDI with Plating:	Inches (mm)	0.02 (0.508)	0.02 (0.508)	
Minimum Core Thickness for ELIC with Solid Cu Via Plating:	Inches (mm)	N/A	N/A	
Maximum Core Thickness for ELIC with Solid Cu Via Plating:	Inches (mm)	N/A	N/A	
Maximum Dielectric Thickness for standard plated µVia:	Inches (mm)	0.008 (0.203)	0.01 (0.254)	
Maximum Dielectric Thickness for Solid Cu µVia	Inches (mm)	N/A	N/A	
<b>Circuit Etching</b>				
<b>Minimum Conductor Width</b>				
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.003 (0.076)	0.003 (0.076)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.003 (0.076)	0.003 (0.076)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Internal Starting Copper Weight 3 oz.:	Inches (mm)	0.012 (0.305)	0.008 (0.203)	
External Starting Copper Weight ½ oz.:	Inches (mm)	0.0035 (0.089)	0.003 (0.076)	

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Description	Unit	Multek Facility		Comments
		China B5		
External Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)	0.004 (0.102)	
External Starting Copper Weight 2 oz.:	Inches (mm)	0.009 (0.229)	0.008 (0.203)	
External Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	Inches (mm)	0.004 (0.102)	0.004 (0.102)	
External VIPPO Starting Copper Weight 1 oz.:	Inches (mm)	N/A	N/A	
External Cu µVia Fill Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	
External Cu µVia Fill with Thru Hole Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	
External Epoxy µVia and Thru Hole Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.004 (0.102)	0.004 (0.102)	
<b>Conductor Width Tolerance</b>				
Internal Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0006 (0.015)	0.0005 (0.013)	
Internal Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.0006 (0.015)	0.0006 (0.015)	
Internal Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.0016 (0.041)	0.0016 (0.041)	
Internal Starting Copper Weight 3 oz.:	+/- Inches (mm)	0.0024 (0.061)	0.0024 (0.061)	
External Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0008 (0.02)	
External Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0008 (0.02)	
External Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.0018 (0.046)	0.0018 (0.046)	
External Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0008 (0.02)	
External VIPPO Starting Copper Weight 1 oz.:	+/- Inches (mm)	N/A	N/A	
External Cu µVia Fill Starting Copper Weight ½ oz.:	+/- Inches (mm)	N/A	N/A	
External Cu µVia Fill with Thru Hole Starting Copper Weight ½ oz.:	+/- Inches (mm)	N/A	N/A	
External Epoxy µVia and Thru Hole Fill Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0008 (0.02)	
<b>Minimum Conductor Spacing (Airgap)</b>				
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.004 (0.102)	0.003 (0.076)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.006 (0.152)	0.006 (0.152)	
Internal Starting Copper Weight 3 oz.:	Inches (mm)	0.008 (0.203)	0.008 (0.203)	
External Starting Copper Weight ½ oz.:	Inches (mm)	0.004 (0.102)	0.004 (0.102)	
External Starting Copper Weight 1 oz.:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
External Starting Copper Weight 2 oz.:	Inches (mm)	0.008 (0.203)	0.007 (0.178)	
External Starting Copper Weight 3 oz.:	Inches (mm)	N/A	N/A	
External VIPPO Starting Copper Weight ½ oz.:	Inches (mm)	0.0045 (0.114)	0.004 (0.102)	
External VIPPO Starting Copper Weight 1 oz.:	Inches (mm)	N/A	N/A	
External Cu µVia Fill Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	
External Cu µVia Fill with Thru Hole Starting Copper Weight ½ oz.:	Inches (mm)	N/A	N/A	
External Epoxy µVia and Thru Hole Fill Starting Copper Weight ½ oz.:	Inches (mm)	0.0055 (0.14)	0.005 (0.127)	
<b>Spacing Tolerance</b>				

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Description	Unit	Multek Facility		Comments
		China B5		
Internal Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
Internal Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0006 (0.015)	
Internal Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.0012 (0.03)	0.0012 (0.03)	
Internal Starting Copper Weight 3 oz.:	+/- Inches (mm)	0.0016 (0.041)	0.0016 (0.041)	
External Starting Copper Weight ½ oz.:	+/- Inches (mm)	0.0008 (0.02)	0.0008 (0.02)	
External Starting Copper Weight 1 oz.:	+/- Inches (mm)	0.0012 (0.03)	0.001 (0.025)	
External Starting Copper Weight 2 oz.:	+/- Inches (mm)	0.0016 (0.041)	0.0014 (0.036)	
External Starting Copper Weight 3 oz.:	+/- Inches (mm)	N/A	N/A	
<b>Trace Crest To Base Difference</b>				
Internal Starting Copper Weight ½ oz.:	Inches (mm)	0.001 (0.025)	0.0005 (0.013)	
Internal Starting Copper Weight 1 oz.:	Inches (mm)	0.002 (0.051)	0.001 (0.025)	
Internal Starting Copper Weight 2 oz.:	Inches (mm)	0.003 (0.076)	0.002 (0.051)	
External Starting Copper Weight ½ oz.:	Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
External Starting Copper Weight 1 oz.:	Inches (mm)	0.001 (0.025)	0.0008 (0.02)	
External Starting Copper Weight 2 oz.:	Inches (mm)	0.0025 (0.064)	0.002 (0.051)	
Minimum Hole to copper feature (Via to adjacent trace):	Inches (mm)	0.01 (0.254)	0.0085 (0.216)	
Minimum Copper to Edge of Board Spacing Internal:	Inches (mm)	0.01 (0.254)	0.010 (0.254)	
Minimum Copper to Edge of Board Spacing External:	Inches (mm)	0.01 (0.254)	0.01 (0.254)	
Internal Plane to Edge of board spacing:	Inches (mm)	0.01 (0.254)	0.01 (0.254)	
Minimum Etched Nomenclature Starting Copper Weight ½ oz.:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Minimum Etched Nomenclature Starting Copper Weight 1 oz.:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Minimum Etched Nomenclature Starting Copper Weight 2 oz.:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	
Maximum Copper thickness per Inner Layer Core:	Oz.	2.0	3.0	
Maximum Copper thickness per Outer Layer Plated Surface:	Oz.	1.0	2.0	
<b>Via and Hole Drilling:</b>				
<b>Laser Drilling</b>				
Laser Drilling Capabilities:	Yes / No	YES		
Smallest Laser DHS:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
µVia Pad Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.006 (0.152)	0.006 (0.152)	
µVia Anti-Pad/Clearance Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.020 (0.508)	0.018 (0.457)	
Feature Location Tolerance within entire pad stack to Master Drill Pattern: (Layer to Layer Tolerance .020 Thick 0.004 DHS HDI/ELIC Build-up 18 x 24 Panel)	Inches (mm)	0.006 0.152	0.006 (0.152)	
<b>Mechanical Drilling</b>				
Mechanical Via Pad Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.090 (2.286)	0.008 (0.203)	
Mechanical Via Anti-Pad/Clearance Size (Drilled Hole Size + A):	DHS + X Inches (mm)	0.016 (0.406)	0.014 (0.356)	
Smallest DHS 0.062 Thick Board:	Inches (mm)	0.0098 (0.249)	0.0079 (0.201)	
Smallest DHS 0.093 Thick Board:	Inches (mm)	0.0098 (0.249)	0.0079 (0.201)	

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Description	Unit	Multek Facility		Comments
		China B5		
Smallest DHS 0.125 Thick Board:	Inches (mm)	0.0098 (0.249)	0.0079 (0.201)	
Smallest DHS 0.150 Thick Board:	Inches (mm)	0.012	0.0098 (0.249)	
Smallest DHS 0.187 Thick Board:	Inches (mm)	0.012	0.0098 (0.249)	
Smallest Non Plated Hole Size:(Finished)	Inches (um)	0.0125 (0.318)	0.010 (0.249)	
Largest Plated Hole Size Drilled:(Finished)	Inches (mm)	No limit	No Limit	
Largest Non-Plated Hole Size Drilled:	DHS + X Inches (mm)	No limit	No Limit	
Largest Tented Non-Plated Hole:	Inches (mm)	0.23622 (6.0)	0.23622 (6.0)	
Standard Plated Hole Tolerance:	+/- Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Press-Fit Plated Hole Tolerance:	+/- Inches (mm)	0.02 (0.508)	0.018 (0.457)	
Non-plated Hole Tolerance:	+/- Inches (mm)	0.002 (0.051)	0.001 (0.025)	
Minimum NPTH to Edge of Board Spacing:	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Drilled Hole Location Tolerance to Datum Zero: ( True Position across 18 x 24 ):	+/- Inches (mm)	0.003 (0.076)	0.003 (0.076)	
2nd Drill Hole Location Tolerance to Datum Zero: ( True Position across 18 x 24 panel )	+/- Inches (mm)	0.004 (0.102)	0.004 (0.102)	
Front to Back Feature Location Tolerance: (Top to Bottom Tolerance Different Core 18 x 24 Panel)	+/- Inches (mm)	0.003 (0.076)	0.003 (0.076)	
Front to Back Feature Location Tolerance : (Top to Bottom Tolerance Same Core 18 x 24 Panel)	+/- Inches (mm)	0.002 (0.051)	0.002 (0.051)	
Feature Location Tolerance within entire pad stack to Master Drill Pattern: (Layer to Layer Tolerance 0.093 Thick 0.0098 Mechanical DHS 18 x 24 Panel)	Inches (mm)	0.009 (0.229)	0.009 (0.229)	
Minimum Copper Pull-Back from NPT Hole on External Layers:	Inches (mm)	0.010 (0.254)	0.01 (0.254)	
Minimum Clearance from Internal Conductor to Non Plated Hole:	Inches (mm)	0.010 (0.254)	0.008 (0.203)	
Minimum Clearance from External Conductor to Non Plated Hole:	Inches (mm)	0.010 (0.254)	0.01 (0.254)	
Minimum Drilled Slot Width:	Inches (mm)	0.118 (3.0)	0.11811 (3.0)	
Minimum Drilled Slot Length to Width Ratio (Length:Width):	Ratio	2:1	2:1	
<b>Via In Pad Plated Over (VIPPO)</b>				
VIPPO Capability:	Yes / No	YES		
VIPPO with filled µVia Capability:	Yes / No	YES		
Smallest Epoxy Filled Drilled Hole Size:	Inches (mm)	0.009843 (0.25)	0.009843 (0.25)	
Largest Epoxy Filled Drilled Hole Size: ( 2 mil dimpling allowed )	Inches (mm)	0.023622 (0.6)	0.023622 (0.6)	
Largest gap in DHS with Epoxy Filled Holes: (without Dimpling > 2.0 mils)	Inches (mm)	0.019685 (0.5)	0.019685 (0.5)	
Smallest Epoxy Filled µVia Size:	Inches (mm)	0.005 (0.127)	0.004 (0.102)	
<b>Mechanical Blind and Buried Via</b>				
Mechanical Blind Via Capabilities:	Yes / No	YES		
Minimum Blind Mechanical DHS:	Inches (mm)	0.010 (0.249)	0.010 (0.249)	

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		Multek Facility		Comments
		China B5		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Control Depth Blind Via Capability:	Yes / No	YES		
Control Depth Drilling Tolerance:	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Mechanical Buried Via Capabilities:	Yes / No	YES		
Minimum Buried Via DHS:	Inches (mm)	0.010 (0.249)	0.0098 (0.249)	
<b>Back-Drilling</b>				
Back-Drilling Capability:	Yes / No	YES		
Depth Control Distance:	Inches (mm)	0.078740157	0.15748 (4.0)	
Back-Drilling Depth Tolerance:	+/- Inches (mm)	0.005	0.004	
<b>Copper Plating</b>				
DC Plating Capabilities:	Yes / No	YES		
Pulse Plating Capabilities:	Yes / No	YES		
Solid Copper $\mu$ Via Fill:	Yes / No	No	No	
Solid Copper Thru Hole Fill:	Yes / No	N/A		
Copper Only Aspect Ratio:	Thkns to DHS	0.542361111	15:1	
$\mu$ Via Laser Drill Aspect Ratio:	Thkns to DHS	0.8:1	0.8:1	
Plated Board Edges Capability:	Yes / No	YES		
Plated Internal Slots & Cut-outs Capability:	Yes / No	YES		
Plated Milled Control Depth Milling:	Yes / No	No	No	
Plated C-Bore / C-Sink Holes:	Yes / No	YES		
<b>Solder Mask</b>				
Solder Mask Types:	Types	Liquid Photo Imageable (LPI)		
Solder Mask Colors	Colors	Green	Blue	
Minimum Solder Mask Clearance: (LPI - Liquid Photo Imageable):	Inches (mm)	0.003 (0.076)	0.002 (0.051)	
Pad size larger than NPTH:	Inches (mm)	0.01 (0.254)	0.008 (0.203)	
Over Surface Image:	Inches (mm)	0.006 (0.152)	0.004 (0.102)	
Web Between Surface Mount Pads:	Inches (mm)	0.003 (0.076)	0.003 (0.076)	
Solder Mask Thickness Over Metal:	Inches (mm)	0.000276 (0.007)	0.000394 (0.01)	
Clearance over Via diameter:	Inches (mm)	0.008 (0.203)	0.006 (0.152)	
Pealable Mask Capability:	Yes / No	No	No	
Pealable Mask Registration:	+/- Inches (mm)	N/A	N/A	
Pealable Mask Overhang:	Inches (mm)	N/A	N/A	
<b>Silk Screen / Legend Printing</b>				
Minimum Width Silk Screen Image:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Minimum spacing between Silk Screen Image:	Inches (mm)	0.006 (0.152)	0.005 (0.127)	
Silk Screen Color Offering:	Colors	White	Yellow, Black	
<b>Mechanical Milling</b>				
Standard Router Bit Diameter:	Inches (mm)	0.07874 (2.0)	0.062 (1.57) 0.0469 (1.00)	
Routed Profile Tolerance:(18"X 24" Panel)	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Routed Cutout Tolerance:(0.50" x 0.50")	+/- Inches (mm)	0.005 (0.127)	0.004 (0.102)	
Minimum Internal Rout Radius:	Inches (mm)	0.031 (0.787)	0.016 (0.406)	

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		Multek Facility		Comments
		China B5		
Description	Unit	High Volume Mass Production Capable	Advanced Capable Production	
Minimum Routed Slot Diameter:	Inches (mm)	0.062 (1.575)	0.031 (0.787)	
Finger Tip Angle and Tolerance:	+/- Degree Inches	2°	2°	
Scoring Angles:	Degree	30°	25° / 45° / 60°	
Scoring Offset Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.004 (0.102)	
Scoring Remaining Web Thickness:	Inches (mm)	1/4 of board thickness	1/4 of board thickness	
Scoring Remaining Web Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.004 (0.102)	
Scoring True Position Tolerance:	Inches (mm)	0.004 (0.102)	0.004 (0.102)	
Control Depth Routing Depth Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.004 (0.102)	
Counter Bore / Sink Depth Tolerance:	+/- Inches (mm)	0.004 (0.102)	0.004 (0.102)	
Minimum routed slot width:	Inches (mm)	0.062 (1.575)	0.031 (0.787)	
<b>Testing</b>				
Minimum Test Continuity Resistance:	Ohms	20 Ohms	10 Ohms	
Maximum Test Voltage:	Volts	100V	250V	
Maximum Test Isolated Resistance:	Ohms	30m Ohms	100m Ohms	
Largest Test Bed Fixture:	Inches (mm)	19.2 X 25.6	22.0 X 40.0	
Largest Test Bed Flying Probe:	Inches (mm)	19.6 X 24.0	N/A	
Electrical Test Pitch for Flying Probe:	Inches (mm)	0.004 (0.102)	0.004 (0.102)	
Electrical Test Pitch for Fixture Test:	Inches (mm)	0.016 (0.406)	0.016 (0.406)	
TDR Test Tolerance Single Ended 50-75 Ohms:	+/- tolerance	+/- 10%	+/- 7%	
TDR Test Tolerance Single Ended > 75 Ohms:	+/- tolerance	+/- 10%	+/- 7%	
TDR Test Tolerance Differential Pair < 101 Ohms:	+/- tolerance	+/- 10%	+/- 7%	
TDR Test Tolerance Differential Pair > 100 Ohms:	+/- tolerance	+/- 10%	+/- 7%	
High Pot Test Voltage:(AC or DC):		500 V	As Requested	
4 Wire Testing Capability:	Yes / No	YES		
LD Testing Capability:	Yes / No	YES		
SET2DIL Testing Capability:	Yes / No	YES		
<b>Surface Finish</b>				
Organic Solder Preservative (OSP) Capability:	Yes / No	YES		
Immersion Gold (ENIG) Capability:	Yes / No	YES		
Immersion Silver (Ag) Capability:	Yes / No	YES		
Electrolytic Hard Gold Capability:	Yes / No	YES		
Thick Soft Gold Capability:	Yes / No	NO	No	
Immersion Tin (Sn) Capability:	Yes / No	YES		
Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) Capability:	Yes / No	NO	No	
Lead Free Hot Air Solder Level (Pb-Free HASL) Capability:	Yes / No	NO	Need Sub-contract	
Aspect Ratio for OSP:	DHS : Overall Thickness	16:1 (5mm board thickness)	16:1 (6mm board thickness)	
Aspect Ratio for ENIG:	DHS : Overall Thickness	10:1 (5mm board thickness)	13:1 (5mm board thickness)	

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Description	Unit	Multek Facility		Comments
		High Volume Mass Production Capable	Advanced Capable Production	
Aspect Ratio for Immersion Ag:	DHS : Overall Thickness	16:1 (6mm board thickness)	N/A	
Aspect Ratio for Electrolytic Hard Gold:	DHS : Overall Thickness	8:1 (3.5mm board thickness)	N/A	
Aspect Ratio for Selective Thick Gold:	DHS : Overall Thickness	N/A	N/A	
Aspect Ratio for Immersion Sn:	DHS : Overall Thickness	10:1 (4mm board thickness)	N/A	
Aspect Ratio for ENEPIG:	DHS : Overall Thickness	N/A	N/A	
Aspect Ratio for Pb-Free HASL:	DHS : Overall Thickness	N/A	N/A	
Recommended Plating Thickness for OSP:	Inches (mm)	0.0079-0.0237 (0.0002-0.0006)	N/A	
Recommended Plating Thickness for ENIG:	Inches (mm)	Ni: 0.1000-0.3150 (0.0025-0.0080); Au: 0.0012-0.0060 (0.00003-0.00015)	N/A	
Recommended Plating Thickness for Immersion Ag:	Inches (mm)	0.0056-0.0178 (0.00014-0.00045)	N/A	
Recommended Plating Thickness for Electrolytic Hard Gold:	Inches (mm)	Ni: 0.050-0.39 (0.00127-0.0100) Au: 0.003-0.05 (0.000076-0.00127)	N/A	
Recommended Plating Thickness for Selective Thick Gold:	Inches (mm)	N/A	N/A	
Recommended Plating Thickness for Immersion Sn:	Inches (mm)	0.0315-0.0552 (0.0008-0.0014)	N/A	
Recommended Thickness (ENEPIG):	Inches (mm)	N/A	N/A	
Recommended Thickness for Pb-Free HASL:	Inches (mm)	N/A	N/A	

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