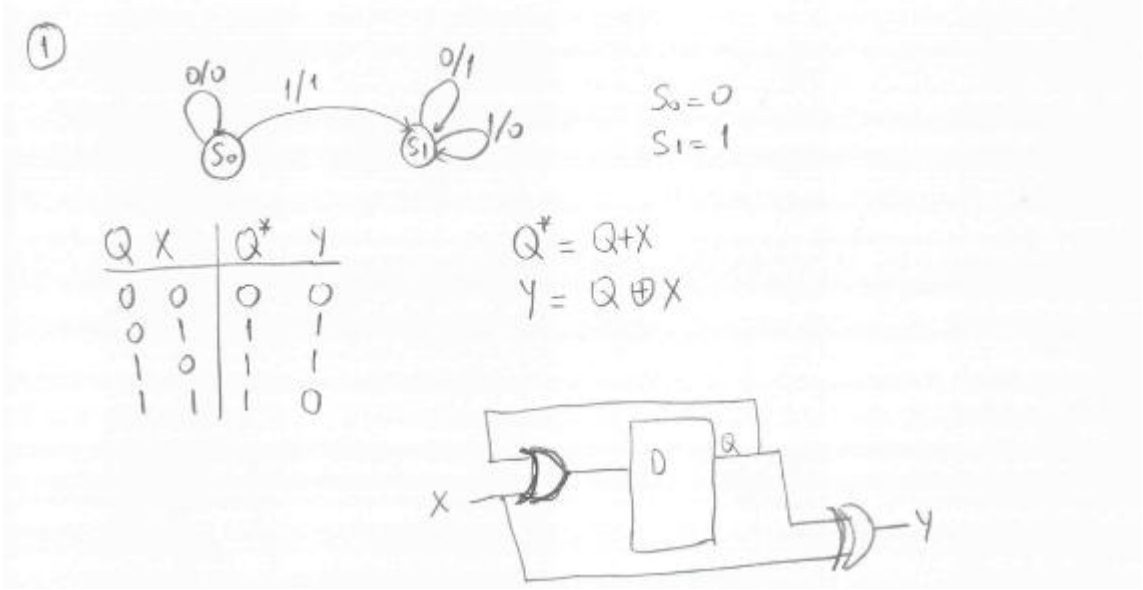
YOUR NAME:_____ ID:_____

Ankara University	**Computer Engineering Dept.**
COM275	**14.01.2014**
Digital Logic Design	**Final Examination**

Question	1	2	3	4	5	6	Total
Marks	20	20	20	20	10	10	100
Earned							

Q1. Design a one input, one output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. You should use at most one D flip-flop and additional gates for your circuit. Use Mealy type FSM.

Hint: 2's complement of a number can be obtained by keeping the least significant bits with value 0 and the first bit with value 1 as unchanged, and then complementing all remaining bits. Example: 011000 → 101000



Q2. a) Two functions F and G are implemented using 3 input – 2 output PLA. PLA table is given below. Determine the functions F and G as sum of minterms. $F = \sum(?)$ and $G = \sum(?)$. [14]

b) Implement F and G using a decoder and or gates. [6]

Product term	Inputs			Outputs (C)	Outputs (T)
	A	B	C	F	G
1	1	-	1	1	-
2	-	1	1	1	1
3	0	0	0	1	-
4	1	1	0	-	1

(2) a) $F = (AC + BC + A'B'C')'$

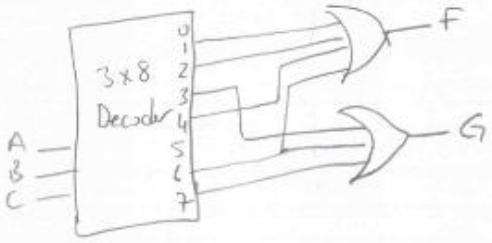
$G = BC + ABC'$

A	B	C	F	G
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1

$F = \Sigma(1,2,4,6)$

$G = \Sigma(3,6,7)$

b)



Q3. a) 4 bit data is coded with 3 parity bits that can correct one single bit error. The code at the receiver side is 10X1111. The receiver is sure that all the bits are correct but cannot read the third bit given as X. Determine the value of X. Show how you determine X. The answer without any work is not accepted.

b) For the data word 1101, construct an eight bit code that can correct single bit error and detect double bit errors.

3) a)

1	2	3	4	5	6	7
0	0	X	1	1	1	1

$C = C_1 C_2 C_4 = 0$

$C_1 = XOR(1,3,5,7) = XOR(0,X,1,1) = 0$

$C_2 = XOR(2,3,6,7) = XOR(0,X,1,1) = 0$

$C_4 = XOR(4,5,6,7) = XOR(1,1,1,1) = 0$

Then, X must be 0.

b)

P_1	P_2	3	P_4	5	6	7	P_8
1	2	3	4	5	6	7	8
		1		1	0	1	

$P_1 = XOR(3,5,7) = XOR(1,1,1) = 1$

$P_2 = XOR(3,6,7) = XOR(1,0,1) = 0$

$P_4 = XOR(5,6,7) = XOR(1,0,1) = 0$

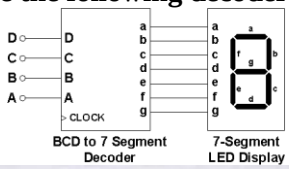
$P_8 = XOR(1,2,3,4,5,6,7) = XOR(1,0,1,0,1,0,1) = 0$

$\Rightarrow$

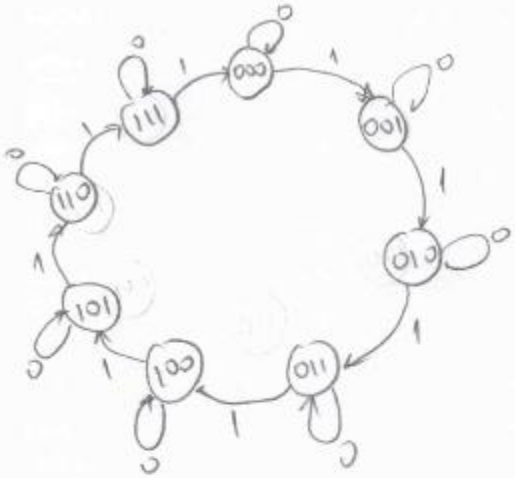
1	2	3	4	5	6	7
1	0	1	0	1	0	1

Code word = 10101010

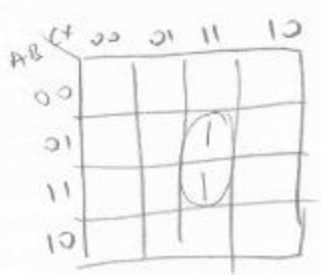
Q4. Design a digital circuit that counts the number of 1's in a 7-bit shift register. You should use T flip-flops for your circuit. Your circuit should display the value on a seven segment display. (Note that you do not need to design the seven segment display decoder, you can use the following decoder.)



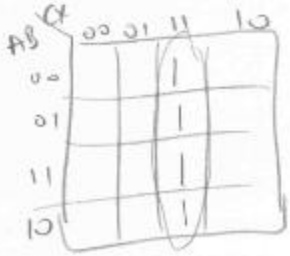
(4) 7-bit shift reg → X (You should count X.)



A	B	C	X	A^*	B^*	C^*	T_A	T_B	T_C
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0	0
0	0	1	1	0	1	0	0	1	1
0	1	0	0	0	1	0	0	0	0
0	1	0	1	0	1	1	0	0	1
0	1	1	0	1	0	0	0	1	0
0	1	1	1	1	0	0	0	1	0
1	0	0	0	1	0	1	0	0	1
1	0	0	1	1	0	1	0	0	0
1	0	1	0	1	1	0	0	1	1
1	0	1	1	1	1	0	0	1	1
1	1	0	0	1	1	1	0	0	0
1	1	0	1	1	1	1	0	0	0
1	1	1	0	1	1	1	0	0	0
1	1	1	1	0	0	0	1	1	1

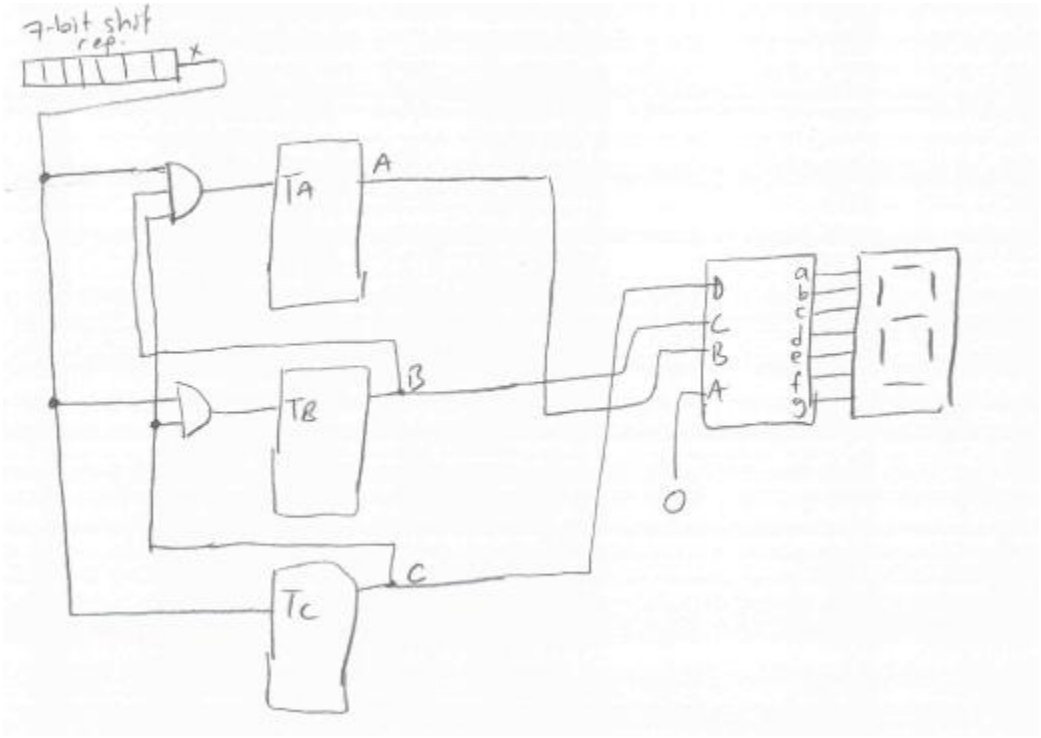


$T_A = BCX$

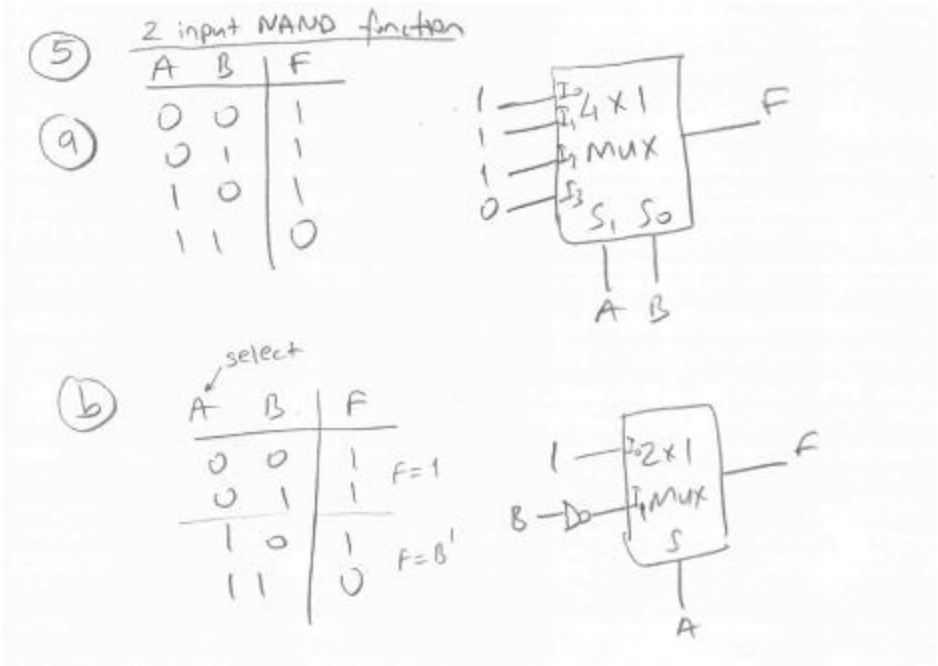


$T_B = CX$

$T_C = X$



Q5. **a) Design a two input NAND gate using a 4x1 MUX.**
b) Design a two input NAND gate using a 2x1 MUX and an inverter.



Q6. Design a T flip-flop that complements the value in flip-flop when T=0. When T=1, the value does not change. (Hint: You should use a D flip-flop and additional gates to design T flip-flop.)