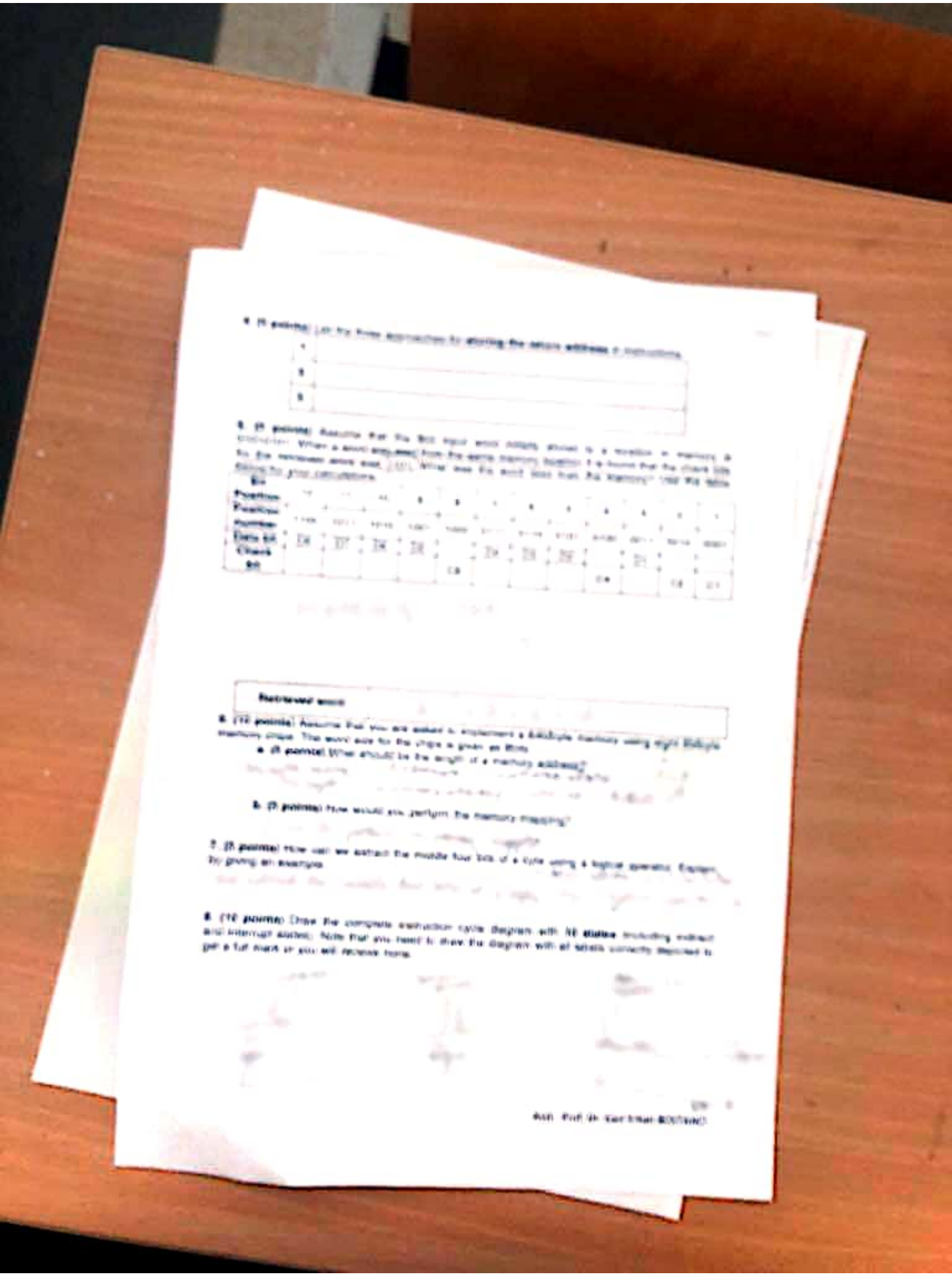


CamScanner ile tarandı

Name-S
Numbe
Durati
Note:

1. f

9. (15 points) Assume that you have the instruction format described below:

OPCODE	MODE	I	OPE1	OPE2
4 bit	2 bit	2 bit	8 bit	8 bit

The OPCODE field specifies the instruction as below. Assume the instructions take 2 parameters. Example:

```
SAL RX, 5; performs left arithmetic shift 5 times on RX register.
```

0001 is the code for SAL (Shift Arithmetic Left) instruction.
0010 is the code for SAR (Shift Arithmetic Right) instruction.
0100 is the code for the ROL (Rotate Left) instruction.

Note that the second operand can be stored in a register or memory location.

The MODE field indicates whether either of the OPE1 and OPE2 are register or memory addresses.
00: OPE1 and OPE2 are memory addresses.
01: OPE1 is register, OPE2 is memory address.
10: OPE1 is memory address, OPE2 is register.
11: OPE1 and OPE2 are registers.

Registers		
Code	Register	Value
00	R0	EB
01	R1	B3
10	R2	00
11	R3	51

Memory	
Address	Value
...	...
A1	03
A2	A3
A3	04
A4	A1
A5	03
...	...

I field indicates whether indirection is used:
00: No indirection is used for both OPE1 and OPE2.
01: Indirection is used only for OPE1.
10: Indirection is used only for OPE2.
11: Indirection is used for both OPE1 and OPE2.

Show the **output result and used operends** for the following instructions for the given memory and register values by giving full explanation of your solution to get a mark. Use (X) notation to indicate indirection where X can be a register (denote as e.g. R1) or a memory location (denote as e.g. [A1]).

i. (5 points)

OPCODE	MODE	I	OPE1	OPE2
0100	01	00	00000011	10100101

Operands Used	Result (in hexadecimal notation)

ii. (5 points)

OPCODE	MODE	I	OPE1	OPE2
0001	01	10	00000001	10100100

Operands Used	Result (in hexadecimal notation)

iii. (5 points)

OPCODE	MODE	I	OPE1	OPE2
0010	01	11	00000010	10100010

Operands Used	Result (in hexadecimal notation)

10. **(10 points)** Answer the following questions about cache memories.

a. **(5 points)** List the four **cache replacement algorithms**.

1.	
2.	
3.	
4.	

b. **(5 points)** Given a main memory of 32Mbytes and a cache memory with a capacity of 128Kbytes. Data can be transferred between the main memory and the cache as blocks of 4 bytes. What should be the length of the tag and line fields if direct mapping is used?

Tag	Line	Word
		2 bits

11. **(15 points)** Answer the following questions considering pipelining:

a. **(5 points)** Suppose you have a program with **100 lines of instructions**, not including any branching. There are a total of **six stages** for an instruction, each stage taking a single cycle. Compute the **speed-up** when pipelining is used rather than sequential execution.

b. **(10 points)** You have a system with a single memory port, but a separate port is available dedicated to the stack. **So you need to be careful when accessing the memory.** Consider the following pipelining scenario to identify the types of the hazards and indicate the numbers of related instructions (which pair of instructions) along with the reason why they occurred. **Note that out instruction uses an I/O port isolated from the memory.**

#	Instruction/Time	1	2	3	4	5	6	7	8	9	10
1	add ax, [si]	FI	DI	FO	EI	WO					
2	push bx		FI	DI	FO	EI	WO				
3	out ex			FI	DI	FO	EI	WO			
4	add cx, dx				FI	DI	FO	EI	WO		
5	and bx, 0					FI	DI	FO	EI	WO	
6	add bx, cx						FI	DI	FO	EI	WO

Hazard #	Hazard Type	Instruction Numbers (instA, instB)	Reason
1.			
2.			

Asst. Prof. Dr. Gazi Erkan BOSTANCI

Ankara University
Computer Engineering Department
Computer Architecture Final Exam

08.06.2018

name:

120 mins
The questions will be answered by only using the techniques discussed in the classes.
Write your answers right under the questions or in the given tables.
Good luck!

QUESTIONS

points) Answer the following questions considering modern computers.

a. (5 points) List the four main **structural components of a computer**

1.	
2.	
3.	
4.	

b. (5 points) List the four major **structural components of a processor.**

1.	
2.	
3.	
4.	

2. (10 points) You have a disk with an average seek time of 3ms. Its rotation speed is 20,000rpm. The disk is organized as 512-byte sectors with 500 sectors per track. Assume that the disk uses sequential organization.

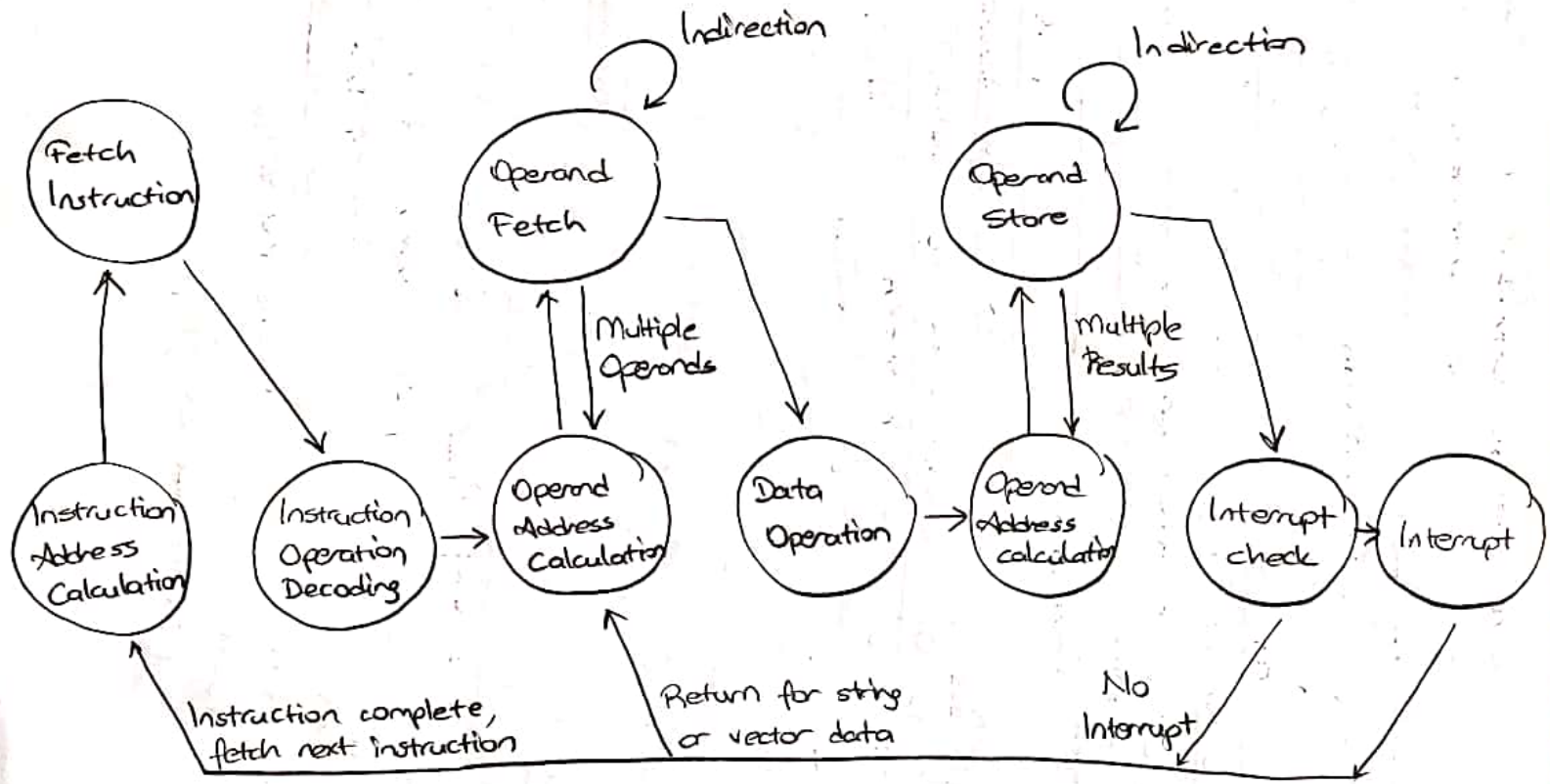
a. (5 points) How long would it take to read a file consisting of 3000 sectors?

b. (5 points) What is the total size of the file read in **MB**?

3. (5 points) What is the advantage of using **data striping** in RAID (Redundant Arrays of Independent Disks) systems for all levels? Explain in detail.

Asst. Prof. Dr. Gazi Erkan BOSTANCI

8) Instruction cycle grafiği:



1) Answer the fdlaing questions considering moden computer.

a. List the four main structual components of a computer.

1. Main Memory
2. CPU (Control Processing Unit)
3. I/O
4. System Interconnection

b. Use the four major structual components of a processor.

1. ALU (Arithmetic Logic Unit)
2. Register
3. Control Unit
4. CPU Interconection

2) You have a disk with on average seek time of 3 ms: Its rotation speed is 20.000 rpm. The disk is organized as 512-byte sectors with 500 sectors per track. Assume that the disk uses sequential organization.

a. How long would it take to read a file consisting of 3000 sectors?

İlk track ⇒ Average seek time : 3
Average rotational time: 1,5
Read 500 sector : 3
+
7,5 ms

60 000 ms / x ms = 20.000 tur / 1 tur

$x = \frac{60.000}{20.000} = \boxed{3 \text{ ms}}$ Avrg = 1,5 ms

$\frac{3000}{500} = 6$ track gerekli

Total = 7,5 + (5 x 4,5) = 30 ms = 0,03 sn

↓ 1 track için → geri kalan 5 track için

b. What is the total size of the file read in MB?

$\frac{512 \times 500 \times 6}{10^6} = 1,536$ MB

9)

I) 00 → direct
01 → Indirect for OPE1
10 → Indirect for OPE2
11 → Indirect for OPE1, OPE2

Registers		
Code	Register	Value
00	R0	EB
01	R1	B3
10	R2	00
11	R3	51

Memory	
Address	Value
...	...
A1	03
A2	A3
A3	04
A4	A1
A5	03
...	...

MODE
01 → OPE1 register OPE2 memory
00 → Illside Memory
10 → OPE1 memory OPE2 register
11 → Illside register

0001 → SAL (Shift Arithmetic Left)
0010 → SAR (Shift Arithmetic Right)
0100 → ROL (Rotate Left)

i)

OPCODE	MODE	I	OPE1	OPE2
0100	01	00	00000011	10100101
ROL		Direct	Register R3	Memory

Operands Used	Result
R3, A5	8A
(51) (03)	

→ 128 + 32 + 4 + 1 = 165 = $(A5)_{16}$

ROL R3, 3
ROL 01010001, 3

10001010 = 128 + 8 + 2 = 138 = $(8A)_{16}$

ii)

OPCODE	MODE	I	OPE1	OPE2
0001	01	10	00000001	10100100
SAL		Indirect for OPE2	Register	Memory

Operands Used	Result
R1, A4	98
(03) (3)	

→ 128 + 32 + 4 = 164 = $(A4)_{16}$

B3 = 16 × 11 + 3 = 179

SAL R1, 3
SAL 10110011, 3 (Soldan 3 bit sil sona 3 sıfır ekle)
10011000 = 128 + 16 + 8 = 152 = $(98)_{16}$

(Sadece sıfır ekle)

3) What is the advantage of using data striping in RAID system for all levels? Explain in detail.

Data striping, gelen verinin parçalandıktan sonra local disklerden birine map edilmesidir. Yani; veri bloklar halinde farklı disklerde tutulur. Böylece; eğer birden fazla ard arda striplari talep eden bir I/O request gelirse, farklı disklere aynı anda erişerek paralellik sağlandığı için, tüm isteklere cevap verilir ve transfer time azalır. Bu durumda performansı arttırır.

4) Mapping çeşitleri: Direct, Associative, Set associative

5) Hamming code sorusu.

6) Assuming that you are asking to implement 64 mb memory chip. The word size for this chip is ---

a. What should be the length of memory?

b. How would you perform the memory mapping?

$$CPI = \sum_{i=1}^{n} \frac{CPI_i \times I_i}{I_c}$$

$$MIPS\ rate = \frac{f}{CPI \times 10^6}$$

7) How can we extract the middle four bits of a byte using a logical operation. Explain by giving an example.

Bu daya bitwise masking denir. AND, OR veya XOR ile yapılabilir.

AND operatörünü kullanarak 4 bitlik kısmı 0000 ile geri kalanı 1 ile ordleyebiliriz.

Bit 101010 1111000000
111111 0000111111 AND

bunun la ordlersek sadece ortadaki 4 biti sıfırlamış olunuz.

ya da 0x3C ile ordleyek veya'da 2 bit bir tarafa 4 bit de diğer tarafa shiftleyek de yeterlidir.

4- [illegible] ...sociative, set associative

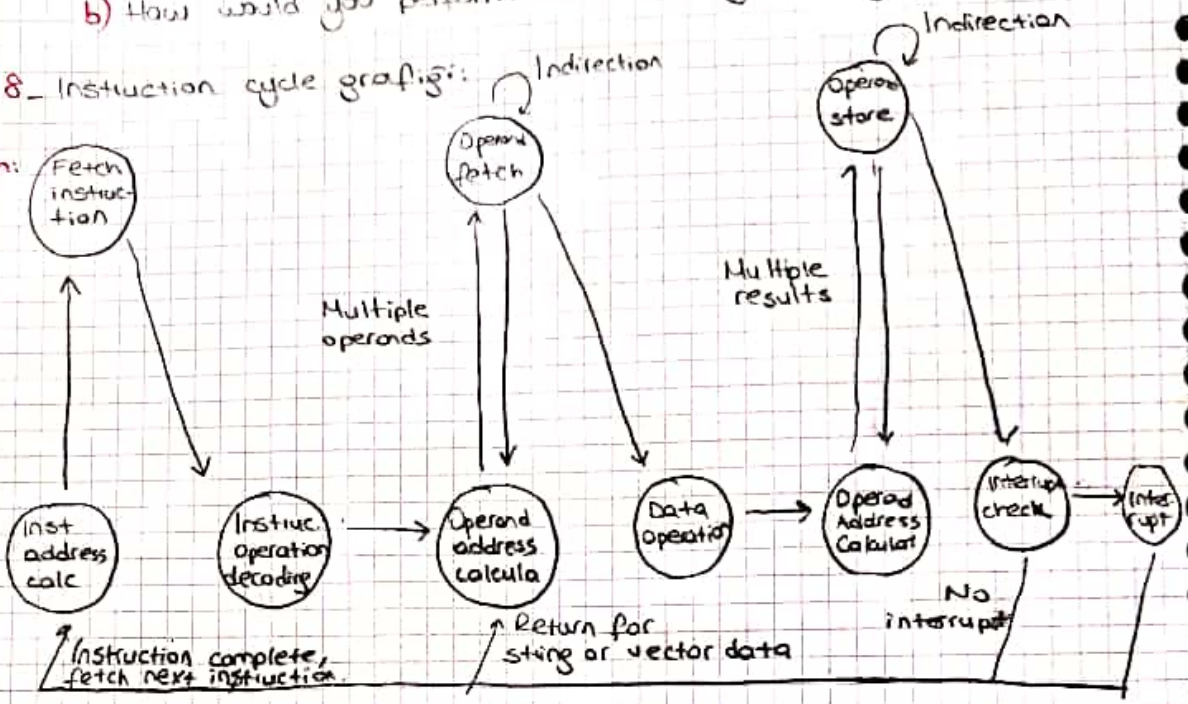
5- Hamming code [illegible]

6- a) What should be the length of memory addressing?

b) How would you perform the memory mapping?

8- Instruction cycle grafiği:

Çözüm:



9-

i-

OPCODE	MODE	I	OPE1	OPE2
0100	01	00	00000011	10100101

ROL

Direct Register Memory

Operands used	Result (in HEX)
R3, AS (51) 3	8A

ii-

OPCODE	MODE	I	OPE1	OPE2
0001	01	10	0000001	10100100

SAL

OPE2 için Register indirect, Memory

Operands used	Result
R1, (A4) (B3) 3	98

iii-

OPCODE	MODE	I	OPE1	OPE2
0010	01	11	00000010	10100010

SAR

2si için indirect, Register, Memory

Operands used	Result
(R2), (A2) (E3) 4	F5

Çözüm: i- ROL R3, 3

ROL 01010001, 3

10001010 = 128+8+2
= 138
= (8A)16

① 128+32+16+1 = 165 | 16 / 10 → AS / 5

② 81 / 64 = 17 = 16 / 1 → 01010001

③ 138 | 16 / 128 / 10 | 8

iii)

OPCODE	MODE	I	OPE1	OPE 2
0010	01	11	00000010	10100010
↓ SAR		↓ Indirect for OPE1, OPE2	↓ Register → R2	↓ Memory

Operands used	Result
R2, A2	FE
(EB) (04)	

↳ 10100010 = 128+32+2

SAR R2, 4 (soldan son 4 biti sil, sola 4 tane) = 162 = (A2)$_{16}$
1 ekle

SAR 11101011, 4 EB = 16×14 + 11 = 235

11111110 = 128+64+32+16+8+4+2 = 254

sign bit ne ise onu ekle

254 | 16
-16 | 15
94
=80
14

FE

10) a. List the four cache replacement algorithms

1. First In First Out (FIFO)
2. Least Recently Used (LRU)
3. Least Frequently Used (LFU)
4. Random

b. Given a main memory of 32 Mbytes and a cache memory with a capacity of 128 Kbytes. Data can be transferred between the main memory and the cache as blocks of 4 bytes. What should be the length of the tag and line fields if direct mapping is used?

Tag	Line	Word
8 bit,	15 bit	2 bits

25

8 17

Memory = $32 \times 2^{20} = 2^{25}$

Cache = $128 \times 2^{10} = 2^{17}$

$\frac{2^{17}}{2^2} = 2^{15}$ (line)

$\frac{2^{25}}{2^{17}} = 2^8$ 8 bit tag

a.

11) Suppose you have a program with 100 lines of instructions not including any branching. There are a total of six stages for an instruction, each stage taking a single cycle. Compute the speed-up when pipelining is used rather then sequential execution.

$$S_k = \frac{T_{1,n}}{T_{k,n}} = \frac{kn}{k+(n-1)} =$$

(stage $k=6$, line $n=100$)

$$S_6 = \frac{T_{1,100}}{T_{6,100}} = \frac{6 \times 100}{6+(100-1)} = \frac{6 \times 100}{6+99} = \frac{600}{105} = 5,71$$

b.

	#	Instruction, Time	1	2	3	4	5	6	7	8	9	10
1 port memory → M	1	add ax, [si]	FI	DI	FO	EI	WO					
	2	push bx		FI	DI	FO	EI	WO				
1 port stack → S	3	out bx			FI	DI	FO	EI	WO			
M	4	add cx, dx				FI	DI	FO	EI	WO		
M	5	and bx, 0					FI	DI	FO	EI	WO	
M	6	add bx, cx						FI	DI	FO	EI	WO

Hazard #	Hazard type	Instruction Numbers	Reason
1.	Resource Hazards	4, 6	Aynı anda memory e erişmeye çalışıyor
2.	Data Hazards	4, 6	Cx'in yeni değeri yazılmadan fetch edilmeye çalışılıyor.

(Kaynak eksikliği? — Kaynak az)

Control Hazards

SHR → 0 ekle → kaydır.

SHL → 0 ekle ← kaydır.

7) 10011101

2 kere sağ SHR 00100111

2 kere sol SHL 10011100

2 kere sol SHL 01110000

2 kere sağ SHR 00011100

10011101

00 0111 00

Instruction complete, fetch next instruction

string or vector data

9-

i-

OPCODE	MODE	I	OPE1	OPE2
0100	01	00	00000011	10100101

ROL

Direct Register Memory

ii-

OPCODE	MODE	I	OPE1	OPE2
0001	01	10	00000001	10100100

SAL

OPE2 is in Register indirect, memory

iii-

OPCODE	MODE	I	OPE1	OPE2
0010	01	11	00000010	10100010

SAAR

OPE2 is in Register indirect, memory

Çözüm: i- ROL R3, 3

ROL 01010001, 3

10001010 = 128+8+2
= 138
= (8A)16

Operands Used	Result (in HEX)
R3, AS (R3) 3	8A

Operands Used	Result
R1, (A4) (R1) 3	98

Operands Used	Result
(R2), (A2) (R2) 4	FE

① 128+32+4+1 = 165 | 16 | 10 | AS | 5

② 81 | 64 | 17 = 16 | 1
01010001

③ 138 | 16 | 128 | 8 | 10

b) Given a mai
with a capacity of
main memory and t
be the length of

TOR
8 bit

Çözüm: Memory = 32
Cache = 12

(1-a) Suppose yo
not including cy
instruction, each
when pipelining is

Çözüm: S_k =

S_b =

b) 4, 6 -
4, 6

10-a) List the four cache replacement algorithms.

Çözüm: 1_First in First out (FIFO)

2_Least Recently Used

3_Least Frequently Used

4_Random.

b) Given a main memory of 32 Mbytes and a cache memory with a capacity of 128 Kbytes Data can be transferred between the main memory and the cache as blocks of 4 bytes. What should be the length of the tag and line fields if direct mapping is used?

Tag	Line	Word
8 bit.	15 bit	2 bits

} 25 bit

Çözüm: Memory $= 32 \times 2^{20} = 2^{25}$

Cache $= 128 \times 2^{10} = 2^{17}$

$\frac{2^{17}}{2} = 2^{15}$.

11-a) Suppose you have a program with 100 lines of instructions, ... There are a total of six stages for an

ii- SAL R1, 3

SAL 10110011, 3

10011000 = 128+16+8
= 152
= (98)16

① 128+32+4 = 164 = A4

② 16x11+3 = 179 =

③ 152 | 16
144 | 9
8

iii- SAR R0, 4

SAR 11101011, 4

11111110 = 255
= FF

① 128+32+2 = 162 = A2

② 16x14+11 = 235

③ 255 | 16
16 | 15
95
90

10- a) List the four cache replacement algorithms

Çözüm: 1- First in First Out (FIFO)
2- Least Recently Used
3- Least Frequently Used
4- Random.

b) Given a main memory of 32 Mbytes and a cache memory with a capacity of 128 Kbytes Data can be transferred between the main memory and the cache as blocks of 4 bytes. What should be the length of the tag and line fields if direct mapping is used?

Tag	Line	word
6 bit	17 bit	2 bits

} 25 bit

Çözüm: Memory = $32 \times 2^{20} = 2^{25}$

Cache = $128 \times 2^{10} = 2^{17}$

11- a) Suppose you have a program with 100 lines of instructions, not including any branching. There are a total of six stages for an instruction, each stage taking a single cycle. Compute the speed-up when pipelining is used rather than sequential execution.

Çözüm:

$$S_k = \frac{T_{1,n}}{T_{k,n}} = \frac{kn}{k+(n-1)} \qquad k=6,\ n=100$$

$$S_6 = \frac{T_{1,100}}{T_{6,100}} = \frac{6 \times 100}{6+99} = \frac{600}{105} = 5.71$$

b)

4, 0 → Resource hazard → Aynı anda memory'e erişmeye çalışıyorlar.

4, 0 → data hazard → CX'in yeni değeri yazılmadan fetch edilmeye çalışıyor.

1) Answer the following questions considering modern comp.

a- List the four main structural components of a computer.

Çözüm: 1- Main memory
2- CPU (Central Processing unit)
3- I/O
4- System interconnection.

b- List the four major structural components of a processor

Çözüm: 1- ALU
2- Register
3- Control unit
4- CPU interconnection

2) You have a disk with an average seek time of 3 ms. Its rotation speed is 20.000 rpm. The disk is organized as 512-byte sectors with 500 sectors per track. Assume that the disk uses sequential organization.

a- How long would it take to read a file consisting of 3000 sectors?

Çözüm: ilk track → Average seek time: 3
Average rotational time: 1.5
Read 500 sector: + 3
7.5 ms.

60.000 msn — 20.000 tur
x ms — 1 tur

x = 3 ms Aur = 1.5 ms

3000/500 = 6 track gerekli

Total = 7.5 + (5 x 4.5) = 30 ms = 0.003 sn

(7.5: 1. track için; 5 x 4.5: Geri kalan 5 track için.)

b- What is the total size of the file read in MB?

$$\frac{512 \times 500 \times 6}{10^6} = 1.536 \text{ MB}$$

3- What is the advantage of using data striping in RAID systems for all levels? Explain in detail

Data striping, gelen verinin parçalandıktan sonra local disc'lerden birine map edilmesidir. Yani; veri bloklar halinde farklı disklerde tutulur.

Böylece: eğer birden fazla ardarda stripleri talep eden bir I/O request gelirse, farklı disklere aynı anda erişerek paralellik sağlandığı için, tüm isteklere cevap verilir ve transfer time azalır. Bu durum da performansı artırır.