Silicon Fabrication Handbook
Intro to CMOS
Version: 1.0
Date: 2026-02-21

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Slide 1: Why CMOS Matters
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- CMOS (Complementary Metal-Oxide-Semiconductor) is the dominant
  technology for digital ICs due to low static power and high density.
- It combines NMOS and PMOS transistors so one network pulls up while
  the other pulls down, reducing DC current except during switching.
- Applications: CPUs, memory, sensors, mixed-signal interfaces, MEMS-CMOS SoCs.

Speaker note:
CMOS scaling enabled Moore-era performance gains while controlling power.

Slide 2: Learning Objectives

By the end of this session, learners should be able to:
1) Describe the CMOS process from bare wafer to packaged die.
2) Distinguish FEOL vs BEOL steps.
3) Explain threshold voltage control and short-channel challenges.
4) Interpret a basic CMOS inverter transfer behavior.
5) List key metrology and reliability checks in production.

Slide 3: CMOS Inverter Concept

- PMOS at top (pull-up), NMOS at bottom (pull-down).
- Input low -> PMOS ON, NMOS OFF -> output high.
- Input high -> PMOS OFF, NMOS ON -> output low.
- Static ideal: near-zero direct path from VDD to GND.

Important metrics:
- Noise margins (NMH, NML)
- Propagation delay (tpHL, tpLH)
- Dynamic power: P_dynamic = alpha * C_load * VDD^2 * f

Slide 4: End-to-End Fabrication Flow

1) Starting substrate / epitaxy
2) Isolation (STI)
3) Well formation (n-well / p-well)
4) Gate stack formation (oxide + gate material)
5) Source/Drain engineering (LDD, spacers, implants)
6) Activation anneal
7) Silicidation
8) Contact formation
9) Metal interconnect stack (BEOL)
10) Passivation, test, dicing, packaging

FEOL = transistor creation on silicon.
BEOL = wiring and interconnect layers.

Slide 5: FEOL Deep Dive

Isolation:
- STI prevents leakage paths between neighboring devices.

Well and channel engineering:
- Ion implantation defines conductivity type and doping profiles.
- Vt adjustment uses channel implants and gate work-function tuning.

Gate stack:
- Historic: SiO2 + poly-Si
- Advanced: high-k dielectric + metal gate to reduce leakage.

Source/Drain:
- Extension implants reduce hot-carrier effects.
- Spacers and raised S/D reduce resistance and control overlap.

Slide 6: BEOL Deep Dive

Interconnect objectives:
- Low resistance, low capacitance, strong reliability.

Typical BEOL steps:
- Dielectric deposition (low-k)
- Patterning trenches/vias
- Barrier/liner + Cu fill (damascene)
- CMP planarization
- Repeat for multi-level metal stack

Reliability concerns:
- Electromigration
- Stress migration
- TDDB in interlayer dielectrics

Slide 7: Scaling and Device Challenges

As dimensions shrink:
- Short-channel effects increase (DIBL, Vt roll-off)
- Gate leakage and variability become more critical
- Power density and thermal issues rise

Technology responses:
- High-k/metal gate
- Strain engineering
- FinFET / GAA structures
- Advanced patterning and design-technology co-optimization (DTCO)

Slide 8: Process Control and Metrology

In-line checks include:
- Film thickness: ellipsometry
- CD and overlay: CD-SEM / scatterometry
- Implant dose/energy: SIMS and sheet resistance monitors
- Defect inspection: optical/e-beam inspection

Electrical monitors:
- I-V parametric tests (Id-Vg, Id-Vd)
- Ring oscillator speed monitors
- Leakage and breakdown structures

Goal: stable yield and predictable performance.

Slide 9: Example Design Tradeoffs

Tradeoff 1: Performance vs power
- Higher VDD improves speed but increases dynamic and leakage power.

Tradeoff 2: Drive strength vs area
- Wider transistors switch faster but consume area and capacitance.

Tradeoff 3: Reliability vs aggressiveness
- Aggressive scaling improves density but tightens process windows.

Engineering rule:
Optimize at system level, not just transistor level.

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Slide 10: Summary
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Key takeaways:
- CMOS success comes from complementary operation + scalable process.
- FEOL builds transistors; BEOL connects them into useful circuits.
- Modern nodes rely on materials and architecture innovation as much as lithogra
phy.
- Metrology and process control are essential for manufacturability.

Next reading in this repository:
- docs/02-cmos-feol/transistor-fabrication.md
- docs/03-cmos-beol/metallization.md
- docs/07-testing-yield/parametric-testing.md

End of deck.
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