RTL Operation Sequence by Team 15:

Cycle 1: DR←M[AR],, S2S1S0=110 , set load_DR = 1,set enable read pin=1

Cycle 2: AR←AR+1, set load_AR=1

Cycle 3: AR←AR+1, set load_AR=1

Cycle 4: AR←AR+1, set load_AR=1

Cycle 5: AC←M[AR], read pin=1,set load AC=1, S2S1S0=110,C3C2C1C0=0010

Cycle 6: AC← Complement(AC), C3C2C1C0=0110, set load_AC = 1

Cycle 7: ,AC ←AC+1

Cycle 8: AC←AC*DR, AR←AR+1, C3C2C1C0=1000, set load_AC ,AR=1

Cycle 9: M[AR]←AC, S2S1S0=011 (AC to bus), enable write pin=1