SSD Testing

#	0010	0100100
#	0011	0110000
ŧ	0100	0011001
#	0101	0010010
#	0110	0000010
#	0111	1111000
#	1000	0000000
#	1001	0010000
#	1010	0001000
ŧ	1011	0000011
#	1100	1000110
ŧ	1101	0100001
#	1110	0000110

1111 0001110

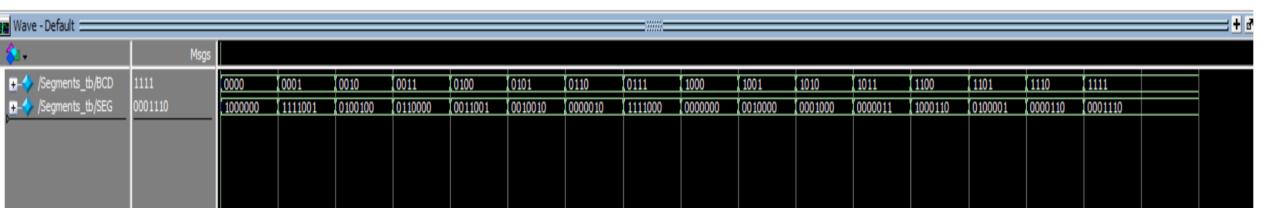
0001 1111001

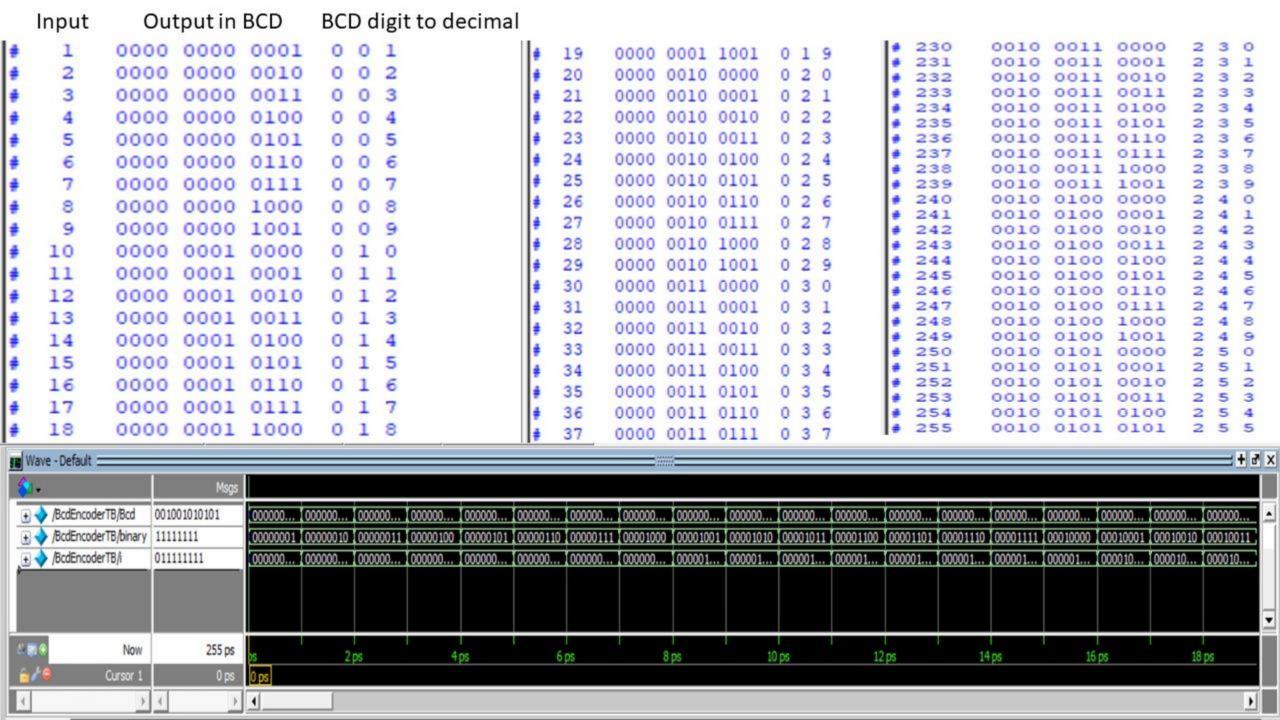
0000

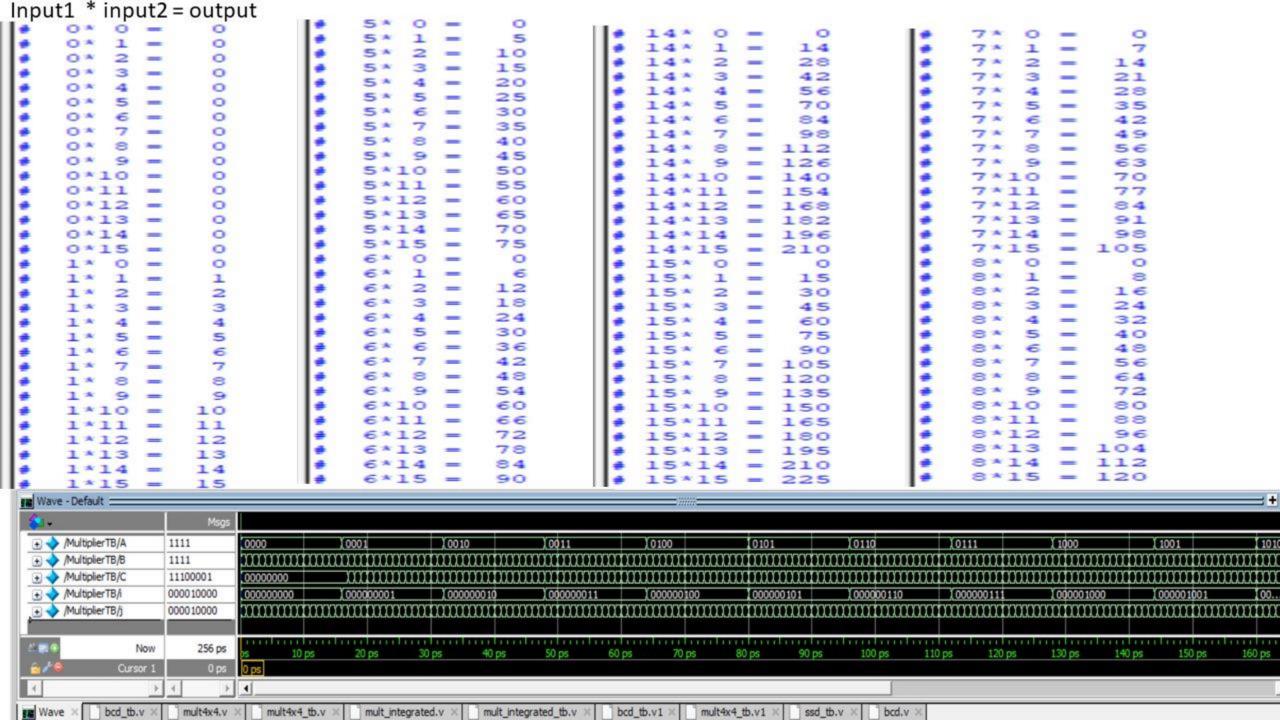
SEG

1000000

in[30]	out[6:0]	Digit	in[30]	out[6:0]	Digit
0000	1000000	0	1000	0000000	8
0001	1111001	1	1001	0010000	9
0010	0100100	2	1010	0001000	R
0011	0110000	3	1011	0000011	Ь
0100	0011001	4	1100	1000110	E
0101	0010010	5	1101	0100001	d
0110	0000010	6	1110	0000110	Ε
0111	1111000	7	1111	0001110	F







Testing The Whole Integrated Circuit

3	2 Seg3	L Seg2	Seg.	A2	A1	#
0 * 0 = 0	1000000	1000000	1000000	0000	0000	#
15 * 1 = 15	0010010	1111001	1000000	0001	1111	ŧ
15 * 15 = 225	0010010	0100100	0100100	1111	1111	ŧ
9 * 8 = 72	0100100	1111000	1000000	1000	1001	#
6 * 9 = 54	0011001	0010010	1000000	1001	0110	#
4 * 7 = 28	0000000	0100100	1000000	0111	0100	#
7 * 7 = 49	0010000	0011001	1000000	0111	0111	#

in[30]	out[6:0]	Digit	in[30]	out[6:0]	Digit
0000	1000000	0	1000	0000000	8
0001	1111001	1	1001	0010000	9
0010	0100100	2	1010	0001000	R
0011	0110000	3	1011	0000011	Ь
0100	0011001	4	1100	1000110	Ε
0101	0010010	5	1101	0100001	d
0110	0000010	6	1110	0000110	Ε
0111	1111000	7	1111	0001110	F

