Zeyu Guo

Wuhan,China | guozy@hust.edu.cn | +86 136-5989-5787 | ZeyuGuo.github.io

Education

Huazhong University of Science and Technology (985 project) Sept 2022 – July 2025 (expected)
MPhil candidate in Information and Communication Engineering. GPA: 3.73/4.0. Wuhan,China

Wuhan University of Technology (211 project) Sept 2018 – June 2022
B.E. in Electronic Information Engineering. GPA: 3.77/4.0; rank: 13/240, top 6%. Wuhan,China

Projects

FPGA-based DNN Inference Optimization: using hls4ml, PolyLUT, and PolyLUT-Add. Oct 2024 - Present
Description: In this project, I gained expertise in FPGA-based deep neural network (DNN) optimization by reproducing results from several open-source projects. Using the Jet Substructure Classification dataset, I utilized a 6-bit quantization and 75% compression by open-source library *hls4ml*, resulting in a 2.6× reduction in LUT usage and a 1.3× decrease in latency, compared to a baseline DNN model with (64, 32, 32, 5) neurons and 16-bit precision, using Vivado HLS. Additionally, I reproduced two state-of-the-art LUT-based DNN models, *PolyLUT* and *PolyLUT-Add*, which, in comparison to the baseline, achieved a 9.9× and 122× reduction in LUT usage and a 10.8× and 13× decrease in latency, respectively.

An FPGA CI/CD Pipeline. Sept 2024 - Oct 2024
Description: In this project, I developed an FPGA CI/CD pipeline for Vivado 2024.01. I began by creating a Dockerfile to build a custom Vivado Docker image. The toolchain I implemented automatically initiates a Docker container on a Linux machine whenever a new commit is detected on my Bitbucket repository. Using custom TCL scripts, the pipeline synthesizes and implements the committed FPGA design. Upon completion, the generated bitstream is tagged with the commit hash and securely stored in Artifactory for future reference.

An FPGA-based PVT-Insensitive Picosecond Resolution Timing Generator for ATE. Oct 2023 - Mar 2025
Description: In this project, I developed a timing generator (TG) to produce precise timing signals for automatic test equipment (ATE) used in digital IC testing. I introduced an interpolation method to enhance both resolution and linearity, along with a robust offset canceller to improve resilience to PVT (process, voltage, and temperature) variations. The TG was implemented on a Xilinx `xcku060ffva1156-2-i` FPGA with a 266.5 MHz clock frequency. Test results demonstrate that the proposed method improved timing resolution from 66 ps to 5 ps and reduced the INL (integral non-linearity) from -17.7/+116.3 ps to -2.3/+1.6 ps. Under worst-case PVT conditions, the INL was further refined to -3.8/+4.1 ps. Resource utilization per TG channel was efficient, requiring only 2.9 % of Slices and 1.4 % of BRAM resources.

A High Precision Time-to-Digital Converter (TDC) based on FPGA. May 2023 - Jan 2024
Description: I developed a time-to-digital converter (TDC) for precise timing measurements in TG generation, using a multi-chain measurement averaging method to overcome intrinsic cell delay limitations and enhance resolution and RMS precision. Bin widths were verified via code density testing, and the TDC was implemented on a Xilinx `xcku060ffva1156-2-i` FPGA at a 400 MHz clock frequency. Results showed improved average resolution from 28 ps to 1.8 ps and RMS precision from 14.1 ps to 5.4 ps, with a worst-case RMS precision of 7 ps under all PVT corners. Resource utilization per TDC channel was efficient, requiring 3.7 % of CARRY8 and 3.9 % of LUT resources.

A Signal Distortion Measurement System. Nov 2021 - Dec 2021
Description: In the National Undergraduate Electronics Design Contest, I designed and implemented a signal distortion measurement system that calculates Total Harmonic Distortion (THD) and displays the results locally while also uploading them via Wi-Fi for remote monitoring. The system with the main controller MSP432P401R utilized sequential equivalent sampling and FFT algorithms to measure signal distortion, with a focus on THD and normalized amplitude. A signal generator produced input signals, and the Automatic Gain Controller (AGC) adjusted the peak-to-peak values within a range of 10mV to 800mV. Despite the 1M sampling rate limitation of the internal ADC, the system was able to measure the fifth harmonic distortion at a fundamental frequency of 500kHz with a relative error of only 3%.

An Infrared Thermal Imaging Security Inspection System based on FPGA. Nov 2020 - Dec 2020
Description: I developed an infrared thermal imaging system that captures and processes temperature array data from an infrared sensor for monitoring, alarms, and security inspections. Using a bilinear interpolation algorithm, I enhanced image resolution from 32×24 to 125×93 pixels. Frame rate was increased from 2 fps to 30 fps through FIFO-based caching of infrared frames. The system was implemented on an Altera `ep4ce10f17c8` FPGA running at 100 MHz, utilizing 56 % of LE resources and 70 % of BRAM resources.

Publications

- **Guo Z**, et al. FPGA-based process, voltage, and temperature insensitive picosecond resolution timing generators with offset correction for automatic test equipment. *Rev. Sci. Instrum.* 1 February 2025; 96 (2): 024702.
- **Guo Z**, et al. A dust sensor monitoring system using Wi-Fi mesh network. Journal of Physics: Conference Series. IOP Publishing, 2021, 1754(1): 012129.
- Dust monitoring and processing system based on Wi-Fi Mesh. CN113543058A.

Internship Experiences

FPGA Internship Engineer, Hangzhou SiGauge Technology, Beijing, China Apr 2024 – Present

Description: Contributed to the design and implementation of digital cards for ATE used in digital IC testing.Responsible for verification and implementation of timing generator, pattern stream, and calibration. Designed and implemented a 32-channel timing generator achieving a testing rate of 200 Kbps to 400 Mbps with 50 ps resolution, incorporating drive and compare functionalities. Developed the interaction logic between FPGA and DDR through FIFO to achieve 200MHz continuous pattern fetching rate from DDR by FPGA. Designed and validated channel-to-channel calibration and TDR calibration schemes for digital cards precision in ATE.

Honors & Awards

National Undergraduate Electronics Design Contest: **National Second Prize**. Dec 2021

National Undergraduate FPGA Innovation Design Competition: **National Second Prize**. Dec 2021

National Undergraduate Electronics Design Contest: **Provincial First Prize**. Oct 2020

Huazhong University of Science and Technology: **First Prize Scholarship**. Dec 2022

Wuhan University of Technology: **First Prize Scholarship**. Nov 2020

Wuhan University of Technology (three times): **Merit Student**. Nov 2019,2020,2021

Wuhan University of Technology: **Outstanding Graduate**. Jun 2022

Skills

Programming Languages: Verilog HDL, C/C++, MATLAB, Tcl, Python, Git, Shell.

Software Tools: Docker, Jenkins, Vivado, Vivado HLS, Quartus ii, Modelsim, MDK5, Altium Designer.

Languages

Mandarin (Native), English (IELTS-6.5).