ECE 343 Lab #3: Power Supply and Voltage Regulator

1 Introduction

Learning Objectives:

- Circuit design using nonlinear circuit elements
- Making and justifying design choices based on requirements
- Simulate design power supply on LTSpice
- Evaluate performance parameters and compare with design requirements
- Build a AC-DC power supply
- Solder circuit on a PCB
- Compute DC-DC conversion efficiency of three circuits voltage dividers, zener diode based on DC-DC conversion (ECE 110), power supply designed in this lab (ECE 343).
- Compare DC-DC conversion efficiency of designed voltage regulators with DC-DC conversion using a boost/buck converter (ECE 469)

Components Required:

- Breadboard
- Resistors, Capacitors: based on designs.
- Diodes: D1N750 (Zener Diode), D1N 4001/4002 (Rectifier Diodes).
- **BJT:** 2N3055, **OpAmp:** LM741

2 Introduction

In this lab we will design an AC/DC power supply. This project will be completed in three lab sessions and will call upon your knowledge of nonlinear circuit elements like diodes and the ability to make justified design choices. The design makes use of two different kinds of diodes - the basic silicon PB junction device, used as a rectifier in this case, and the zener diode, used to regulate the output DC voltage. Figure 1 shows the block diagram of a basic DC power supply.

The various components of the DC power supply are:

- Transformer: Transfers electrical energy from one circuit to another. It consists of two coils (primary and secondary) would on a magnetic core. The primary winding is connected to the 120 V (RMS) AC mains and the secondary winding is connected to the rectifier circuit.
- Diode Rectifier: The rectifier circuit converts the input AC signal V_s to a one sided signal. (Lab 2).
- **Filter:** The output of rectifier is passed through a filter block to reduce ripple in the signal.
- **Zener-diode based regulator**: Used to further reduce the ripple in the voltage and to give a stable DC output voltage.

3 Design Specifications

The power supply will be designed to meet the following specifications,

- DC open circuit output voltage is 4.7V.
- Open circuit output voltage stays within 2% of the desired voltage as AC line voltage varies from 115 V (rms) to 125 V (rms).
- Ripple voltage at output is less than 2% of open circuit output DC voltage.
- The output current can vary from 0 to 20 mA.

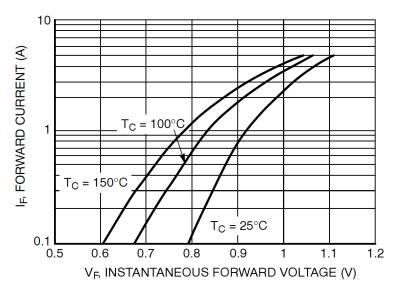
4 Design Walk-through

4.1 AC power source and rectifier

For this design we will use the sine wave source for LTSpice simulations. The actual circuit will be tested using a transformer connected to AC mains. The input sine wave to the power supply is rectified using as shown below. There are two possible rectifier: (1) Half-wave rectifier (Fig. 2 (a)) and (2) Full-wave bridge rectifier (Fig. 2 (b))

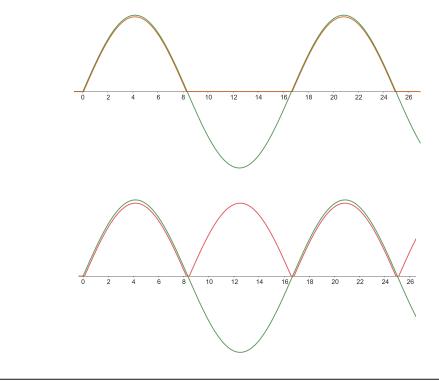
• Give a sketch of voltage across resistor $\mathbf{R_1}$ and $\mathbf{R_2}$. Assume $\mathbf{V_{in}(t)} = 25\sqrt{2}\sin(2\pi60t)\mathbf{V}$. Clearly indicate the peak value of voltage in each case.

Suppose the diode has a forward voltage of $V_{\rm F}$. The datasheet gives the following data:



So we see that the forward voltage is around 0.8-1.1V, but it could be smaller. In the LTSpice, a simulation with $R_1=R_2=1000\Omega$ gives $V_F\approx755mV$. Then the peak value of voltage is

$$\begin{split} \max(V_{R1}) &= |V_{in}| - V_F \approx \boxed{34.60V} \\ \max(V_{R2}) &= |V_{in}| - 2 \cdot V_F \approx \boxed{33.845V} \end{split}$$



• What are the advantages/disadvantages of each circuit

For the half-wave rectifier, as the name implies, you only get half of the entire waveform, which is will have a bigger ripple voltage compared to full-wave rectifier, but the peak voltage will be much closer to the peak voltage of the original waveform than a full-wave rectifier does. For whole-wave rectifier, you will get full input waveform, but your waveform will has less peak voltage when compared to half-wave rectifier, and each sine pulse in the waveform are separated by a small time gap.

• The average voltage value, $\langle \mathbf{V} \rangle$, of voltage $\mathbf{V}(\mathbf{t})$ is given by,

$$\langle \mathbf{V}
angle = rac{1}{T} \int_0^T \mathbf{V(t)} \, \mathrm{dt}$$

Compute the average value of input voltage $V_{in}(t)$, half wave rectified output $V_{R1}(t)$, and full wave rectified output $V_{R2}(t)$. You may assume the rectification is ideal and there is no voltage drop across the diodes.

By symmetry, so

$$V_{in}(t) = 0V$$

and doing the integral, we get

$$\mathbf{V_{R1}(t)} = rac{1}{\mathbf{T}} \int_0^{\mathbf{T}} \mathbf{A} \sin\!\left(rac{2\pi}{\mathbf{T}} \mathbf{t}
ight) \mathbf{dt} = -rac{\mathbf{A}}{\mathbf{T}} rac{\mathbf{T}}{2\pi} \!\cos\!\left(rac{2\pi}{\mathbf{T}} \mathbf{t}
ight)igg|_0^{\mathbf{T}/2} = rac{\mathbf{A}}{\pi} pprox \mathbf{11.254V}$$

$$\mathbf{V_{R2}(t)} = rac{1}{T} \int_0^T \mathbf{A} \sin\!\left(rac{2\pi}{T} \mathbf{t}
ight) \mathbf{dt} = -2 \cdot rac{\mathbf{A}}{T} rac{\mathbf{T}}{2\pi} \cos\!\left(rac{2\pi}{T} \mathbf{t}
ight)igg|_0^{T/2} = rac{2\mathbf{A}}{\pi} pprox 22.508 \mathrm{V}$$

4.2 Regulator

The regulator is simply a resistor and zenor-diode (Fig. 3), whose function is to hold the output voltage, V_0 , constant against variations in the load current and against variations in the AC line voltage. It also serves to reduce the ripple voltage that appears across the filter capacitor and would otherwise appear at the power supply output V_0 as well.

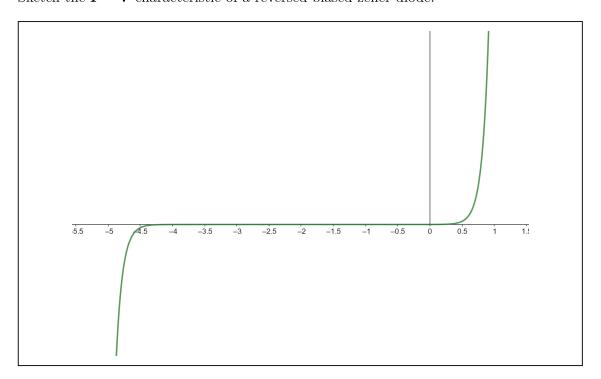
4.3 Regulator Design

The regulator design mainly involves picking an appropriate **operating point** for the zener diode. The basic configuration of regulator is show in Fig. 3. Following considerations must be kept in mind:

- 1. Too much current will cause the diode to overheat.
- 2. Too little current will cause diode to sit in flat region of the I-V curve and lose regulation.
- 3. The resistor ${\bf R_s}$ limits the maximum current that can flow through the zener diode. This condition occurs when the load current ${\bf I_L}={\bf 0}$

Answering the following question will help you design the regulator circuit:

• Sketch the I - V characteristic of a reversed biased zener diode.



Based on your sketch, give a short explanation of how reversed biased zener diode can function as a regulator. Also mention which part of the I - V curve should the diode be operated to operate as a regulator.

The zenor diode should operate in breakdown region $(V < V_Z)$. It could regulate variations in the AC line voltage V_m , as V_m changes or has fluctuations, its current will vary greatly, but according to the graph, the V will sit close to V_Z , so the output voltage is regulated. When the load current changes, its current voltage will vary greatly, but again according to the graph, the V will sit close to V_Z .

• The zener voltage V_z is fixed by the DC supply output voltage. What is the value of V_z for this design.

It should be $\overline{\mathbf{V}_{\mathbf{Z}} = 4.7 \mathrm{V}}$, as we want the DC supply voltage to be 4.7V

• The part number of zener diode used in this lab is D1N750. Refer to the device data sheet and note down the max power rating of the diode. Use 75% of the maximum power to compute the maximum current that the diode can tolerate (This condition occurs when load current $\mathbf{I_L} = \mathbf{0}$)

From the datasheet, we see that **maximum power dissipation** is 500mW. To use 75% of the maximum power, the maximum current have to be $I_{max} = (500 \text{mW} \cdot 75\%)/4.7 \text{V} = \boxed{79.79 \text{mA}}$.

• What is the value of $\mathbf{R_S}$ required to ensure that current through the diode does not exceed the maximum allowed value. Assume $\mathbf{V_m} = \mathbf{25}\sqrt{2}\mathbf{V}$.

The zenor diode will have its maximum current when $I_L=0A$. So in this case

$$\mathbf{I_Z} = \mathrm{I} = (\mathrm{V_m} - \mathrm{V_Z}) \ / \ \mathrm{R_s} \leq \mathrm{I_{max}}$$

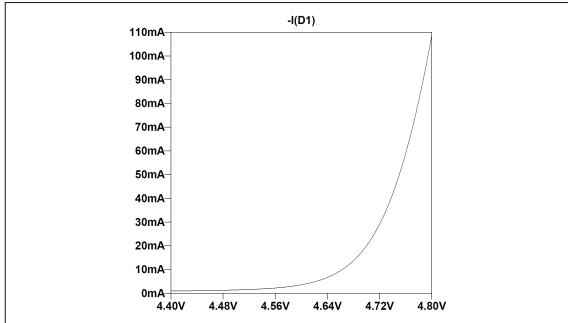
using ideal diode assumption. So

$$\mathbf{R_s} \geq rac{\mathrm{V_m} - \mathrm{V_Z}}{\mathrm{I_{max}}} pprox \boxed{384.21\Omega}$$

• The current $\mathbf{I}_{\mathbf{Z}}$ though will vary based on the load current $(\mathbf{I}_{\mathbf{L}})$ that is drawn from the regulator. What is the minimum value of current $\mathbf{I}_{\mathbf{Z}}$?

Suppose we use the I_{max} calculated when $I_L=0A$. We see that maximum I_L is 20mA, so the minimum $I_Z=79.79mA-20mA=59.79mA$.

At this point you must verify that the zener diode operates in the correct region of operation. Perform a DC sweep simulation of the circuit shown in Fig. 4. You can sweep voltage V_{in} from 4.4 - 4.8V. Plot I_Z vs V_{in} and verify that the minimum current through the zener diode is above the knee of the I_Z vs V_{in} curve.



We see that once $\mathbf{I_Z}$ is bigger than $59.79 \mathrm{mA}$, it's indeed well "above the knee" of the $\mathbf{I_Z}$ vs $\mathbf{V_{in}}$ curve.

4.4 Filter

The filter block is used to reduce the ripple in the rectifier output. The filter section is **only** a **single capacitor** connected from the output of the rectifier circuit to ground. (Fig. 6.). The following points illustrate the role of the capacitor:

- The capacitor provides current to the load between peaks of rectified output.
- Between peaks of rectified voltage, the filter capacitor is discharging at a rate that depends upon the amount of current delivered to the regulator.

• The ripple voltage, V_{ripple, C}, across the capacitor (C) can related to the value of the capacitance as follows,

$$\mathbf{V_{ripple,C}} = \frac{\mathbf{I_L}}{\mathbf{fC}}$$

where, $\mathbf{I_L}$ is the DC component of the load current and \mathbf{f} is the frequency of the filter output.

• In order to use the expression to compute C, the output ripple voltage must be converted to the ripple across capacitor.

Picking the Capacitor

Using the maximum allowable **output ripple voltage** (from the specifications), we can work backwards to the maximum allowable ripple voltage at the filter. This is done by replacing the diode by its incremental model as shown below:

Use the device data-sheet to obtain the incremental resistance of the diode

$$m R_{z,\,max} = 19\Omega$$

The actual R_z seems to be much smaller than the worst case situation, usually around 2Ω (from LTSpice simulation).

Use the maximum allowable output ripple voltage to obtain the maximum allowable ripple across the capacitor.

We therefore know that $V_{ripple,\,out} \leq 2\% \cdot 4.7V = 0.094V$, and it's obvious that

$$V_{ripple,\,out} = \frac{R_z}{R_z + R_s} \cdot V_{ripple,\,C} = \frac{19\Omega}{384.21\Omega + 19\Omega} \cdot V_{ripple,\,C} \leq 0.094V$$

and therefore

$$m V_{ripple, \, C} \leq 0.094V \cdot rac{384.21\Omega + 19\Omega}{19\Omega} pprox 1.995V$$

Compute the capacitor value. Also mention the voltage rating of the capacitor . Hint: This is obtained from the maximum voltage difference across the capacitor.

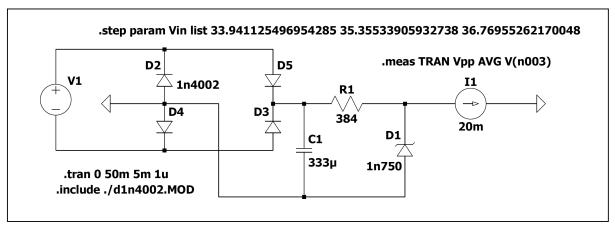
Using the formula, we know that for a half wave rectifier, the frequency f is roughly the same as the input frequency 60Hz, for a full wave rectifier, the frequency f is roughly the twice of the input frequency 120Hz. So,

$$egin{aligned} \mathbb{C}_{ ext{half}} &\geq rac{I_{ ext{L,max}}}{f \cdot V_{ ext{ripple, C}}} = rac{79.79 ext{mA}}{60 ext{Hz} \cdot 1.995 ext{V}} = \boxed{666.6 \mu ext{F}} \ \mathbb{C}_{ ext{full}} &\geq rac{I_{ ext{L,max}}}{f \cdot V_{ ext{ripple, C}}} = rac{79.79 ext{mA}}{120 ext{Hz} \cdot 1.995 ext{V}} = \boxed{333.3 \mu ext{F}} \end{aligned}$$

$$\mathbb{C}_{\mathrm{full}} \geq rac{\mathrm{I}_{\mathrm{L,max}}}{\mathrm{f} \cdot \mathrm{V}_{\mathrm{ripple,\,C}}} = rac{79.79 \mathrm{mA}}{120 \mathrm{Hz} \cdot 1.995 \mathrm{V}} = \boxed{333.3 \mu \mathrm{F}}$$

4.5 Complete Design

Sketch the complete power supply circuit (based on bridge rectifier) you have designed. Include all the components and their values. For now you can replace the transformer circuit with sinusoidal input of appropriate value.

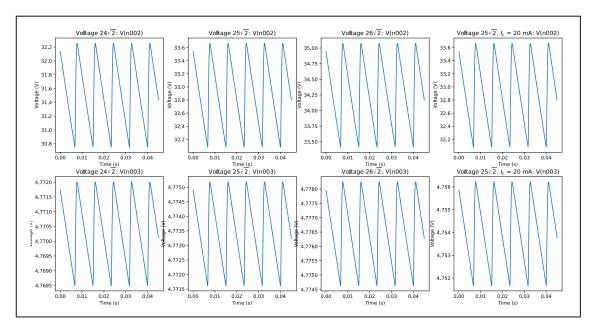


5 Simulations

• We will now verify the designed power supply using LTSpice. You are to construct the power supply and run simulations that will test the performance of the power supply over a variety of realistic situations like variable loading and dirty power.

${f V_{in}}$	$\mathbf{I_L}$	Ripple across	Output voltage	Output DC
(V)	(mA)	C (V)	ripple (mV)	voltage (V)
$24\sqrt{2}$	0	1.505	3.521	4.770
$26\sqrt{2}$	0	1.662	3.621	4.777
$25\sqrt{2}$	0	1.583	3.571	4.774
$25\sqrt{2}$	20	1.584	4.557	4.754

• Also save the output plots for each case.



6 Bench Test

Build the circuit you have tested in simulations. Complete the following table to verify its operation. **Please note:** ask your TA to verify your circuit before you test it.

${f V_{in}}$	$\mathbf{I_L}$	Ripple across C	Output voltage ripple	Output DC voltage
(V)	(mA)	(V)	(mV)	(V)
$125\sqrt{2}$	0	1.89	47.7	4.8475

7 Increasing the supply voltage

7.1 Design and Calculation

The first step is to increase the output voltage of the power supply to approximately **10V**. Consider the circuit shown below:

• Compute gain of the circuit $\mathbf{A_V} = \mathbf{V_{out}} / \mathbf{V_{in}}$ and fix the ratio $\mathbf{R_1} / \mathbf{R_2}$ to obtain $\mathbf{A_V} \approx \mathbf{2}$.

From ideal Op-Amp assumption, we have

$$\mathbf{A_V} = rac{\mathbf{V_{out}}}{\mathbf{V_{in}}} = \left(1 + rac{\mathbf{R_1}}{\mathbf{R_2}}
ight) pprox 2$$

Therefore,

$$\frac{\mathbf{R_1}}{\mathbf{R_2}} \approx 1$$

• Compute the maximum power dissipated in the resistor $\mathbf{R_1}$ and $\mathbf{R_2}$. While performing bench test of the designed circuit, the resistors you pick must be rated for this power. **Hint:** Determine the condition under which max power dissipation occurs.

If the I_{out} is 0, then the resistors will have maximum dissipated power. In this case, the power for them is

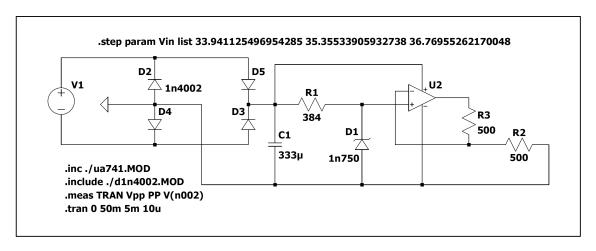
$$\mathrm{P}_{\mathrm{max},\,1} = \mathrm{P}_{\mathrm{max},\,2} = rac{\mathrm{V}_{\mathrm{out}}^2}{4\cdot\mathbf{R_1}} = rac{\mathrm{V}_{\mathrm{out}}^2}{4\cdot\mathbf{R_2}}$$

• The Op-Amp circuit shown in Fig. 9 will be used to increase the output voltage of the DC power supply you designed. The rail voltages for the Op-Amp can be taken from the terminals of filter capacitor. You must ensure that this satisfies the maximum allowed rail voltages for LM 741 IC (ref: Datasheet). Note down the maximum allowed rails voltages from the device datasheet and then justify if voltage across the plates of capacitor satisfies this requirement.

$\mathbf{V}_{\mathbf{amp,max}}$ (V)	$\mathbf{V_{c,max}}$ (V)
$\pm 22 { m V} \sim 44 { m V}$	35.36V

This should work, as the maximum voltage difference $\mathbf{V}_{\mathbf{c,max}}$ is smaller than the Op-Amp maximum.

Sketch the new circuit that includes Op-Amp in negative feedback configuration to increase the power supply output. Note: The rail voltage V₊ can be taken from the terminals of filter capacitor and V₋ can be at ground.



7.2 LTSpice Simulation

• Simulate your circuit using LTSpice. Complete the following table to verify its operation. Please Note: Ask your TA to verify your circuit before you test it.

${f V_{in}}$	$\mathbf{I_L}$	Ripple across	Output voltage	Output DC
(V)	(mA)	C (V)	ripple (mV)	voltage (V)
$24\sqrt{2}$	0	1.540	7.269	9.541
$26\sqrt{2}$	0	1.700	7.478	9.553
$25\sqrt{2}$	0	1.620	7.373	9.547
$25\sqrt{2}$	5	1.620	7.374	9.548
$25\sqrt{2}$	20	1.620	7.474	9.548
$25\sqrt{2}$	80	1.620	4.470e-5	0.184

• Is the output DC voltage maintained at the designed value for different load currents? Justify your answer. **Hint: Device Datasheet can give you a clue**

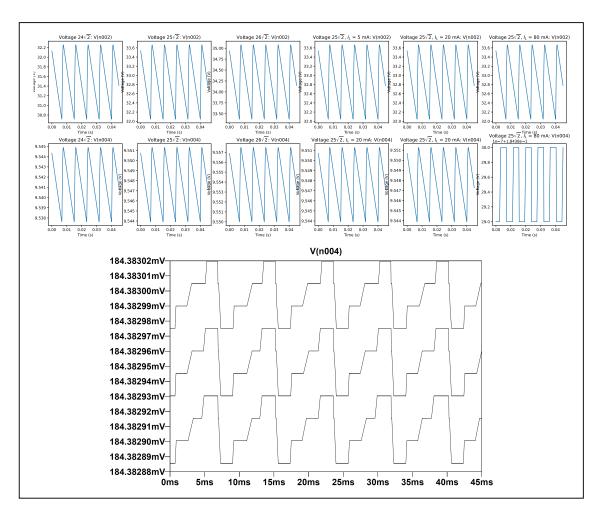
Seems like that at 80mA, the circuit fails to maintain its voltage. The datasheet said that LM741 have a maximum short circuit output current of 25mA, so it's not able to sustain 80mA output.

• Note down the maximum power dissipated by resistors ${\bf R_1}$, ${\bf R_2}$ and ${\bf R_s}$ under no load conditions and ${\bf V_{in}}=25\sqrt{2}$

$$\mathbf{R_1} = 45.58 \mathrm{mW}$$
 $\mathbf{R_2} = 45.58 \mathrm{mW}$ $\mathbf{R_s} = 2.061 \mathrm{W}$

• Save simulation plots showing DC output voltage and ripple.

Note, there is a error is y axis for last simulation in the first plot, the correct one for the last simulation is the middle trace in the second plot.



8 Increasing output current rating

8.1 Design and Calculation

In this section you will make further modifications to your circuit to meet the output current specifications of the power supply. Consider the BJT shown below:

• Give a brief explanation of how the BJT can be used to provided DC current gain

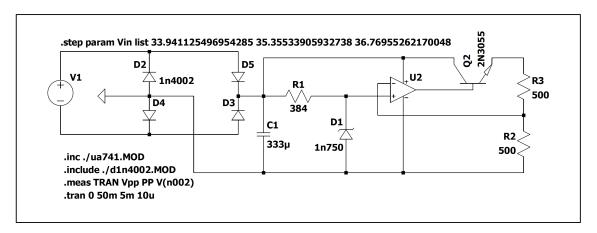
The output current $I_E = (1 + \beta)I_B$, and β is a big constant, so we see that DC current get amplified.

• Consider now the circuit shown in Fig. 11 below. Compute the maximum power dissipated by the BJT in the circuit shown in Fig. 11. Compare with the specifications in device data sheet.

P _{max, datasheet} (W)	P _{max, calculated} (W)
115W	$2.0768\mathrm{W}$

As the BJT power could be approximated as $I_E \cdot V_{CE}$ where $V_{max,\,CE} = 35.36V - 9.4V = 25.96V$, and $I_{max,\,E} = 80mA$. The calculated power is way smaller than the maximum power rating in datasheet, so we should be fine in this case.

• Sketch the complete power supply unit:



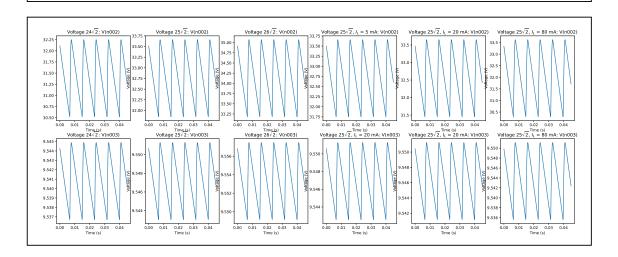
8.2 LTSpice Simulation

• Simulate your circuit using LTSpice. Complete the following table to verify its operation.

${f V_{in}}$	$\mathbf{I_L}$	Ripple across	Output voltage	Output DC
(V)	(mA)	C (V)	ripple (mV)	voltage (V)
$24\sqrt{2}$	0	1.729	8.183	9.541
$26\sqrt{2}$	0	1.888	8.329	9.553
$25\sqrt{2}$	0	1.808	8.253	9.547
$25\sqrt{2}$	5	1.906	8.712	9.547
$25\sqrt{2}$	20	2.198	10.084	9.547
$25\sqrt{2}$	80	3.326	15.509	9.544

• Note down the power dissipated by the transistor (P_T) and power delivered to the load (P_L) under maximum load conditions and $V_{in}=25\sqrt{2}V$

$$\mathrm{P_{T}} = 1.989\mathrm{W} \quad \mathrm{P_{L}} = 764\mathrm{mW}$$



9 Bench Test

Build the circuit you have tested in simulations. Complete the following table to verify its operation. Please Note: Ask your TA to verify your circuit before you test it.

$\mathbf{V_{in}}$ (V)	$\mathbf{I_L} \; (\mathrm{mA})$	Output DC voltage (V)
$115\sqrt{2}$	0	9.588
$120\sqrt{2}$	0	9.637
$125\sqrt{2}$	0	9.650

10 Soldering

Solder the DC power supply components on the PCB provided to you! Check if the soldered PCB gives the correct output.

11 DC-DC Conversion

In this section we will explore the idea of DC-DC conversion in some more detail. DC-DC conversion is an important operation in electronic circuits. The power supply in a desktop personal computer (PC) converts an AC input to a DC voltage value that is then used to power different components on the PC. Circuits also use multiple DC voltage levels. The pinout of an ATX power supply used in a PC is shown below in Fig. 12. Note that the pinouts indicate several DC voltage values. The power supply we designed can be viewed as a DC-DC converter (after the rectification step). The final regulator designed in this lab used a reference voltage of $V_{ref} = 4.7V$.

1. Consider a common method for DC-DC conversion shown in Fig. 13. The circuit in Fig. 13 is a voltage divider. Assume $\mathbf{V_1} = \mathbf{25}\sqrt{\mathbf{2}}\mathbf{V}$. Compute the efficiency η of the voltage divider circuit for the values of $\mathbf{V_{out}}$ shown in table 8. You may assume $\mathbf{R_1} = \mathbf{1k}\Omega$. $(\eta = \frac{\text{output power}}{\text{input power}})$

$\mathbf{V}_{\mathrm{out}}$	${f R_2}({f k}\Omega)$	Efficiency, η
8	292.4	22.63%
4.7	153.3	13.30%
2	59.96	5.657%

2. Consider now a circuit similar to the DC-DC conversion circuit you saw in ECE 110 (Introduction to Electronics). We designed a similar circuit in Phase 1 of this project. Compute the efficiency of the circuit shown below under full load conditions. Assume $V_{in} = 25\sqrt{2}~V,~R_1 = 375\Omega,~I_L(max) = 20mA,~V_{out} = 4.7V$

$$\eta = rac{0.02 \cdot 4.7}{(25\sqrt{2} - 4.7)^2/375} = 3.751\%$$

3. Consider the DC-DC conversion step that we implemented using the circuit shown in Fig. 15 below.

Assuming that power consumed by the transistor is the main source of power loss in the converter shown in Fig. 15, compute the efficiency of the DC regulator you designed under full load conditions ($I_L = 80mA$). Assume $V_z = 4.7V$, $R_1 = 10k\Omega$, $R_2 = 10k\Omega$, and $V_{out} = 9.54V$

$$I_E = I_L + rac{\mathrm{V_{out}}}{\mathrm{R}_1 + \mathrm{R}_2} = 80.477 \mathrm{mA}$$

$$I_C = \alpha I_E = 79.672 \mathrm{mA}$$

when taking $\alpha = 0.99$.

$$\eta = rac{80 \cdot 9.54}{79.962 \cdot (25\sqrt{2})} = 27.00\%$$

4. Consider this circuit shown in Fig. 16. The switches $\mathbf{S_1}$ and $\mathbf{S_2}$ operate in complimentary fashion. The figure also shows the switching function $\phi_1(t)$ of switch $\mathbf{S_1}$. Note that $\phi_1(t)$ is periodic with period \mathbf{T} . The switch $\mathbf{S_1}$ is turned on for a duration \mathbf{DT} during every cycle. The quantity \mathbf{D} is called duty ration and is given by

$$\mathbf{D} = rac{ ext{Time switch } \mathbf{S}_1 ext{ is on}}{\mathbf{T}}.$$

The circuit above represents the idea behind buck converter circuit that you will study in detail in ECE 464/469 (Power Electronics/Power Electronics Lab). The average value, $\langle \mathbf{V}_{\mathbf{x}} \rangle$, of voltage $\mathbf{V}_{\mathbf{x}}(\mathbf{t})$ is given by,

$$\langle \mathbf{V_x}
angle = rac{1}{\mathrm{T}} \int_0^{\mathrm{T}} \mathrm{V_x}(t) \, \mathrm{dt}.$$

Compute the value of $\langle \mathbf{V}_{\mathbf{x}} \rangle$ in terms of duty ratio **D**.

It is trivial as $\langle V_x \rangle = DV_{in}$.

5. The inductor and capacitor in Fig. 16, perform lowpass filtering on voltage $V_x(t)$. Assuming that all the components in Fig. 14 are ideal, what would be DC-DC conversion efficiency (in theory) of the converter in Fig. 16.

The response function is

$$H(\omega) = rac{1/j\omega C}{1/j\omega C + j\omega L} = rac{1}{1-\omega^2 LC}$$

Taking $\omega \to 0$, the theoretical efficiency is 100%.

6. Observe demo of the DC-DC conversion using a boost/buck converter (based on the circuit shown in Fig. 16) used in ECE 469. Note down the input power and output power of the converter, and compute the efficiency of the converter.

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The output power P = \frac{(7.6\text{V})^2}{10\Omega} = 5.776\text{W}, the input power is P = V \cdot I = 20\text{V} \cdot 0.356\text{A} = 7.12\text{W}, and so the efficiency is \eta = 5.776\text{W}/7.12\text{W} = 81.1\%.
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12 Reflections

1. What are the advantages and disadvantages of each of the DC-DC converters discussed in Section 11.

Voltage Divider: Low efficiency. Noisy. Easy to setup.

Zener Diode / OpAmp + BJT: Low efficiency, resistant to noise (reduced by Zener Diode / OpAmp feedback).

Buck Circuit: High efficiency (almost 100%). Noisy. Typically requires plenty of space to setup. (The capacitor and inductor will be really big).

2. Identify one application for each type circuit we discussed in section 11.

Voltage Divider: Digital circuit (noise doesn't matter here).

Zener Diode / OpAmp / BJT: Analog circuit (where noise does matter)

Buck Circuit: Power circuit (where efficiency matters)

3. You may have noticed several solar panels on the roof of ECE building. Some of solar panels (60 in number!) are used for research purposes. One of the goals is to use these sixty panels to supply power back to the power grid. This will require converters to be designed for each solar panel. Assuming that the goal is to transfer **21kW** of power back to power grid, which one of the converters will you pick. State your reasons. What would be the main constraint that will influence your decision? Would any additional information help you make your decision?

We need to have high current/voltage output, and we need high power efficiency. Buck converter is the best, as it has high output and high power efficiency. Addition information like that noise requirement, max current and voltage could help us to decide the capacitor and inductor we want to choose when we build the buck converter. (but it's almost certain that we need to use buck converter in this case, other options' energy loss is not acceptable, unless we have really strange requirements).

4. Figure 17 shows various components in an IPhone. Identify some analog components in Fig. 17.

Wolfson WM6180C Audio Codec.

TriQuint TQM666032, TQM667031, TQM661035 Power Amplifiers.

Infineon SMP3i SMARTi Power Management IC

5. Lithium-Ion batteries used in cell phones are rated at 3.7V. The analog components usually operate in the range 1.2V - 1.8V, depending on the process technology (65nm - 180nm). Analog components are also sensitive to noise. Would any of the methods discussed in section 11 work? Justify your answer. If none of the above methods work, propose a method that can be applied in this case.

We could use Zener diodes / OpAmp + BJT, as the analog device requires as low noise as possible. (other options all have noises).