ECE 343 Lab #4: MOSFET: Large Signal Model

1 Introduction

In this lab, we will be going over DC characterization of our first "three-terminal" device: the MOSFET. The learning objectives for this lab are:

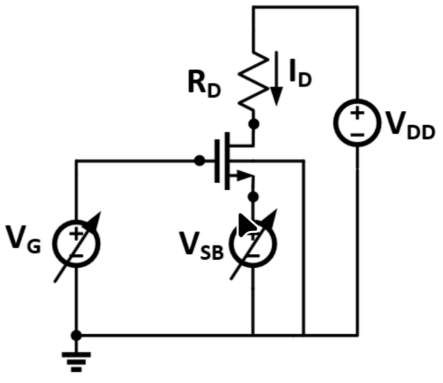
- Investigate the $\mathbf{I-V}$ curves of a MOSFET: $\mathbf{I_D}$ vs $\mathbf{V_{GS}}$ and $\mathbf{I_D}$ vs $\mathbf{V_{DS}}$
- Impact of body effect on $\mathbf{I-V}$ curves
- Obtain the values of transistor parameters: $\mathbf{V_T}$, $\mathbf{R_{on}}$, $\mathbf{k_n}$, λ
- Comparison between theory, simulation, and measurement.

2 Simulations

In this section we will perform LTspice simulations to obtain the $\mathbf{I_D - V_{GS}}$ and $\mathbf{I_D - V_{DS}}$ characteristics of a MOSFET. We will also verify the impact of body bias ($\mathbf{V_{SB}} \neq 0$) on threshold voltage $\mathbf{V_T}$. The simulation results will be used to obtain key MOSFET parameters.

2.1 $\mathbf{I_D}$ vs $\mathbf{V_{GS}}$ Characteristic

The setup for obtaining $\mathbf{I_D}$ vs $\mathbf{V_{GS}}$ is shown in Figure. 1. We have a single NMOS4 device with a series resistor in order to limit the drain current $\mathbf{I_D}$. For simulation purposes we will use a voltage source $\mathbf{V_{SB}}$, as shown in Figure. 1, to vary the body bias voltage.



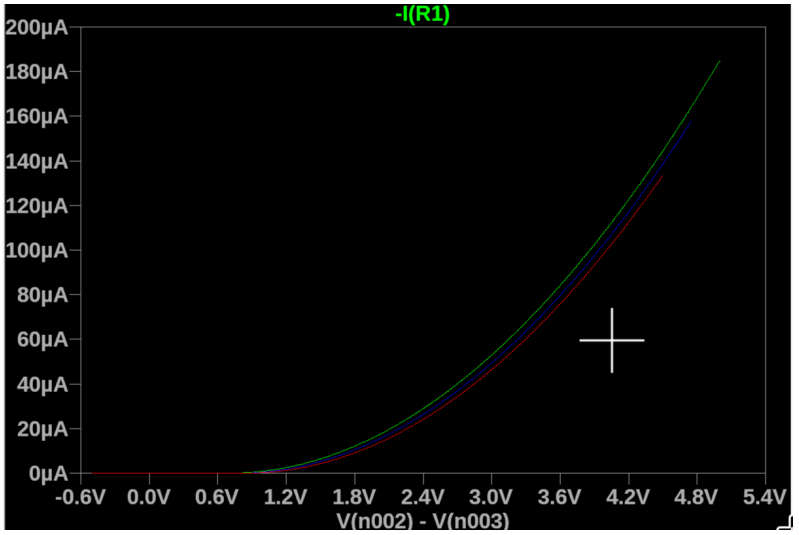
1. Draw the circuit shown in Figure. 1. Add an NMOS4 device, and use $V_{DD} = 5V$ and $R_D = 100\Omega$.
2. Define your own NMOS model (in this case called `custom`) by adding a spice directive with the text:

   ```
   .model custom nmos (vt0=0.7 gamma=0.6 phi=0.8)
   ```

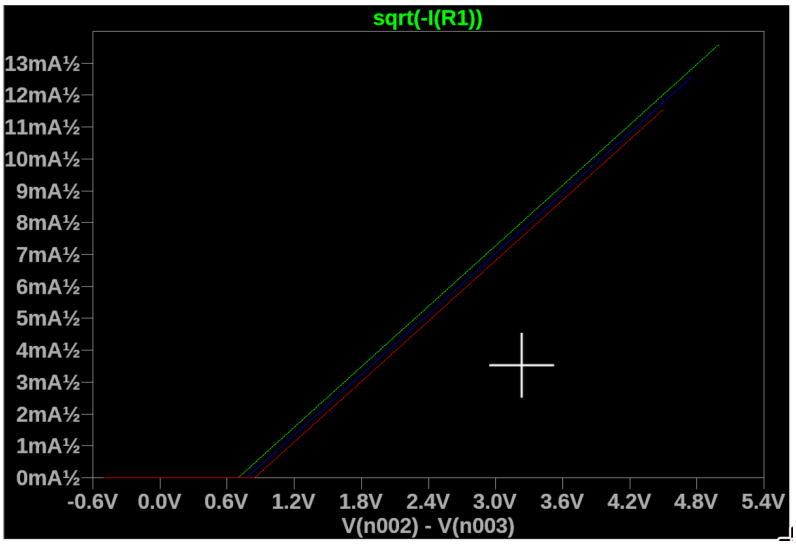
3. Right click the NMOS4 and change the model name (`custom`).

4. Perform a **DC sweep** simulation by changing the gate voltage $\mathbf{V_G}$ from $0 - 5\text{V}$ with increments of 1mV. Also perform a parametric sweep of the source-body voltage to plot all three curves on the same graph. (This could also be done with the command `.step param Vsb 0 0.5 0.25` where `Vsb` is the value of the voltage source. Refer to the tutorial for more details.)

5. Plot and save screenshots of $\mathbf{I_D}$ vs $\mathbf{V_{GS}}$ and $\mathbf{V_D}$ vs $\mathbf{V_{GS}}$. (Note: The x-axis is $\mathbf{V_{GS}}$, which is not necessarily equal to $\mathbf{V_G}$)



6. Plot and save a screenshot of $\mathbf{sqrt(I_D)}$ vs $\mathbf{V_{GS}}$. (Note: Right click the name of the window and type **sqrt**() around the name of your measurement).



7. Complete the information in Table 1. (Note: You can remove markers onto different curves by using the up or down arrow key. You can also right click the markers to view which parametric value the curve corresponds to).

Source-Body Voltage $\mathbf{V_{SB}(V)}$	Threshold Voltage $\mathbf{V_T(V)}$
0	700mV
0.25	780mV
0.50	850mV

8. Give a short explanation of the $\mathbf{V_D}$ vs $\mathbf{V_{GS}}$ plot and threshold voltage results that you obtain.

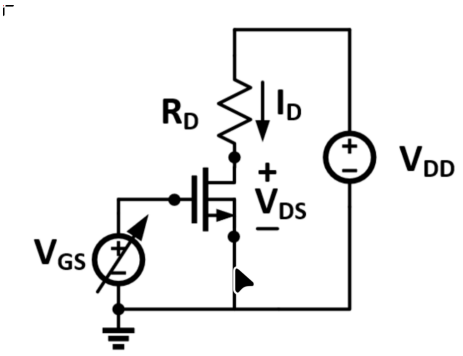
It seems that V_T actually changes. Since

$$I_D = C(V_{GS} - V_T)^2$$

bigger V_T makes the I_D smaller. So the case where V_{SB} is bigger make the V_T bigger, and therefore make I_D smaller and therefore V_D bigger (at same V_{GS}).

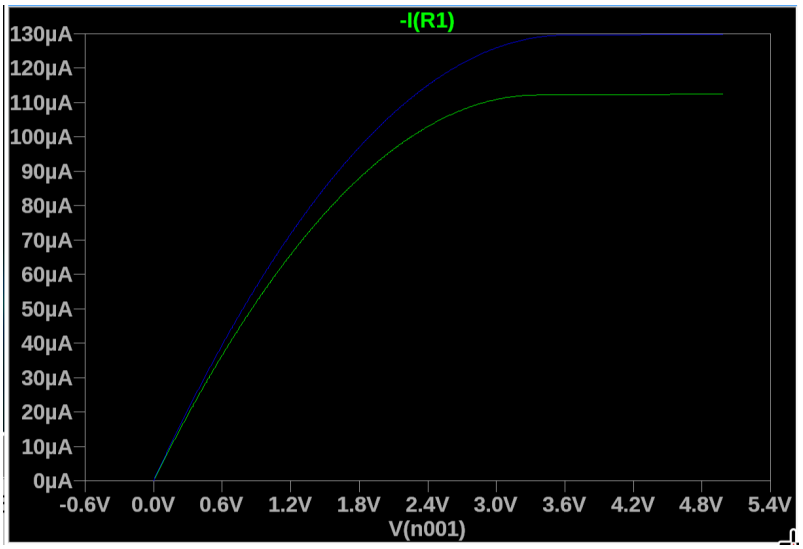
2.2 $\mathbf{I_D}$ vs $\mathbf{V_{DS}}$ Characteristic

In this section we will investigate the $\mathbf{I_D}$ vs $\mathbf{V_{DS}}$ characteristic of the MOSFET. We will use the setup shown in Figure. 2 for this purpose.



Components Values: MOSFET = NMOS4, $R_D = 510\Omega$.

1. Perform a **DC sweep** simulation by changing $\mathbf{V_{DD}}$ from $0 - 5$V with 1mV increments. Do a parametric sweep for the values of $\mathbf{V_{GS}}$ shown in Table 2 so that both curves are shown on the same plot.
2. Plot and take a screenshot of $\mathbf{I_D}$ vs $\mathbf{V_{DS}}$.



3. Complete the information in Table 2.

$\mathbf{V_{GS}(V)}$	$\mathbf{R_{on}(\Omega)}$ (Linear)	$\mathbf{R_{on}(\Omega)}$ (Saturation)	λ	$\mathbf{k_n}$
4.00V	18.9kΩ	∞	0	11.94μ
4.25V	19.753kΩ	∞	0	8.966μ

HINTS:

- λ : Channel-length modulation parameter.
- $\mathbf{k_n} = \mathbf{k_n'}\frac{\mathbf{W}}{\mathbf{L}}$: transistor transconductance parameter.
- $\mathbf{R_{on}}$ (saturation) and λ in this ideal MOSFET case is very simple since the current in saturation is constant. No need to do any complicated calculations!

- To calculate $\mathbf{k_n}$, please assume that $\mathbf{V_T = 1V}$. In addition to $\mathbf{V_T}$, you will need to use some other values from your simulation, but the equation you can use to solve for $\mathbf{k_n}$ should be one that you are very familiar with.

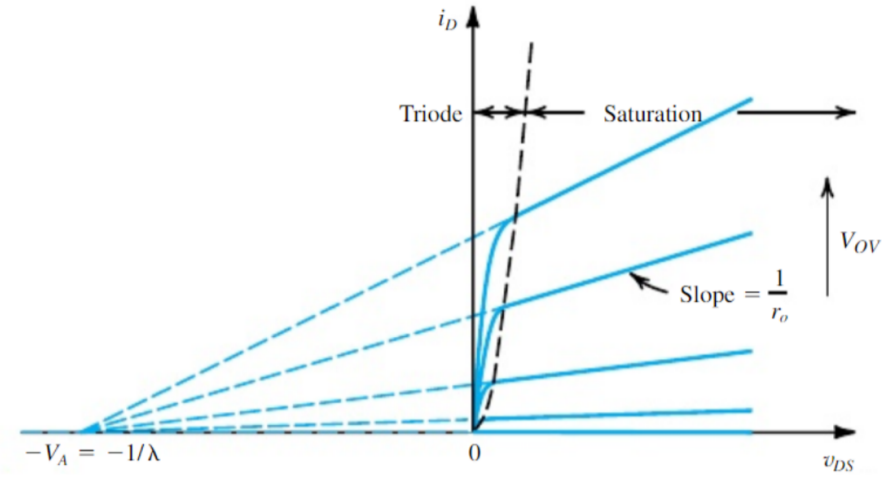


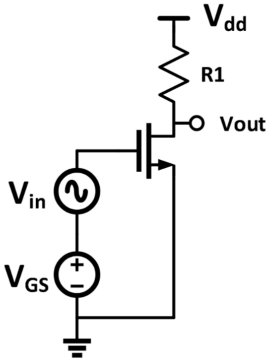
Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

4. Comment on the value of the output resistance $\mathbf{R_{on}}$ in the different regions of operation. What other factors can $\mathbf{R_{on}}$ depend on?

> $\mathbf{R_{on}}$ goes to infinite in the saturation region, while gradually increase in the linear region. (So, not *really* linear in this sense). From ECE 342 lecture notes, we also now that
>
> $$\mathrm{R_{on}} \approx \frac{1}{\mu_n C_{ox}(\mathrm{W}/\mathrm{L})(\mathrm{V_{GS}} - \mathrm{V_T})} \quad \text{if } (\mathrm{V_{GS}} - \mathrm{V_T} \gg \mathrm{V_{DS}})$$
>
> so it could also depends on the technology, or its dimensions, or the $\mathrm{V_{GS}}$

2.3 Amplifier

In this section we will investigate the impact of width-length $\mathbf{W}/\mathbf{L}$ ratio of a common source amplifier (Figure. 4) on its small signal gain and bandwidth.



Component Values: MOSFET : NMOS(BSS123), $V_{in} = 0.001\sin(100\pi t)$, $V_{dd} = 5V$, $R_1 = 1500\Omega$

1. Perform a **DC sweep** simulation to approximate the threshold voltage of the MOSFET. Save a screenshot. What is the threshold voltage?

Cutoff voltage $\mathbf{V_T}$ is around 1.25V, and saturation voltage is around 1.63V.

2. What is the role of V_{GS} and V_{in} in Figure 4.

$\mathbf{V_{GS}}$ provides DC bias, $\mathbf{V_{in}}$ is the small signal.

3. Find the small signal gain of this amplifier in terms of transconductance and load resistance.

For this circuit, $A = -G_m R_{out}$ where $G_m = g_m$ and $R_{out} = R_D \parallel r_{ds}$

4. Perform a **Transient** simulation (stop time 150 ms, maximum step 0.1 ms) to find the AC gain of the amplifier. (You have to choose a proper $\mathbf{V_{GS}}$ to bias the MOSFET in saturation region. For example $\mathbf{V_{GS}} = 1.562V$. Also, note that frequency of the sine wave is actually 50Hz.)

The input peak-to-peak is 0.002V and output peak-to-peak is 0.05917V. So the gain is about 29.585.

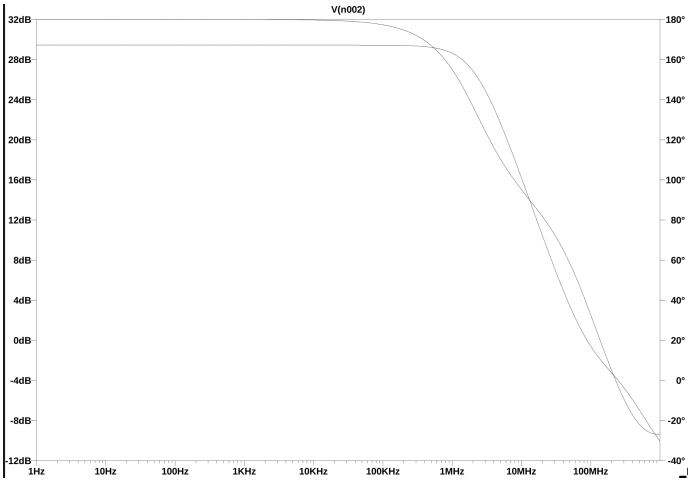
5. Add the command `options plotwinsize=0` to your schematic and run the simulation again. Select the result window and go to `View -> FFT` of $\mathbf{V_{out}}$. Note down the frequency and magnitude (in dB) of the first three peaks. What do the peaks in this plot represent?

First three peaks have frequency of 50Hz, 100Hz, and 150Hz with corresponding magnitude of -33.58dB, -83.44dB, and -139.55dB. Since we are using the MOSFET as an amplifier here, the first peak represents the amplified input sine wave, the later two peaks are noises at harmonic frequencies (but they are very small compared to the first one, and could be ignored).

6. Change the AC magnitude of the input to **50 mV** and find the FFT of $\mathbf{V_{out}}$. Note down the frequency and magnitude (in dB) of the first three peaks. How will you interpret two sets of data with different input amplitude?

> First three peaks have frequency of **50Hz**, **100Hz**, and **150Hz** with corresponding magnitude of **710.671mdB**, **−15.45dB**, and **−37.944dB**. This is amplifier, since we increase the input signal, so it is expected to see that first peak (the amplified sine wave) also get increases, the noise in the output also increases as well (the second and the third peaks)

7. Perform an **AC sweep** simulation to find the DC gain and bandwidth of the amplifier. Take a screenshot of the result.



> The DC gain is about **29.5dB**, the **3dB** bandwidth is about **1.96MHz**.

8. In order to have larger small signal gain, we can increase either transconductance of the MOSFET or load resistance in the setup. In this section, we will increase the **transconductance** and explore its impact on gain and bandwidth. Write down the formula of $\mathbf{I_D}$ and $\mathbf{g_m}$ (in terms of $\mathbf{I_D}$ and $\mathbf{V_{ov}}$). What values should you change to increase transconductance while keep operating points of the circuit fixed?

> $$\mathbf{g_m = 2 \cdot I_D / V_{ov}}$$
>
> One simple way it to just increase the $\mathbf{I_D}$, which could be done by put more NMOS in parallel to increase the $\mathbf{W/L}$.

9. Since the width-length ratio of the model we used in LTspice is fixed, we can put more NMOS in parallel to increase the width-length ration. Repeat listed procedure above to complete information in Table 3.

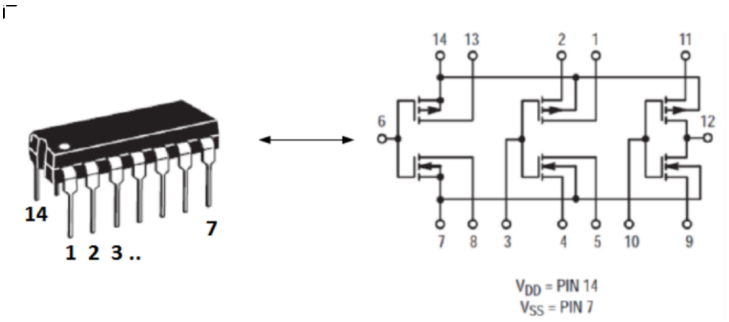
V_{GS}(V)	W/ L	I_D	g_m	A_v (gain)	Bandwidth
1.562	1X	1.310mA	0.00840	29.5dB	1.96MHz
1.518	2X	1.306mA	0.00837	30.0dB	1.18MHz
1.494	3X	1.310mA	0.00840	30.5dB	751kHz

3 Measurement Data

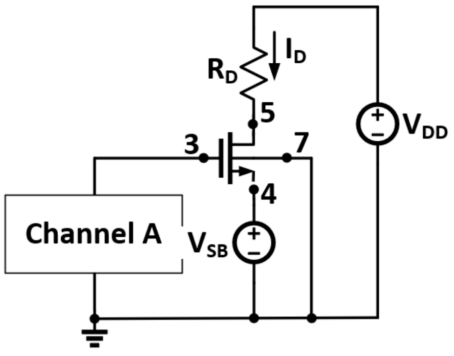
List of Components Required:

- MOSFET : CD4007UB
- Resistors: 1kΩ, 510Ω
- Potentiometer: 5kΩ

In this section we will build circuit from section 2 on a breadboard and, repeat the measurements done earlier. We will use the CD4007UB IC shown in Figure. 5 below to perform these experiments. The CD4007UB IC pins are numbered with reference to the dot on the IC in a counter-clockwise fashion as shown in Figure. 5. The figure also shows the internal structure of the IC and what each pin connection is used for.



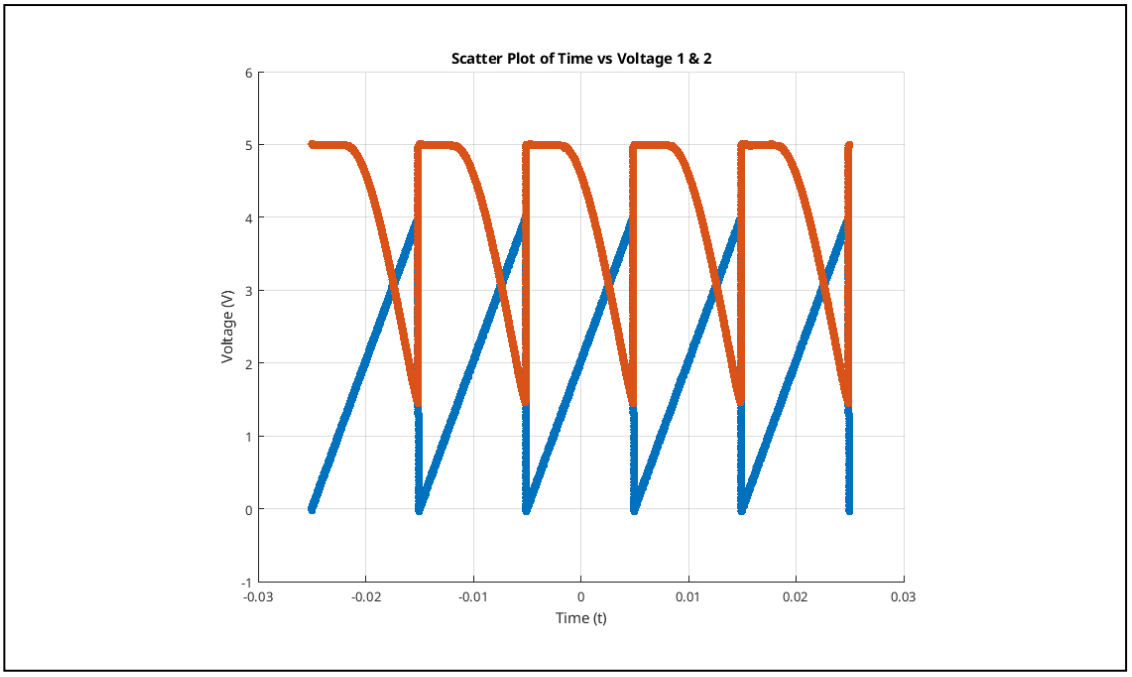
3.1 I_D vs V_{GS} Characteristic



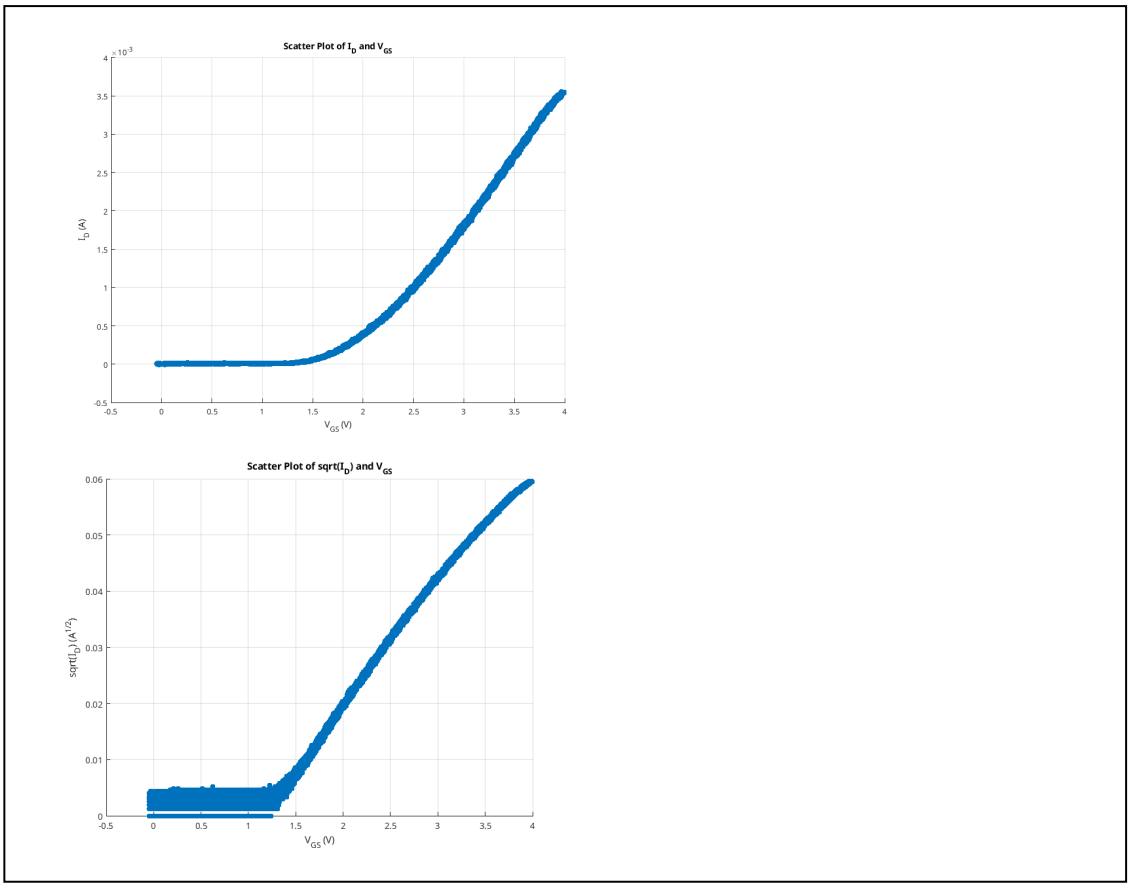
Component Values: MOSFET : CD4007UB, $V_{DD} = 5V$, $R_D = 1k\Omega$

1. Assemble the circuit shown Figure. 6 above. Use the NMOS device in CD4007UB with gate terminal at `PIN(3)` drain at `PIN(5)`, source at `PIN(4)` and body terminal at `PIN(7)`. Initially you can ground both `PIN(7)` and `PIN(4)`. Use Channel A as your input $\mathbf{V_G}$.

2. Use the 5V output pin of ADALM2000 board for $\mathbf{V_{DD}}$.
3. Use **ALICE** to generate a sawtooth waveform of amplitude $\mathbf{V_{pp}} = 4.0\text{V}$ and frequency of 100Hz on channel A. Connect Channel A to `PIN(3)` as shown in Figure. 6.
4. Ensure that `PIN(4)` and `PIN(7)` are grounded so that $\mathbf{V_{SB}} = 0\text{V}$.
5. Use Channel B to measure the voltage at `PIN(5)`
6. Take a screenshot of the output and export the data as a `.csv` file.



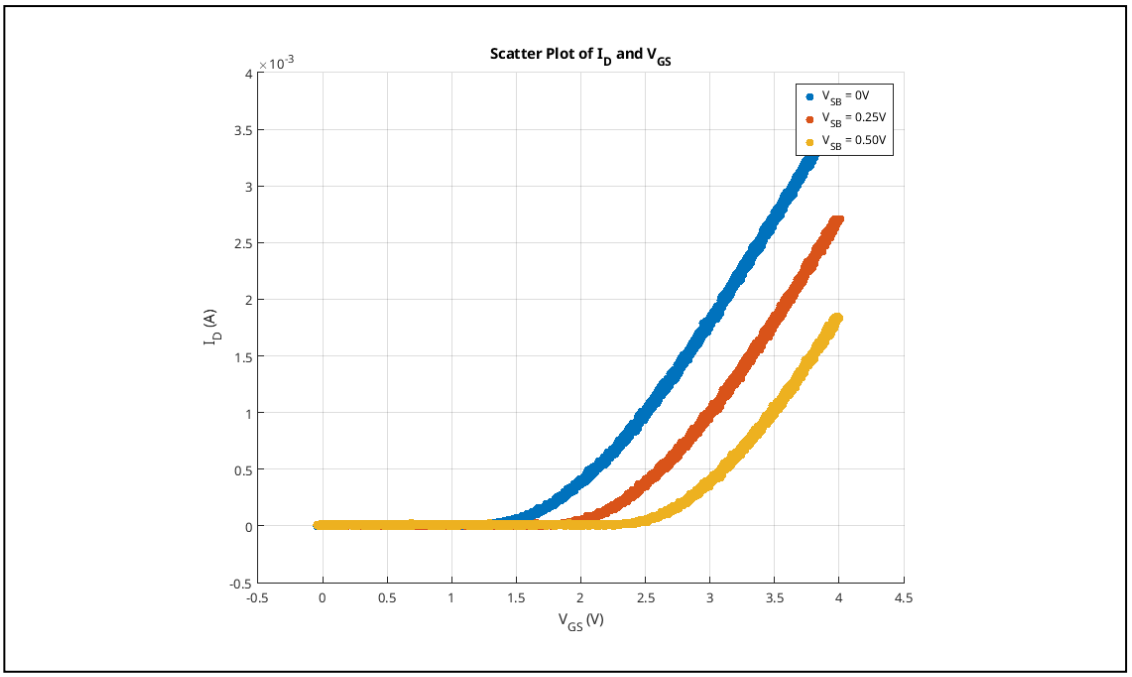
7. Use MATLAB to compute $\mathbf{I_D}$. Plot $\mathbf{I_D}$ vs $\mathbf{V_{GS}}$ and $\mathbf{sqrt(I_D)}$ vs $\mathbf{V_{GS}}$ and find the threshold voltage $\mathbf{V_T}$. (Hint: Use "scatter" to plot the graphs in MATLAB).



8. Use the 5kΩ potentiometer to generate a constant $\mathbf{V_{SB}}$ at `PIN(4)` as shown in Figure. 6. (Hint: You can generate this by using the trimpot and the 2.5V from the ADALM1000). **Alternatively**, you con generate $\mathbf{V_{SB}}$ by connecting the **Analog Output 2(`W2`)** to the source node and set **DC** voltage of your choice in the signal generator. Repeat the steps $5-7$ for $\mathbf{V_{SB} = 0.25V}$ and $\mathbf{V_{SB} = 0.5V}$. Complete the information in Table 4.

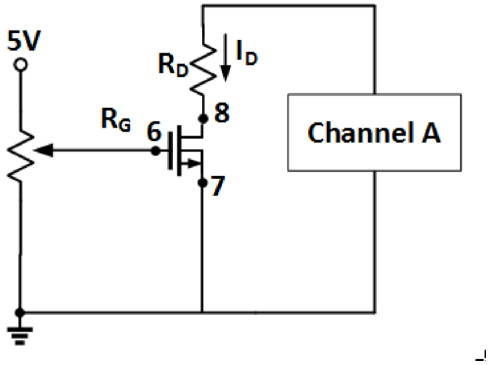
Source-Body Voltage $\mathbf{V_{SB}(V)}$	Threshold Voltage $\mathbf{V_T(V)}$
0	1.25V
0.25	1.77V
0.50	2.25V

9. Finally, plot all three curves of $\mathbf{I_D}$ vs $\mathbf{V_{GS}}$ together on one graph, and all three curves $\mathbf{sqrt(I_D)}$ vs $\mathbf{V_{GS}}$ on another. (Hint: Use the "hold on" command.)



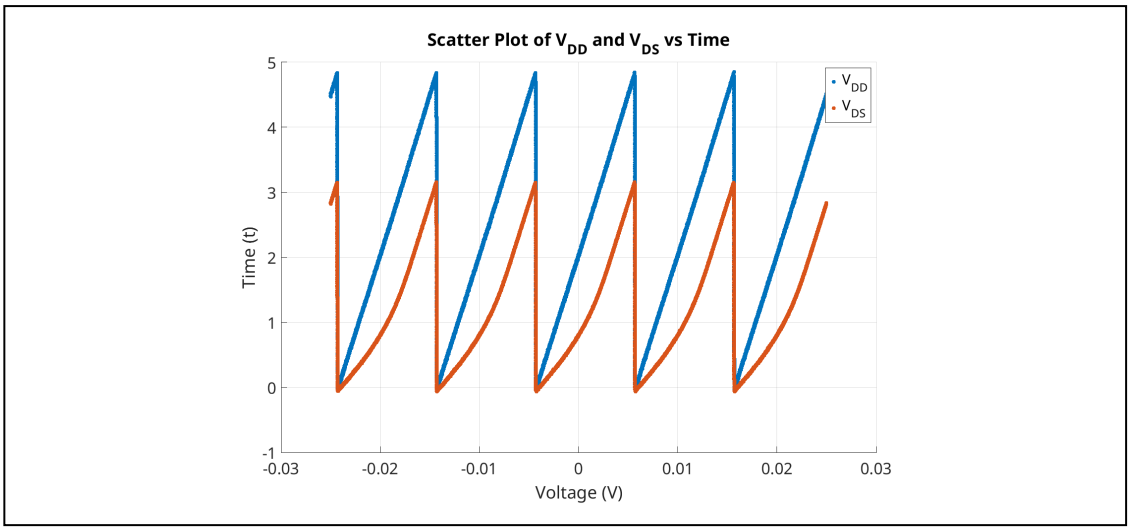
10. Keep the circuit of $\mathbf{V_{SB} = 0V}$ for demo in lab.

3.2 I_D vs V_{GS} Characteristic

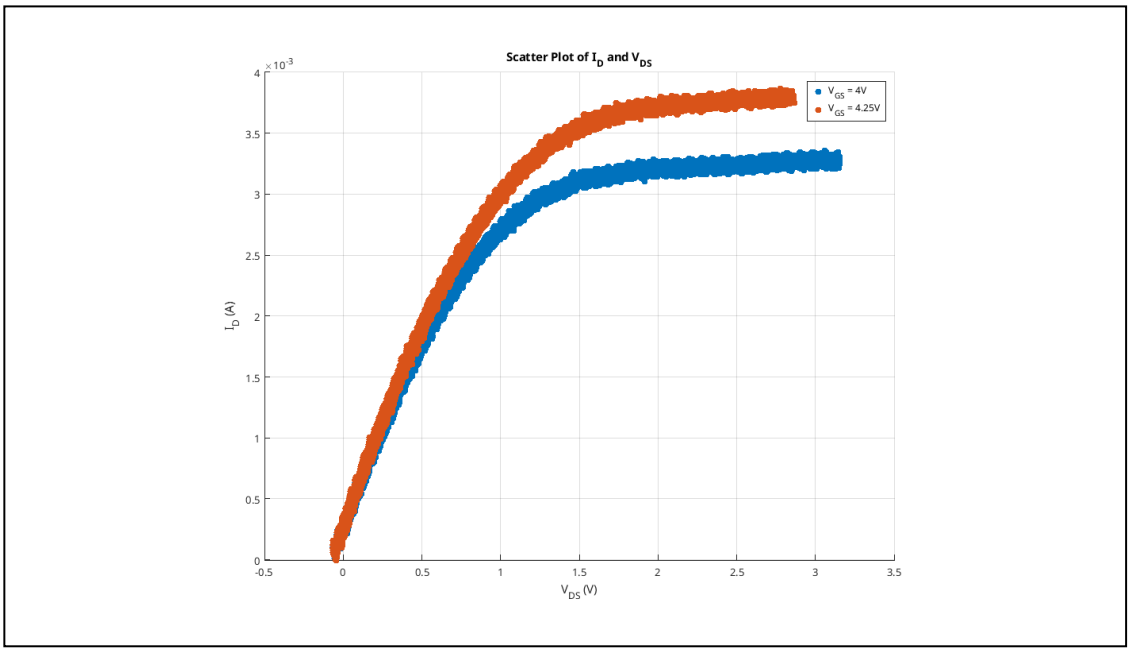


Component Values: $R_D = 510\Omega$.

1. Assemble the circuit shown Figure. 7 above. Use the NMOS device in CD4007UB with gate terminal at `PIN(6)`, drain at `PIN(8)`, source `PIN(7)`.
2. Use the 5V output pin of ADALM2000 board and a 5kΩ potentiometer to fix the gate voltage $\mathbf{V_{GS} = 4.0V}$. Again, the $\mathbf{V_{GS}}$ can be generated by **Analog Output 2(`W2`)** with arbitrary DC voltage from signal generator.
3. Use **ALICE** to generate a sawtooth waveform of amplitude $\mathbf{V_{pp} = 5V}$ with **freq = 100Hz** on Channel A.
4. Use Channel B to measure the voltage at `PIN(8)`.
5. Take a screenshot of the output and export the data to a `.csv` file.



6. Use MATLAB to compute $\mathbf{I_D}$ and plot $\mathbf{I_D}$ vs $\mathbf{V_{DS}}$.



7. Repeat the steps for $\mathbf{V_{GS} = 4.25V}$. Make sure to show both curves on the same plot.

8. Compute the information in Table 5.

9. Keep the circuit with $\mathbf{V_{GS} = 4.25V}$ for demo in lab.

$\mathbf{V_{GS}(V)}$	$\mathbf{R_{on}(\Omega)}$ (Linear)	$\mathbf{R_{on}(\Omega)}$ (Saturation)	λ	$\mathbf{k_n}$
4.00V	327.99Ω	8.793kΩ	0.0387	0.0004355
4.25V	328.68Ω	7.617kΩ	0.0383	0.0004223