Hybrid CMOS-OxRAM Image Sensor for Overexposure Control

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***Abstract*—This paper presents a first of its kind unique application of OxRAM devices in CMOS image sensor pixels. Our proposed hybrid CMOS-OxRAM pixel circuit exploits the non-linear capacitive and resistive properties of OxRAM device to control image overexposure autonomously. HfOx based OxRAM device is used as a programmable capacitive load in a conventional 4T-APS (active pixel sensor) circuit. Our solution exploiting HfOx based OxRAM devices, improves the dynamic range of individual pixels by a factor of $\sim$ 2.45 (or 7.8 dB), and capacitance density by a factor of $\sim$5 at 180 nm node.**

***Index Terms*—RRAM, OxRAM, Pixel conversion gain, Photodiode, CMOS Image Sensor, Overexposure.**

I. Introduction

CMOS image sensors (CIS) are widely used in imaging applications but have limited dynamic range. High dynamic range and high spatial resolution CIS are desirable in difficult lighting conditions. For example in surveillance, security and medical imaging applications, where objects needs to be detected in both dark- and bight- light conditions. The dynamic range of a conventional CIS is in the order of 50-70 dB [1]. Most scenes have dynamic range greater than 120 dB [2]. Dynamic range is determined by the ratio of the maximum to minimum signal that can be detected. The minimum signal level that can be detected in a CMOS image sensor is dominated by the readout circuit noise, while the maximum signal is determined by the photodiode capacitance or charge - voltage conversion node capacitance in pixel [2]. Thus to increase the dynamic range of a CIS either the noise has to be suppressed or the signal needs to be enhanced. Fig. 1, illustrates the basic concept. In CIS, incident light photons generate electron-hole pairs which are converted into a voltage and read using a Correlated Double Sampling (CDS) circuit. If the dynamic range of the sensor is low, overexposure happens and the obtained image obtained is as shown in Fig. 1b. If the dynamic range is high, overexposure is prevented and the resultant image is shown in Fig. 1c.

For CIS, relationship between the output voltage (V_{output}), integration time (t_{int}) and the photocurrent (i_{photo}) is given by [2],

$$V_{output} = Vrst - \frac{i_{photo} t_{int}}{C_{ppd}} \quad (1)$$

where $Vrst$ is known reset potential across photodiode and C_{ppd} is the photodiode capacitance. The dynamic range of a CIS can be improved by controlling the parameters in equation (1). Numerous techniques have been proposed in literature to enhance the CIS dynamic range [3], such as- (1) Logarithmic pixels; these enhance the dynamic range up to 120 dB, but suffer from high reset noise and have a low signal-to-noise ratio (SNR) [4]. (2) Capturing multiple images with varying integration time and reconstruction, however this technique limits the circuit readout speed [6]. (3) Self-adjusting integration time [5]. Solutions (1-3) considerably increase the overall sensor design complexity. From equation (1), slope of the pixel response can also be optimized by manipulating the integration capacitor C_{ppd}. Larger the value of C_{ppd}, smaller the responsivity. One such capacitance based solution relies on the use of an additional lateral overflow capacitor to drain the excess charges from the photodiode, in bright-light situations [7]. Another capacitance based solutions involves the use of bulk charge modulated device (BCMD) transistors [8] and MOS-CAP modulated conversion gain [9]. However capacitive solutions for dynamic range enhancement, increase the individual pixel size thus impacting the CIS spatial resolution.

In this paper, the trade-off between dynamic range and spatial resolution is overcome using a novel capacitive solution. The proposed solution comprises of a compact hybrid CMOS-OxRAM pixel circuit with variable conversion gain. The circuit exploits resistive and capacitive properties of HfOx-

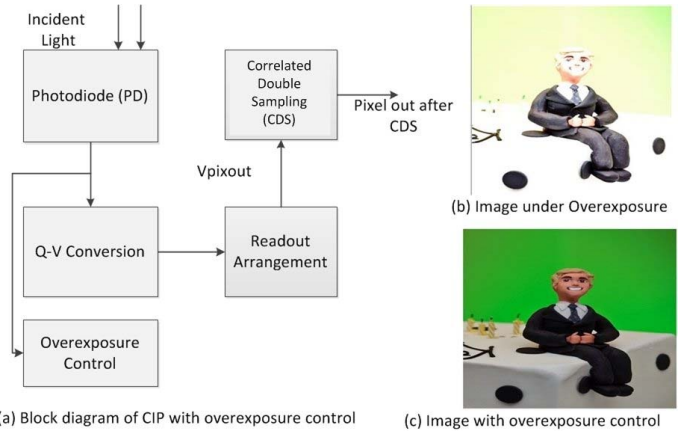

Fig. 1. (a) Block diagram of CIS pixel with overexposure control unit. Sample image obtained (a) without- and (b) with- overexposure control, respectively.

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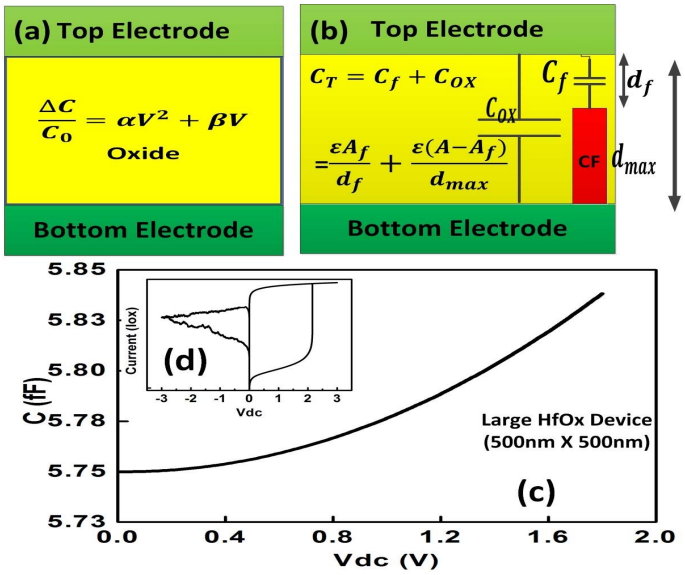

Fig. 2. (a) Two terminal MIM-type OxRAM structure, inset shows dc non-linear CV property. (b) Capacitive model (C_{OX} and C_f) in case of non-zero filament length. (c) C versus dc bias (V) for Pt/HfO2/TiN stack. (HfOx thickness = 10 nm, electrode dimensions = 500 nm X 500 nm.

OxRAM (Oxide based resistive RAM) device, to vary pixel conversion gain for dim- and bright- light situations. There are several merits of using OxRAM device in the proposed application over conventional capacitive solutions such as - (a) high-integration density/possibility of 3D integration, (b) low-cost of fabrication [10], (c) programmable resistance and capacitance states, (d) high capacitive density [11], and (e) full CMOS compatibility. These properties offer the possibility of designing giga-scale pixels economically with enhanced dynamic range without significantly compromising CIS spatial resolution. Section II discusses OxRAM basics and its capacitve attributes. Section III outlines the working of our proposed hybrid CMOS-OxRAM pixel circuit and discusses the simulation results. Conclusions are presented in section IV.

II. OxRAM as Capacitive Device

OxRAM (or ReRAM or RRAM or even the theoretical Memristor) is a two-terminal MIM-type (metal-insulator-metal) structure sandwiching a thin active insulating oxide layer, between two metallic electrodes as shown in Fig. 2(a). The active layer exhibits reversible non-volatile resistive switching behavior on application of appropriate programming current/voltage across the device terminals. Formation of a conductive filament (comprising of oxygen vacancies and defects) in the active layer, switches the device to a low resistance (LRS/On) SET-state, while rupturing of the conductive filament (CF) switches the device in a high-resistance (HRS/Off) RESET-state [10]. Resistive behavior of OxRAM devices has been well characterized [10], modelled [12], [13] and studied in detail in literature for several different "high-k" stacks such as HfOx, TaOx etc. Characteristic OxRAM I-V curves and resistance programmability has been widely proposed for use in applications such as non-volatile storage, neuromorphic computing [14], machine-learning [15] and embedded design [16].

However, not much work has gone in studying and exploiting the capacitive behavior of OxRAM devices either for memory or non-memory applications. OxRAM devices mainly exhibit capacitive properties owing to their MIM-type structure. Effective OxRAM capacitance can be computed for two different situations (a) when device is hard-RESET (with zero or negligible CF height, Fig. 2a), and (b) when device is soft-RESET (finite CF height, Fig. 2b). In case of soft-RESET, the effective capacitance (Cox + C_f) is computed using the equation shown in inset of Fig. 2b, where A is total device area and A_f is effective cross section area of the CF. Experimentally, Cox has been shown to have a nonlinear dependence on applied voltage [11], [17], [18], described by relationship (2).

$$\frac{\Delta C}{C_0} = \alpha V^2 + \beta V \tag{2}$$

where, $\Delta C = C(V) - C_0$, C_0 being the OxRAM capacitance at 0 V dc bias, and $C(V)$ the capacitance at any applied dc bias V; α and β are the quadratic- and linear-CV linearity coefficients, respectively. Both depend on material, oxide thickness and process related parameters such as deposition technique and temperature. The dc CV non-linearity is believed to arise from intrinsic factors such as traps near the oxide-metal interface, and space charge region based electrode polarization [18]. For validating the proposed overexposure control application detailed in Sec.III, we chose pt/HfO_2/TiN OxRAM device stack due to following reasons- (a) high capacitance density ($\sim 22\ fF/\mu m^2$), (b) availability of strong compact model [19] for circuit simulations, (c) ample resistive/capacitive characterization data (d) low leakage current and (e) optimum CV linearity coefficients. For 10nm HfOx device, $\alpha \sim 4840\ ppm/V^2$ and $\beta \sim -290\ ppm/V$ [17]. From eq. (2) and Fig. 2c, it is clear that $C(V) > C_0$ for $V_{dc} > 0V$ and only if $V_{dc} < V_{set}$. For the proposed circuit in Sec.III and all simulations in this paper, we chose a large electrode area (500nm X 500nm) device with a 10nm thick HfOx layer, as it could offer an initial capacitance of $\sim$ 5.75 fF. Fig. 2(d) shows the simulated I-V characteristics of this large device (set voltage $\sim$ 2.3 V), which we obtained using the 2D compact model described in [19]. Fig. 2(c) shows the non-linear capacitance characteristics for the same device, obtained by plotting eq. (2) with a voltage sweep from 0 to 1.8 V. For the overexposure control application, since we wanted to exploit the CV non-linearity, it made sense to operate the device as a variable capacitor in the hard-RESET state (Fig. 2a). Having no CF, increases the range of voltage points for which the capacitance can be manipulated in order to adapt the dynamic range of the pixel. Operating the OxRAM as a variable capacitor in soft-RESET, limits the range of attainable capacitance values along with the risk of shunting the device by an accidental SET-operation.

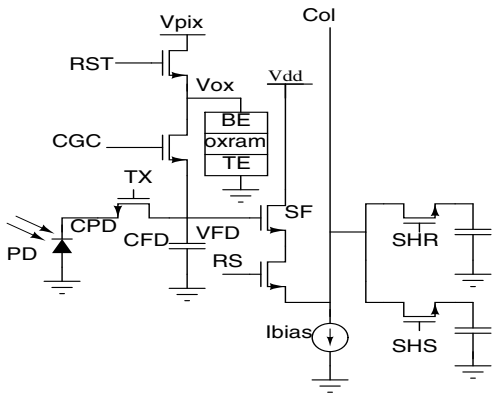

Fig. 3. Proposed hybrid CMOS-OxRAM pixel for overexposure control simulated at 180 nm node.

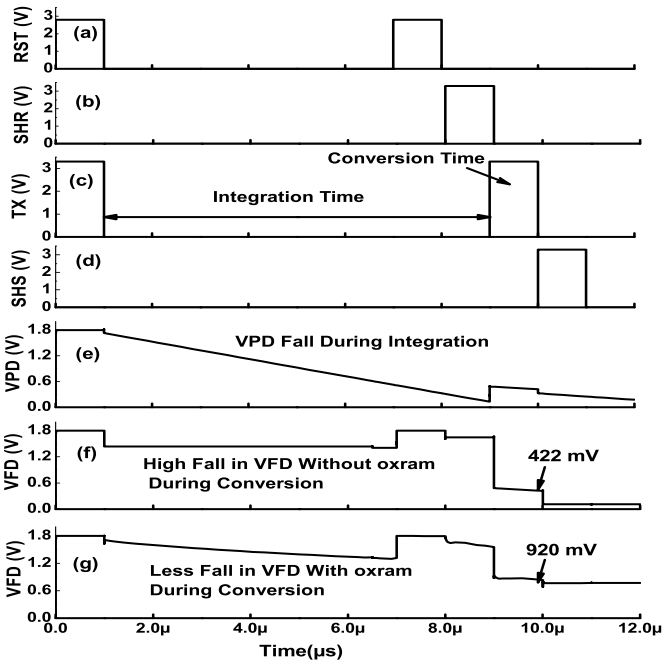

Fig. 4. Time-line for 1-full overexposure control cycle in bright-light stimuli.(a) Reset (b) Sample Hold Reset (c) Transfer Gate (d) Sample Hold Signal. Evolution of- (e) PD potential, (f) VFD (without OxRAM) and (g) VFD with OxRAM.

III. Our proposed hybrid CMOS-OxRAM pixel circuit for overexposure control

Fig. 3 shows our proposed solution where a HfOx based OxRAM device is connected in parallel to the floating diffusion node (VFD) of a typical 4-T CMOS pixel circuit. A transistor, called the conversion gain control switch (CGC), is used to connect or disconnect the OxRAM to the node VFD. In normal or dim-light stimuli, CGC is OFF, keeping the OxRAM disconnected from the node VFD. However in bright-light stimuli (i.e. overexposure), the incident light intensity exceeds a certain threshold, CGC is turned ON, and OxRAM is connected to the VFD node. When the OxRAM is connected to VFD node, the OxRAM capacitance (Cox, due to its MIM structure) is actually in parallel to CFD (i.e floating diffusion capacitor of the 4-T pixel circuit). This leads to a larger effective capacitance (C_{Total} = Cox + CFD) in parallel to the photodiode capacitance (CPD). A larger capacitance in parallel to CPD would enable the pixel circuit to assimilate the large amount of charge generated in bright-light situation through improved charge sharing. This leads to a reduction in the overall conversion gain of the pixel at VFD node, thus controlling the overexposure.

For all simulations, CPD = 8 fF, CFD = 1.15 fF and UMC 180 nm node design kit were used. OxRAM dimensions (as described in Sec.II) were chosen in such a way that a hard-RESET Cox (5.75 fF) = 5 times the value of CFD for effective overexposure control.

Timing diagram of our proposed CMOS-OxRAM pixel circuit for one full overexposure control cycle is shown in Fig. 4. OxRAM device is initialized by a hard-RESET condition. The overexposure control operation starts by resetting the photodiode (PD) and floating diffusion node (VFD) to a fixed potential (Vpix) by asserting the RST and TX signals as shown in Fig. 4(a), (c) respectively. CGC is already ON as it is the case for bright-light stimuli and will remain ON for complete overexposure control cycle. Light integration process starts just after resetting the PD. Incident light generates electron-hole pairs in the depletion region of the PD. Accumulation of charge leads to a continuous fall in PD potential (VPD) during integration time (see Fig. 4e), as electrons are collected on the n-side of PD due to direction of the internal electric field in the depletion region. RST is asserted at 7 μs just before asserting the SHR to refresh the VFD potential.

After the integration time, TX is again pulsed high as shown in Fig. 4(c), allowing the transfer of integrated charges from PD to a parallel combination of CFD and Cox. Fig. 4(f) shows the impact of charge transfer on the VFD under bright-light situation, if there is no OxRAM in the circuit. While Fig. 4(g) shows the impact when the circuit contains an OxRAM device. Clearly, the fall in VFD is less drastic in the case when OxRAM is present. The difference in VFD values for the two cases at the end of conversion time (t = 10 μs) is $\sim$500 mV. Steep fall in VFD is undesired as it may lead to an undetectable VFD signal at the SF stage.

Fig. 5 shows the evolution of OxRAM capacitance and resistance for the complete duration of operation. The OxRAM doesn't switch during entire overexposure control cycle and remains in the hard-RESET state (Fig. 5d). However, Cox changes (Fig. 5b) according to CV non-linearity explained in Sec.II (eq.2). We basically exploit the HfOx CV non-linearity to induce a volatile increase in Cox, which otherwise is obtainable only by increasing the OxRAM device dimensions. An optimal set of α and β values, by engineering the material properties of the active oxide layer, would ensure sufficient increase in Cox due to non-linear CV and a non-steep fall in VFD during conversion time, both of which may act as inherent trade-offs arisig from eq.2. Impact of charge flux (PD to CFD) on VFD, during conversion time (Fig. 4(c)),

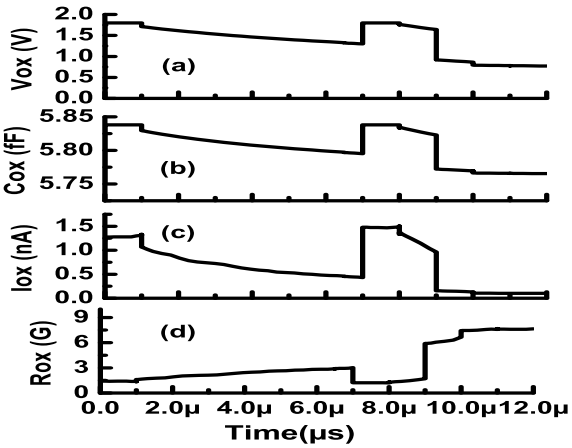

Fig. 5. (a) Voltage (b) Capacitance (c) Current and (d) Resistance evolution of the HfOx OxRAM device for one full overexposure control cycle.

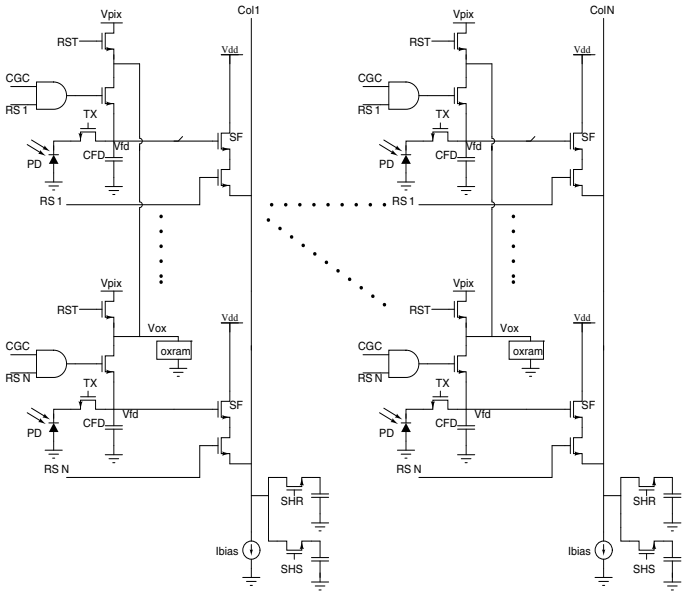

Fig. 6. NxN CIP array with hybrid CMOS-OxRAM pixels. One OxRAM per column is used.

is dependent on the coversion gain (μV/e^-),

$$Conversion\ Gain\ (CG) = \frac{q}{C_{Total}} \tag{3}$$

where q is charge of a single electron. Hence, a large C_{Total} leads to a lower CG. In the case, when OxRAM is included in the circuit, CG decreases by a factor of 6.05. Dynamic range (DR), of the pixel, is inversely proportional to $\sqrt{CG}$ [2]. Thus, addition of OxRAM improves the DR by a factor of 2.45 (or 7.8 dB), compared to the case without an OxRAM.

The row select (RS) transistor connects the pixel output to the column bus. The column circuit consists of a Correlated Double Sampling (CDS) circuit, where column outputs are stored on sampling capacitors as shown in Fig. 4(b), (d) during both the sample hold reset (SHR) control and the sample hold signal (SHS) control signal. The CDS circuit eliminates kTC noise, which contributes significantly to the sensors noise floor [2]. After CDS, difference between reset-signal and the sampled-signal is computed. The difference signal represents the amount of light integrated and thus the digital representation of this signal gives the gray scale intensity level of the pixel.

NxN pixel array of hybrid CMOS-OxRAM pixels is shown in Fig. 6. CIS pixels are read progressively, one row is read at a given time. Thus single OxRAM device can be used for all pixels in a given column. For pixel readout, the corresponding row select (RS) signal is asserted. Asserting the CGC signal enables overexposure control as it connects the OxRAM in parallel to CFD.

IV. Conclusion

In this paper we present and analyze a novel hybrid CMOS-OxRAM pixel circuit. In our proposed solution, we exploit the non-linear capacitive properties of HfOx based OxRAM device to autonomously control image overexposure in bright-light situations. Dynamic range of the pixel is improved by a factor of ~ 2.45. Optimizing the OxRAM non-linear parabolic CV curve by material engineering can further improve the pixel dynamic range, even without scaling up the lateral device electrode dimensions. Our solution is highly scalable as single OxRAM device can be shared across entire coloumn bus. The proposed application looks beyond conventional storage, and more recently proposed computing applications of emerging non-volatile OxRAM devices. It opens new doors in a commercially relevant space that includes: difficult-lighting, giga/mega-pixel, security, surveillence, and medical- imaging applications.

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