



上海交通大学
SHANGHAI JIAO TONG UNIVERSITY



集成电路工艺原理

Fundamental Principles of Integrated Circuit Fabrication

第1周 --- 第8周
星期二 第1节--第2节
星期四 第7节--第8节
东下院402

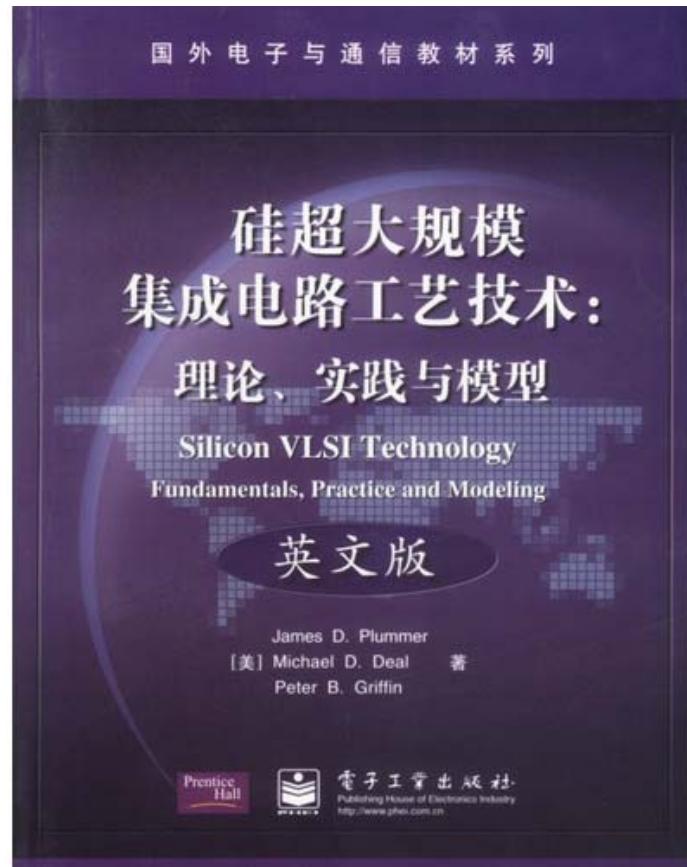


教材

硅超大规模集成电路工艺技术：理论、实践与模型

Silicon VLSI Technology
Fundamentals, Practice and
Modeling

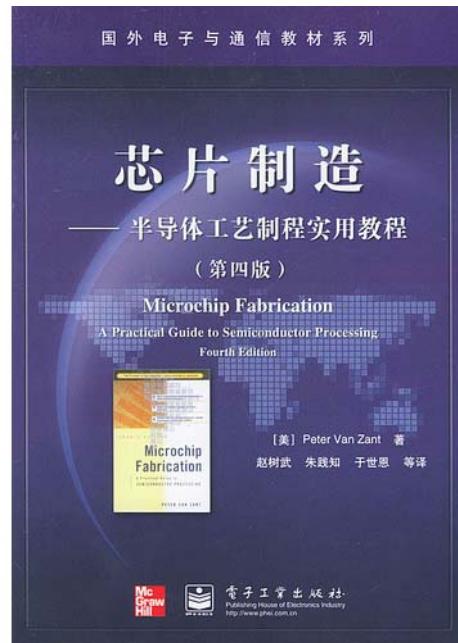
(美) 普卢默 等著
电子工业出版社



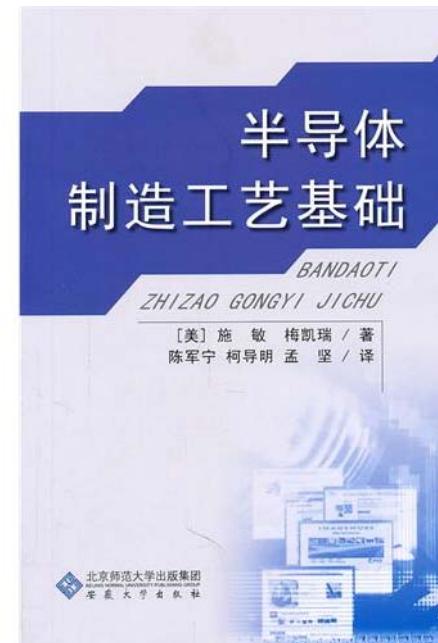
参考书



(美) 夸克 等著
2006年06月
电子工业出版社



(美) 赞特 著
2004年10月
电子工业出版社



(美) 施敏, 梅凯瑞 著
2007年04月
安徽大学出版社

课程内容

本课程是电子科学技术专业的**理论基础课**。本课程将以硅基超大规模集成电路（**Silicon VLSI**）作为讨论分析对象，主要围绕现代**集成电路制造的基础工艺**，重点介绍与微电子技术相关的器件和集成电路的制造工艺原理和技术，通过本课程的学习，期望学生能掌握**集成电路核心工艺流程及关键制造技术的基本原理**，包括氧化、扩散、离子注入、薄膜淀积、光刻、刻蚀、金属化工艺以及工艺集成等内容,为集成电路与系统的设计和制造打好必要的IC技术的理论基础。

先修课程及考试

- 先修课程
 - 半导体物理学，半导体器件基础等相关课程
- 考核及成绩评定方式
 - 平时作业：30%
 - 考试：70%。主要考核对本课程内容的基本原理和技术的掌握程度
(开卷)

教学纲要

教学内容	课堂教学	讨论	作业及要求
一般情况和历史演变	2学时	课堂教学中融入讨论	每几次课后有课外作业
整体流程设计	2学时		
环境要求、材料要求	6学时		
单项工艺	20学时		
总结与复习	2学时		

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请提供邮箱地址，平时作业及课件群发给大家。

上课前打印课件，做好笔记

硅光子技术

硅光子器件是下一代光网络和计算机发展的关键支撑技术

■ 光通信领域

- 全光信息处理
- 提高网络节点信息处理能力

电子处理能力有限，将严重制约
网络性能的提升



■ 计算机领域

- 芯片内和芯片间光互连
- 延续摩尔定律

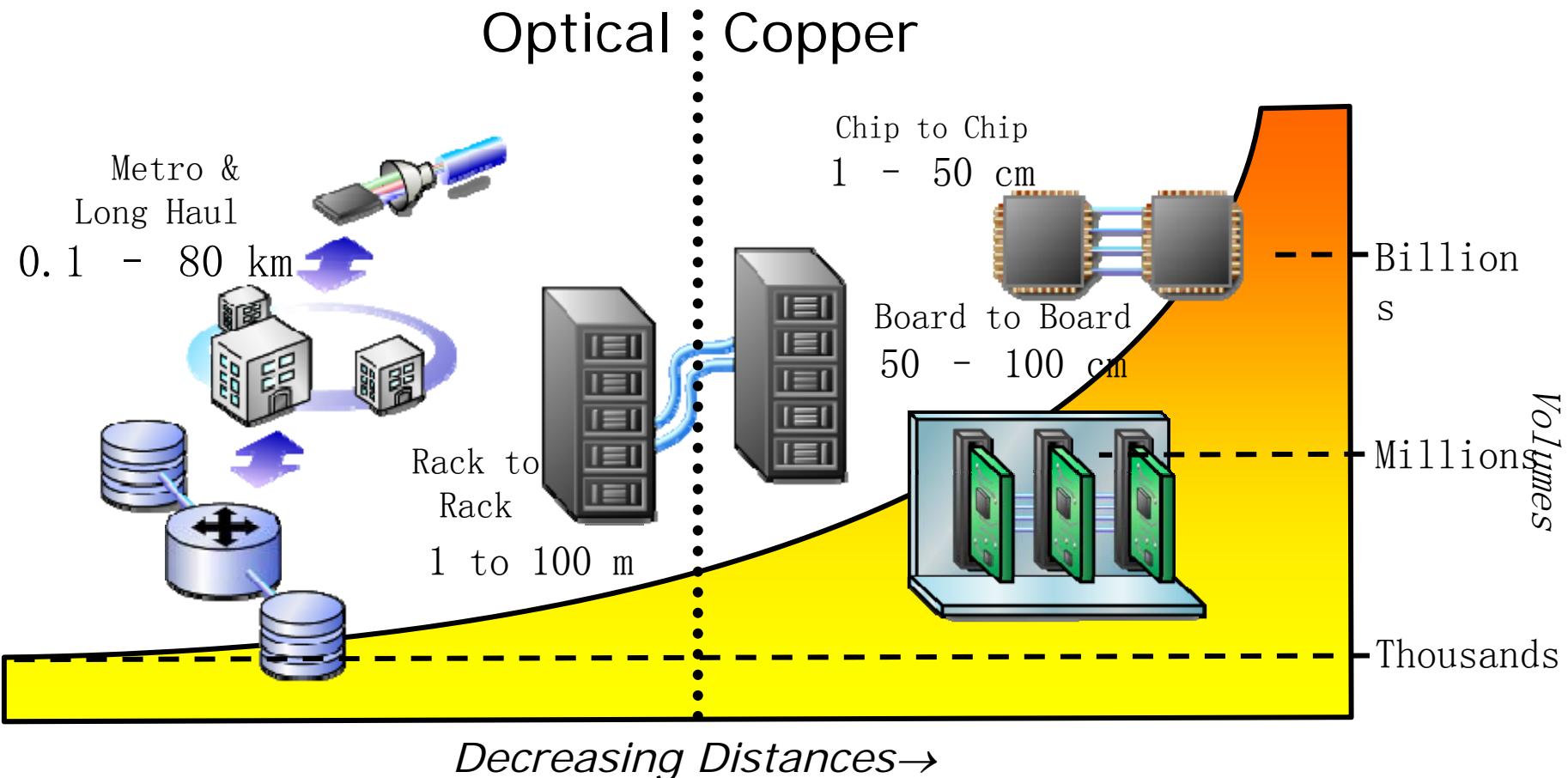
金属互连线延时和功耗大，
成为计算机性能提高的瓶颈



硅光子学

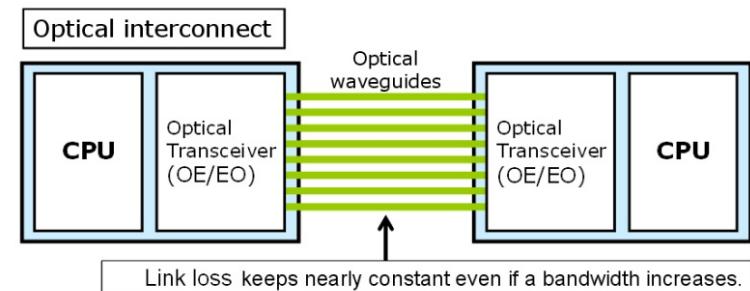
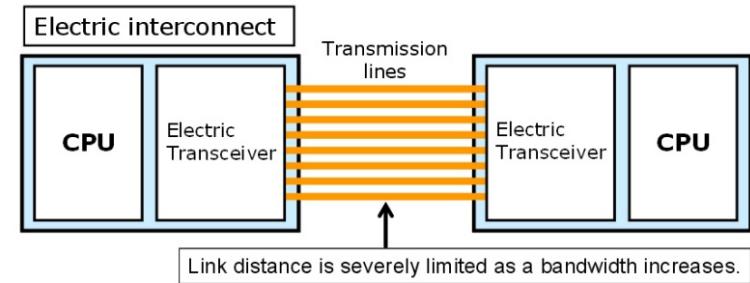
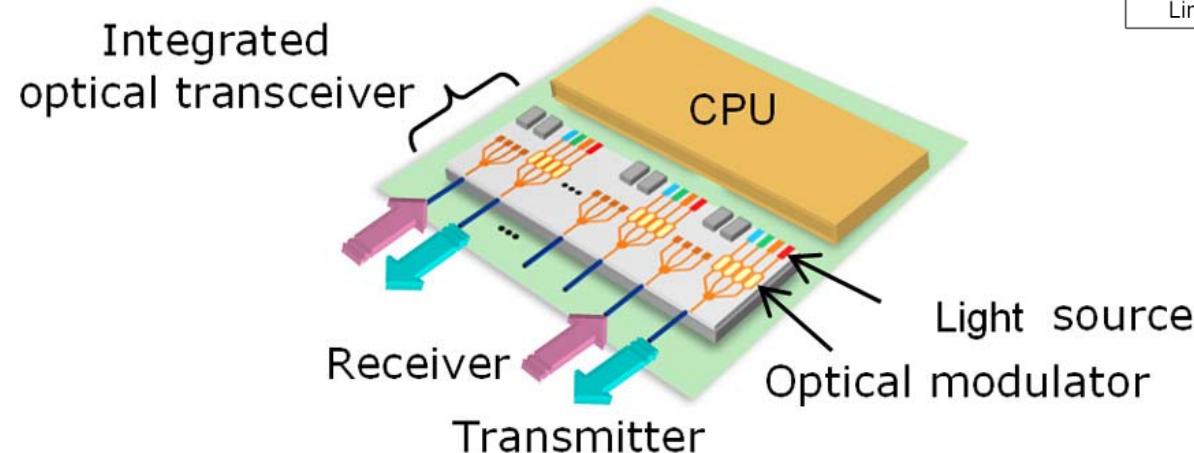
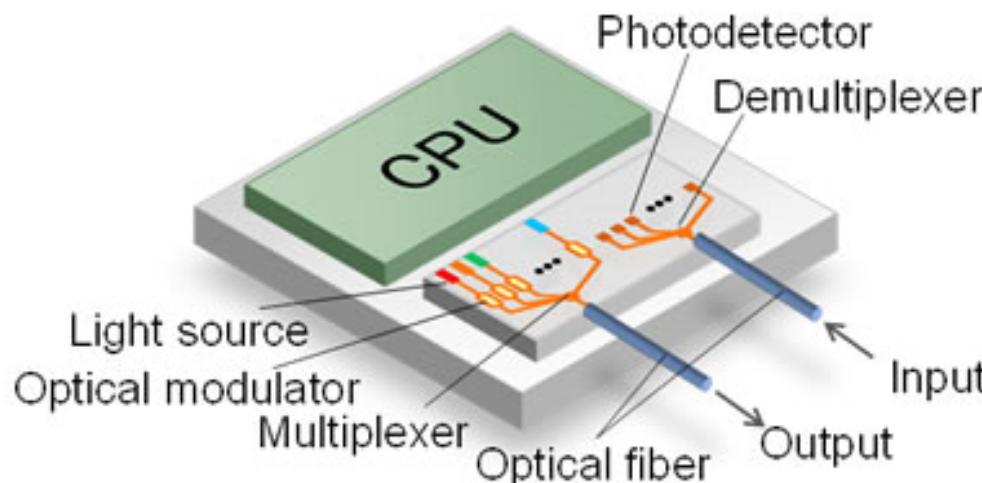
- 国际前沿学科 (DARPA、IBM、Intel)
- 列入973、重大专项等计划
- 上海市重大基础研究

Today's High Speed Interconnects



Goal: Drive optical to high volumes and low costs

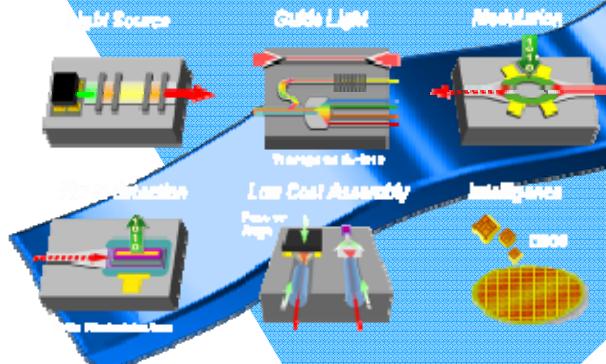
Optical interconnect



Integration vision

Time →

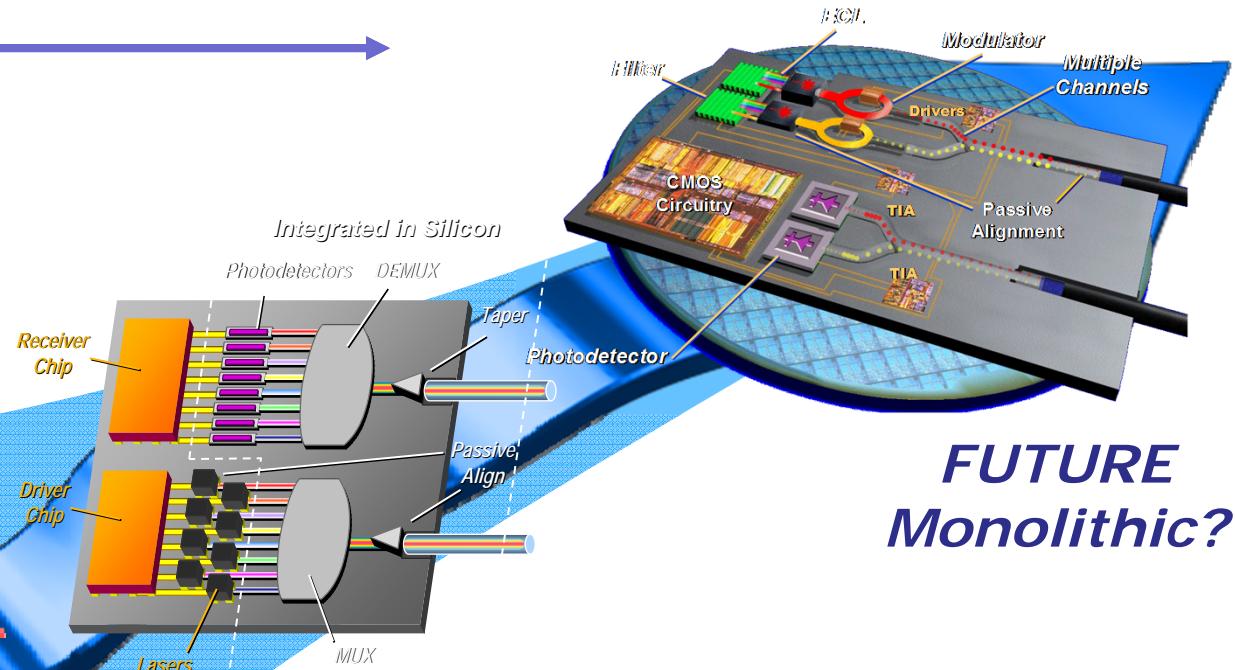
TODAY
*Device level –
Prove silicon
viable*



*Integrate silicon devices
into hybrid modules*

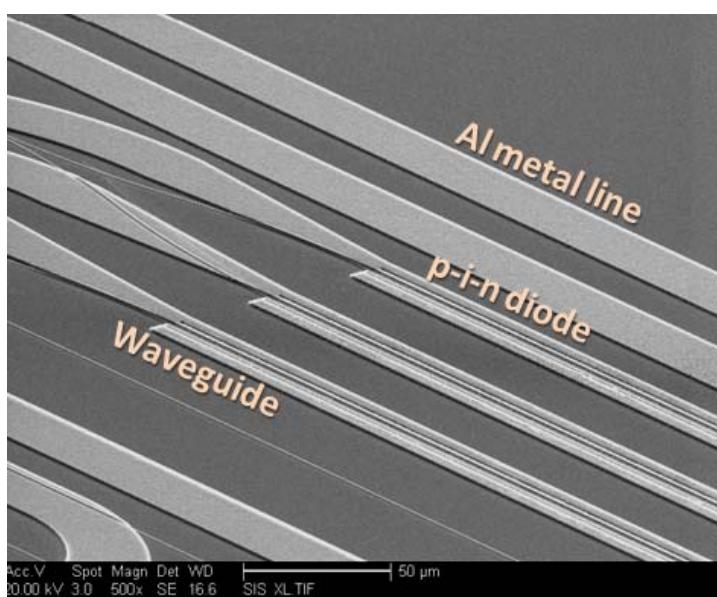
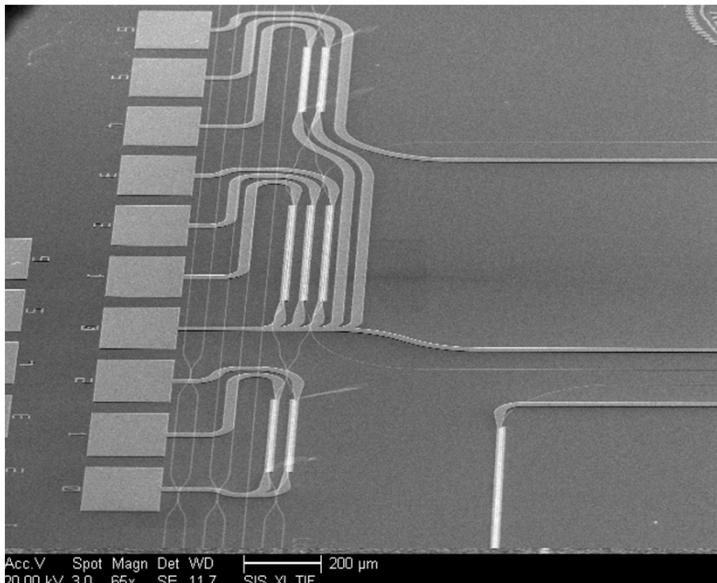
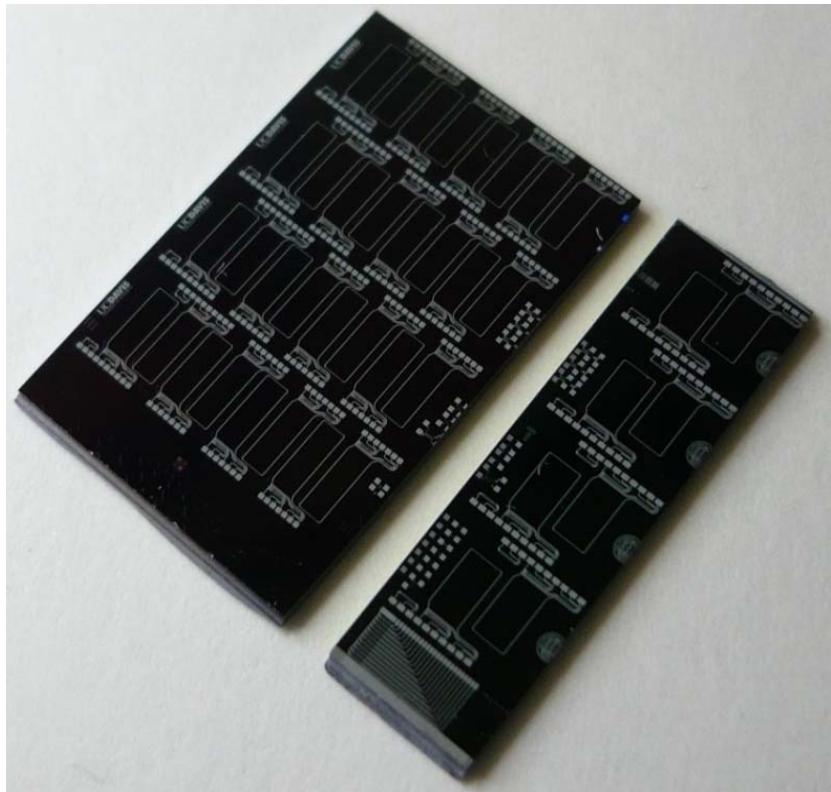
**Increasing silicon
integration over time**

FUTURE
Monolithic?

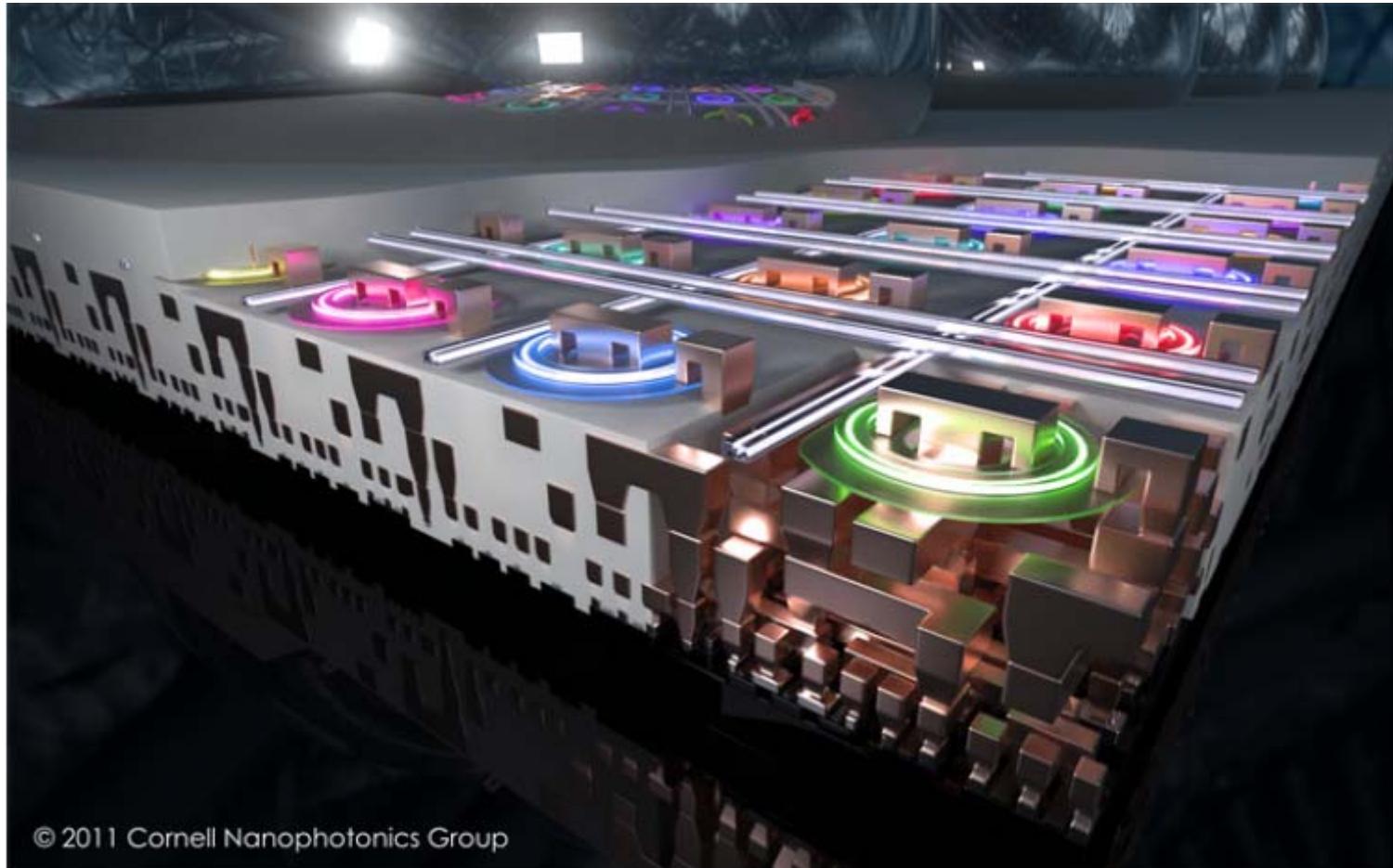


From Intel

Silicon Photonic Chips



3D Integration



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Vision of a 3D optical network on a microelectronic chip based on deposited optics over CMOS electronics. Multiple bus waveguides are positioned at different vertical layers above a set of an array of microring resonators.

Research for UG students

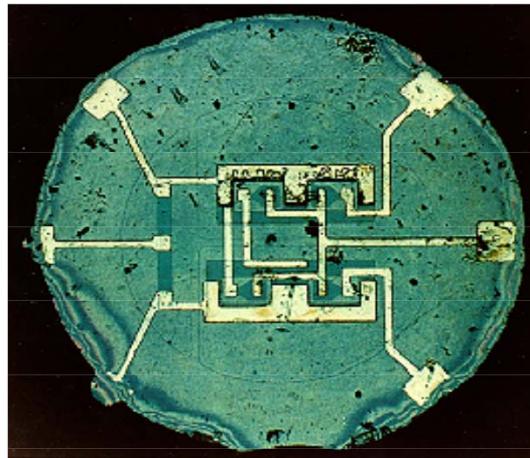
- Silicon modulators
- Optical filters
- Device optimization
- Optical delay lines
- Optical signal processing
- Plasmonic devices
- etc.

If you would like to do research on these topics,
please contact Prof. Linjie Zhou (ljzhou@sjtu.edu.cn)

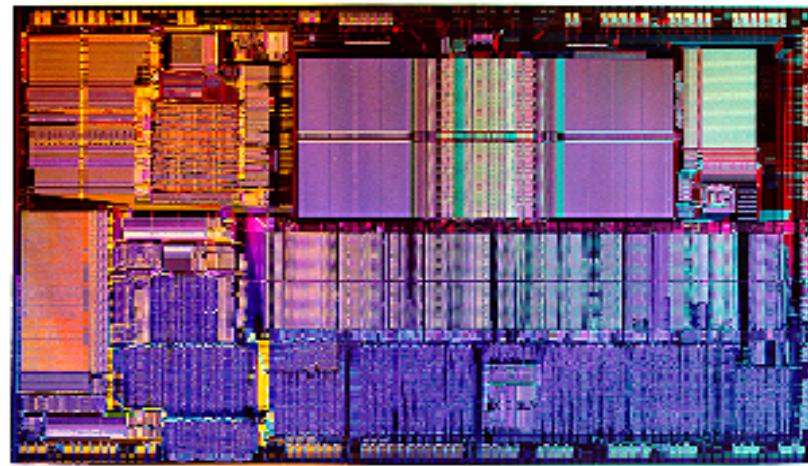
Microelectronics Development History

Silicon Integrated Circuits

- Beginning of Information age
- Basic building block for economics



1960s



1990s

Increasing: circuit complexity, packing density, chip size, speed, and reliability

Decreasing: feature size, price per bit, power (delay) product

Feature size reduction - $0.7 \times /2$ years (3 years).

Increasing chip size $\approx 16\%$ per year (6.3% for MP, 12% for DRAM).

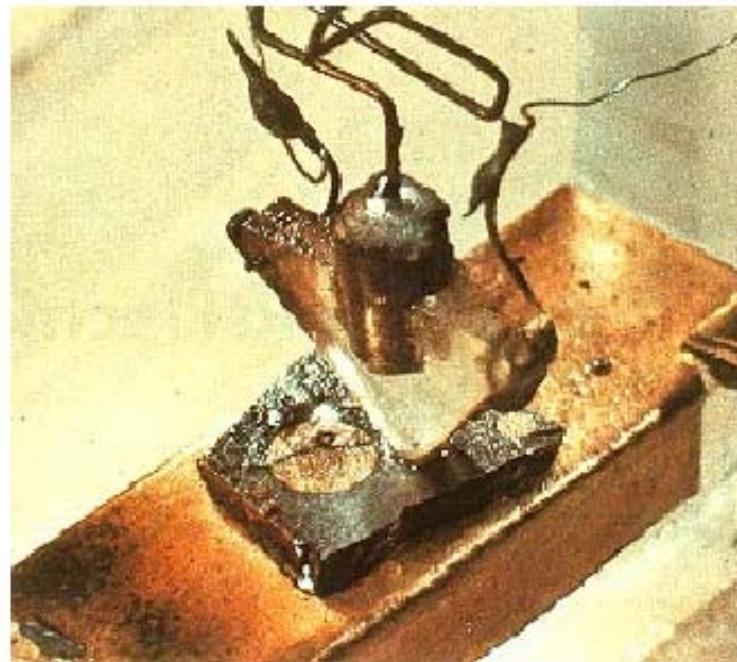
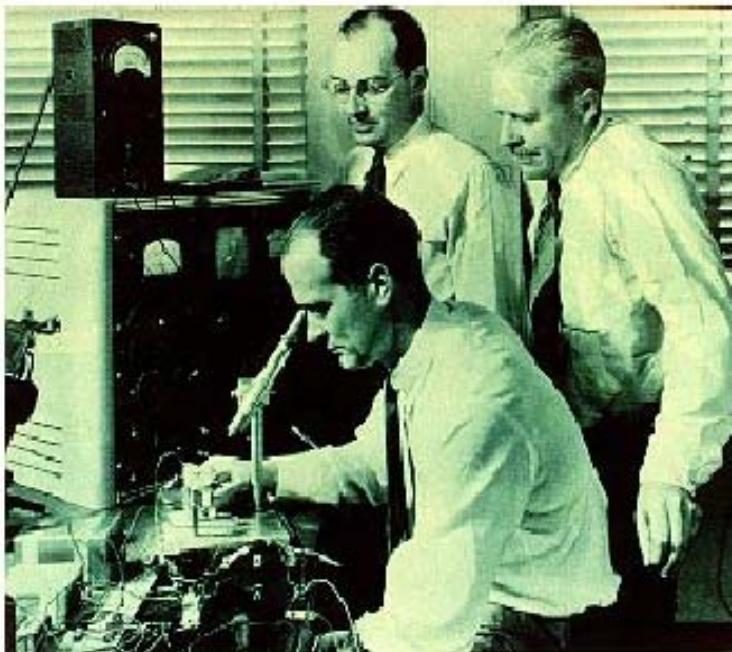
“Creativity” in implementing functions.

IC Fabrication: Brief History

- ④ 1940s – setting the stage- the initial inventions that made integrated circuits possible.
 - ④ In 1945, Bell Labs established a group to develop a semiconductor replacement for the vacuum tube. The group led by William Shockley, included, John Bardeen, Walter Brattain and others.
 - ④ In 1947 Bardeen and Brattain and Shockley succeeded in creating an amplifying circuit utilizing a point-contact "transfer resistance" device that later became known as a transistor.
 - ④ In 1951 Shockley developed the junction transistor, a more practical form of the transistor.
 - ④ By 1954 the transistor was an essential component of the telephone system and the transistor first appeared in hearing aids followed by radios.
-

Transistor invented at Bell lab. in 1947

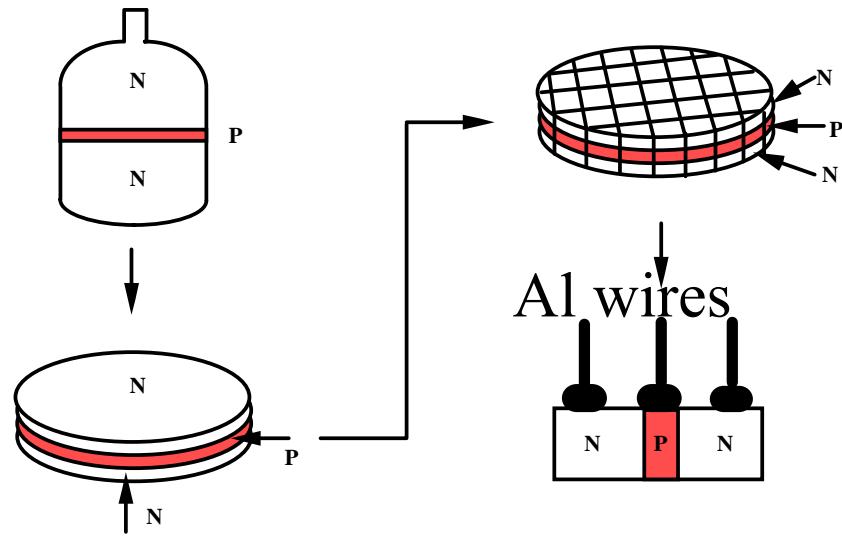
Point contact transistor



In 1956 the importance of the invention of the transistor by Bardeen, Brattain and Shockley was recognized by the **Nobel Prize in physics**.

Grown and Alloy Junction Transistors

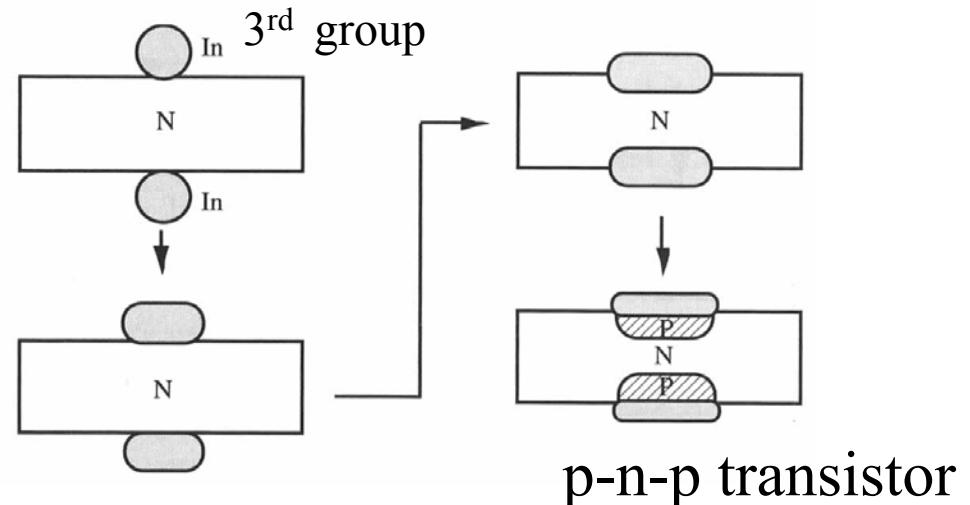
Grown junction transistors in 1950s



Exposed junctions had degraded surface properties and no possibility of connecting multiple devices

Alloy junction technology in 1950s

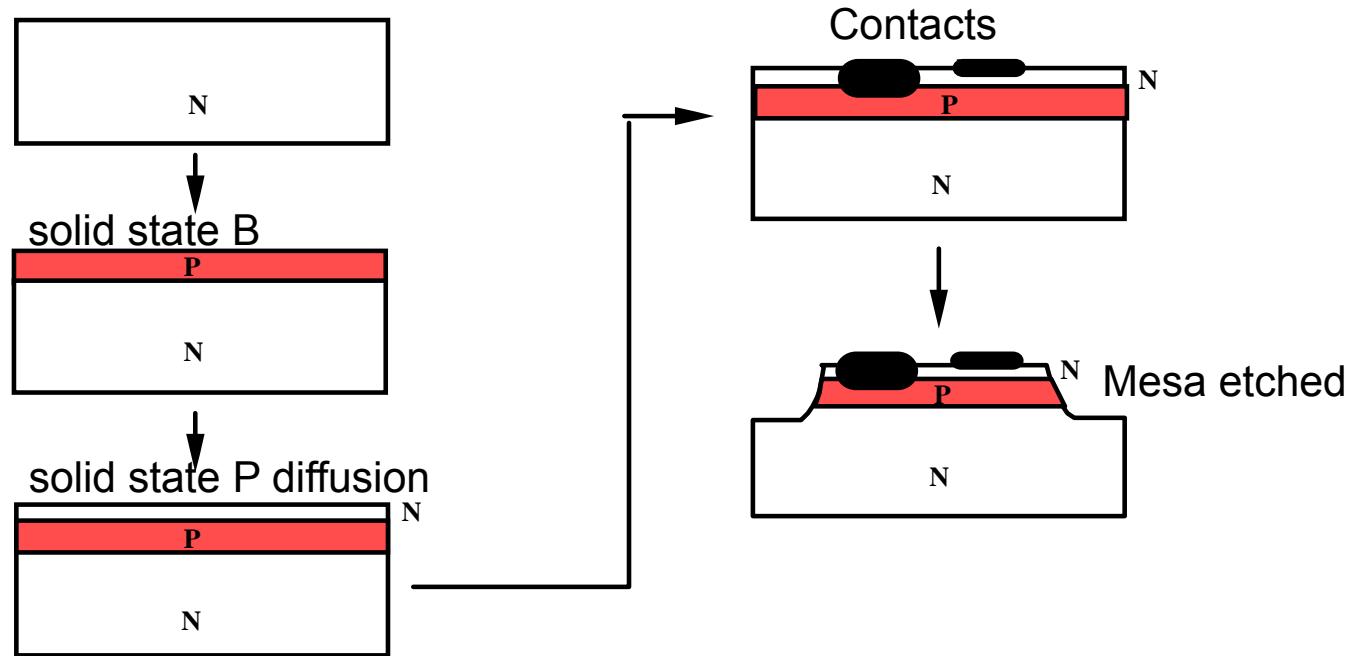
Ge used as a crystal, III and V group atoms used as dopants



p-n-p transistor

The Mesa Design of Bipolar Transistors

Bell Lab, 1957, Double Diffused Process

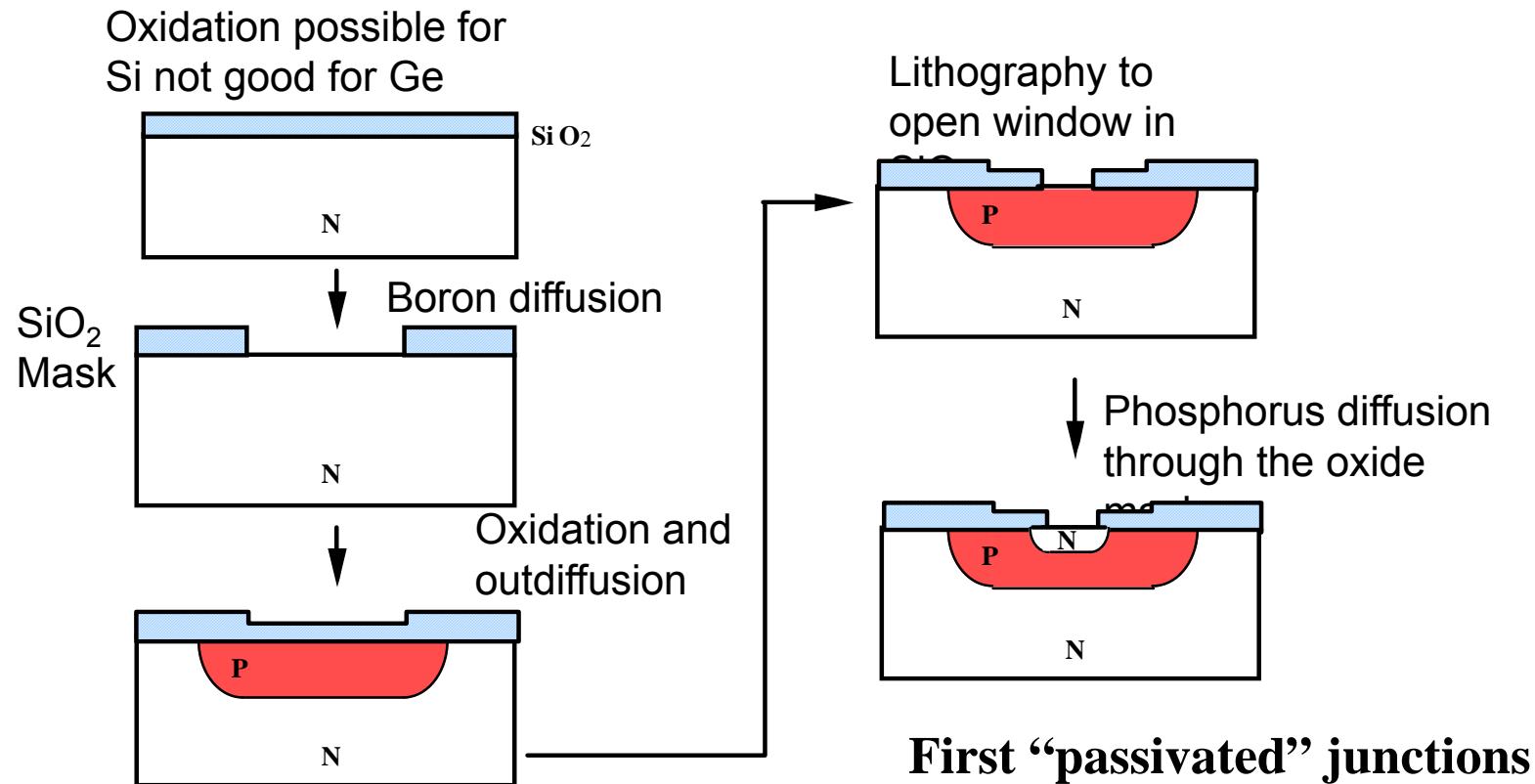


Advantage: Connection of multiple devices but no ICs

Disadvantage: Degradation by exposed junctions at the surface

The Planar Process – Masking

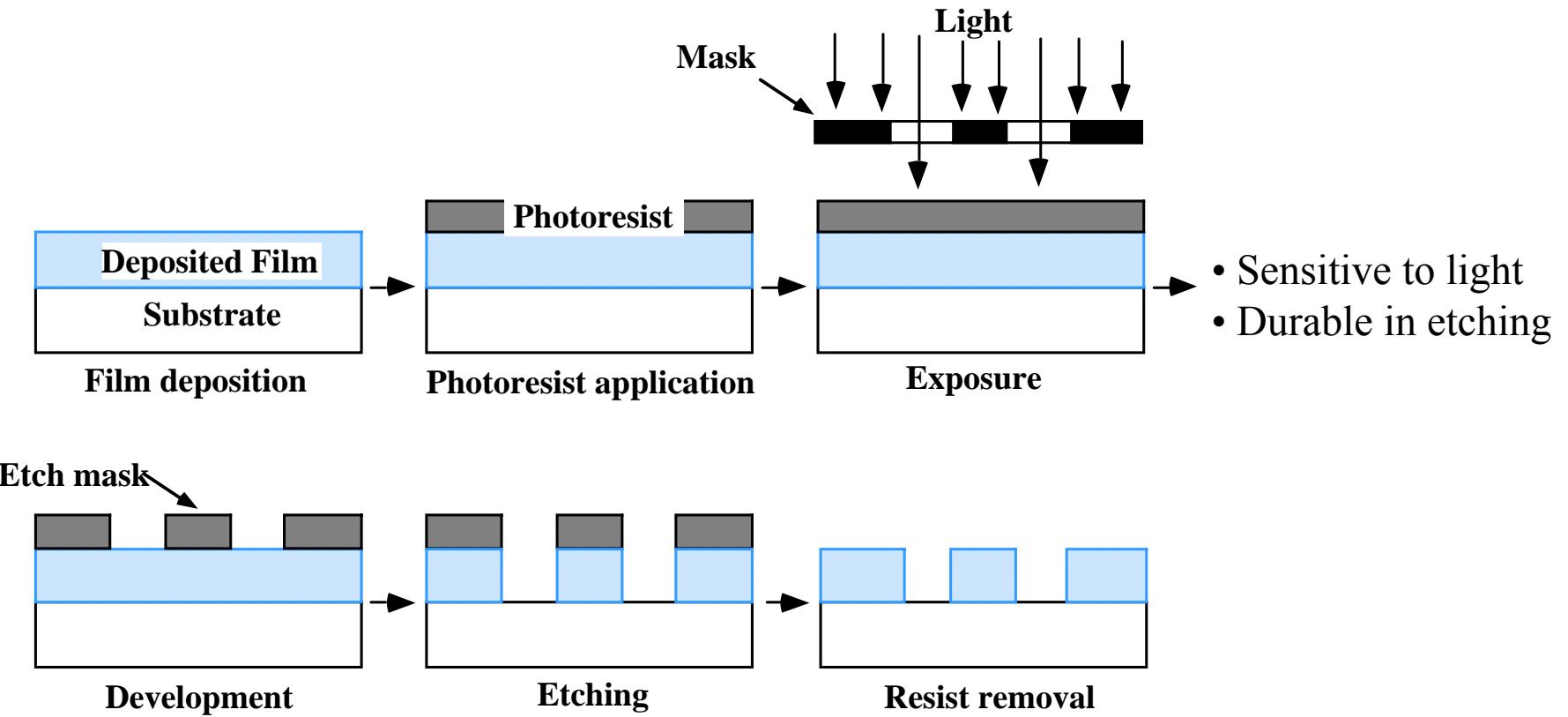
The planar process of Hoerni of Fairchild (1950s)



Beginning of the Silicon Technology and the End of Ge devices

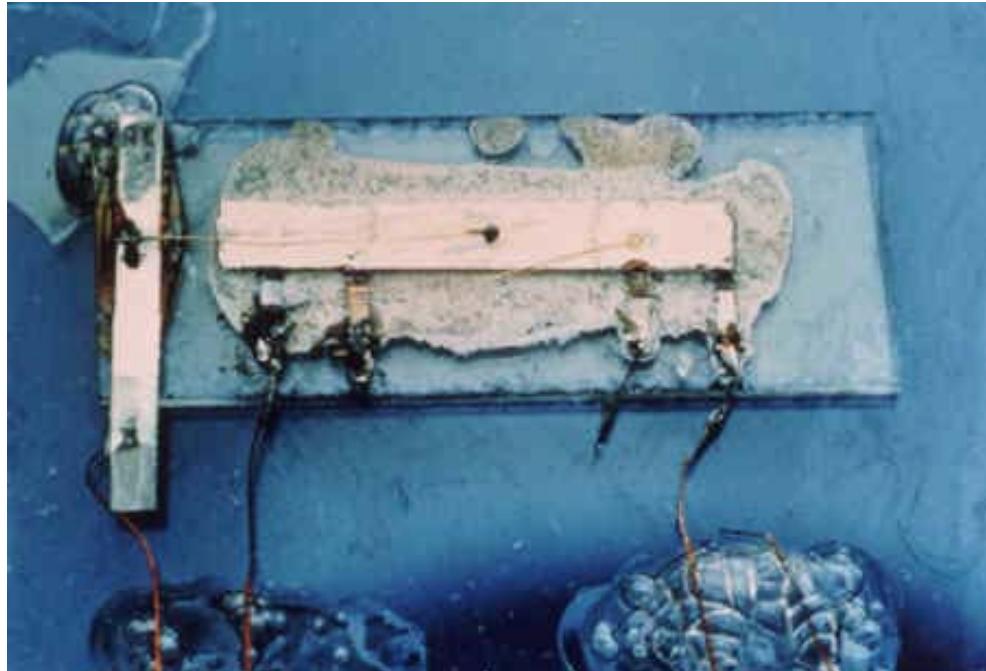
Implementation of a masking oxide to protect junctions at the Si surface

The Planar Process – Photolithography



Basic lithography process which is central to today's chip fabrication.

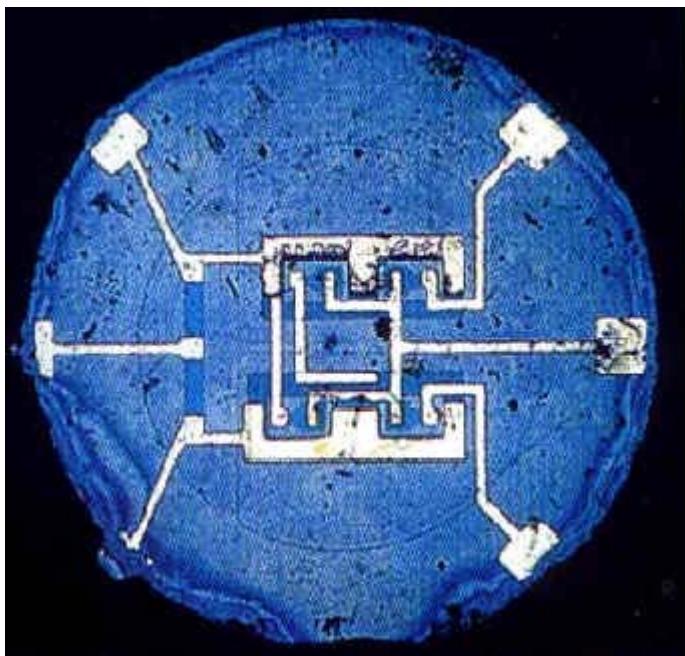
1958 - Integrated circuit invented



A simple oscillator
five integrated components (resistors, capacitors, distributed capacitors and transistors)

- September 12th 1958
Jack Kilby at Texas instrument had built a simple oscillator IC
 - In 2000 the importance of the IC was recognized when Kilby shared the **Nobel prize in physics** with two others.
 - Kilby was cited by the Nobel committee "*for his part in the invention of the integrated circuit*"
-

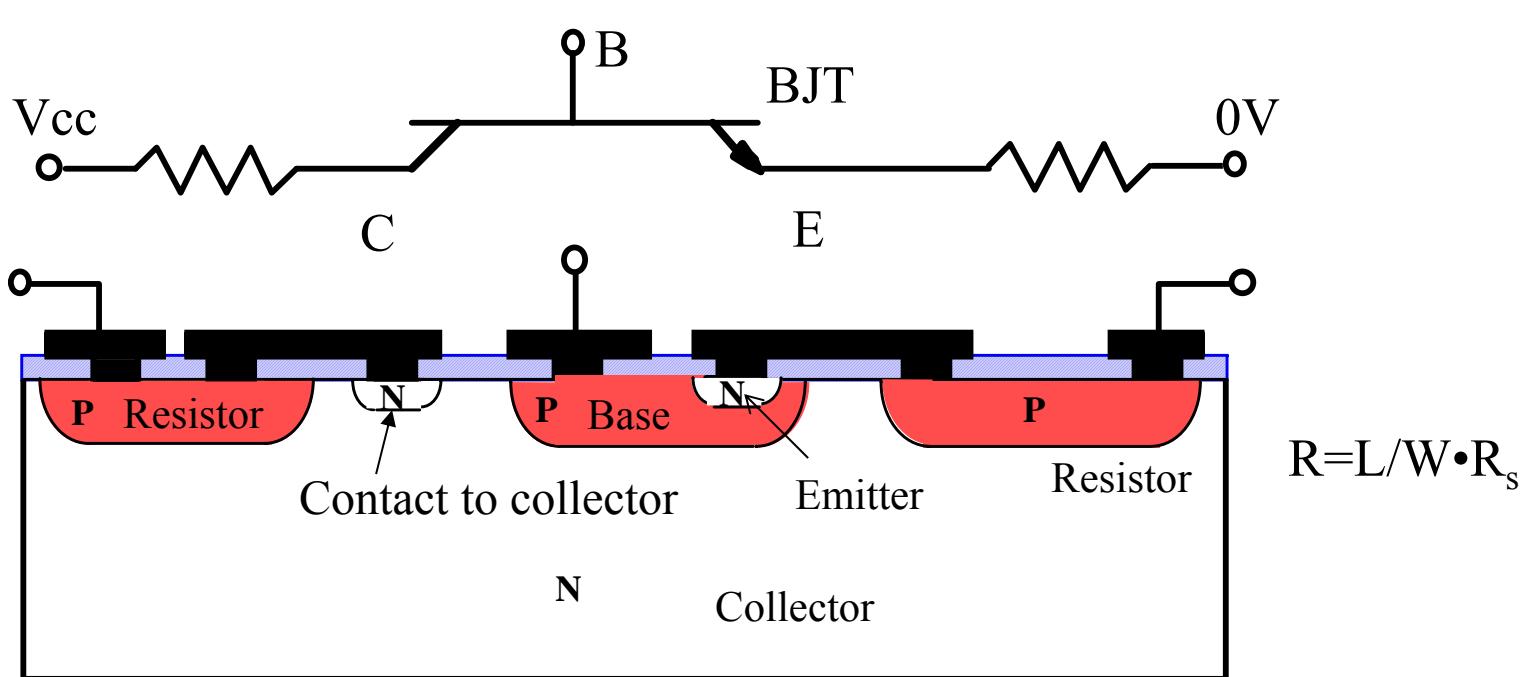
1959 - Planar technology invented



Planar technology

- Kilby's individual circuit elements were connected with **gold wires**, difficult to scale up
- By late 1958 **Jean Hoerni** at Fairchild had developed a structure with N and P junctions formed in silicon. Silicon dioxide was used as an insulator and holes were etched open in the silicon dioxide to connect to the junctions.
- In 1959, **Robert Noyce** also of Fairchild had the idea to **evaporate a thin metal layer** over the circuits created by Hoerni's process.
- Planar technologies set the stage for complex integrated circuits and is the process used today.

Alignment of Layers to Fabricate IC Elements



- Lithographic process allows integration of multiple devices side by side on a wafer.
- Bipolar Transistor and resistors made in the base region
- Accuracy of placement $\sim 1/4$ to $1/3$ of the linewidth being printed

IC Fabrication Technology: History (cont.)

- ⌚ **1960 - Epitaxial deposition developed**

Bell Labs developed the technique of Epitaxial Deposition whereby a single crystal layer of material is deposited on a crystalline substrate. Epitaxial deposition is widely used in bipolar and sub-micron CMOS fabrication.

- ⌚ **1960 - First MOSFET fabricated**

Kahng at Bell Labs fabricates the first MOSFET.

- ⌚ **1961 - First commercial ICs**

Fairchild and Texas Instruments both introduce commercial ICs.

- ⌚ **1962 - Transistor-Transistor Logic invented**

1962 - Semiconductor industry surpasses \$1-billion in sales

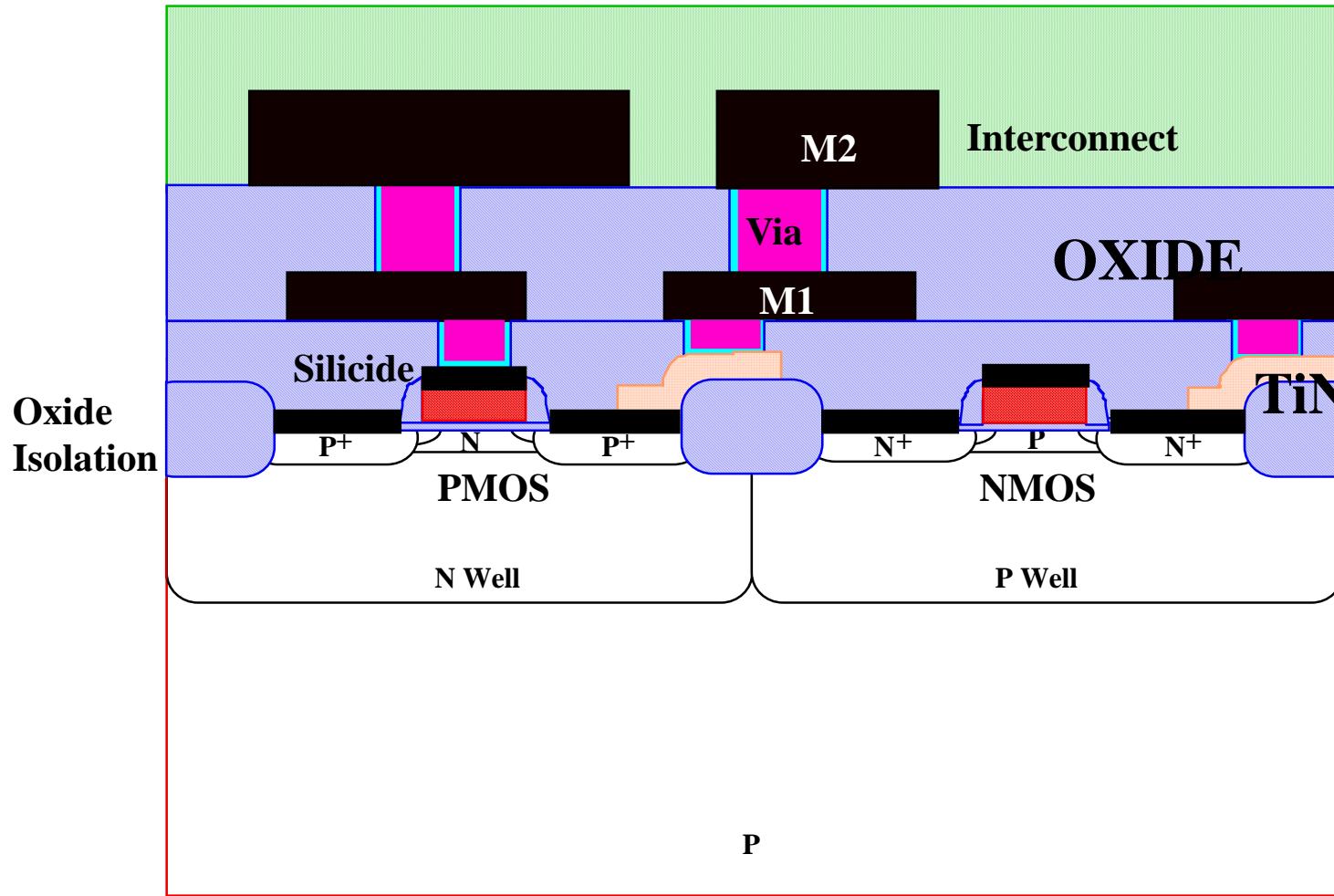
- ⌚ **1963 - First MOS IC**

RCA produces the first PMOS IC.

1963 - CMOS invented

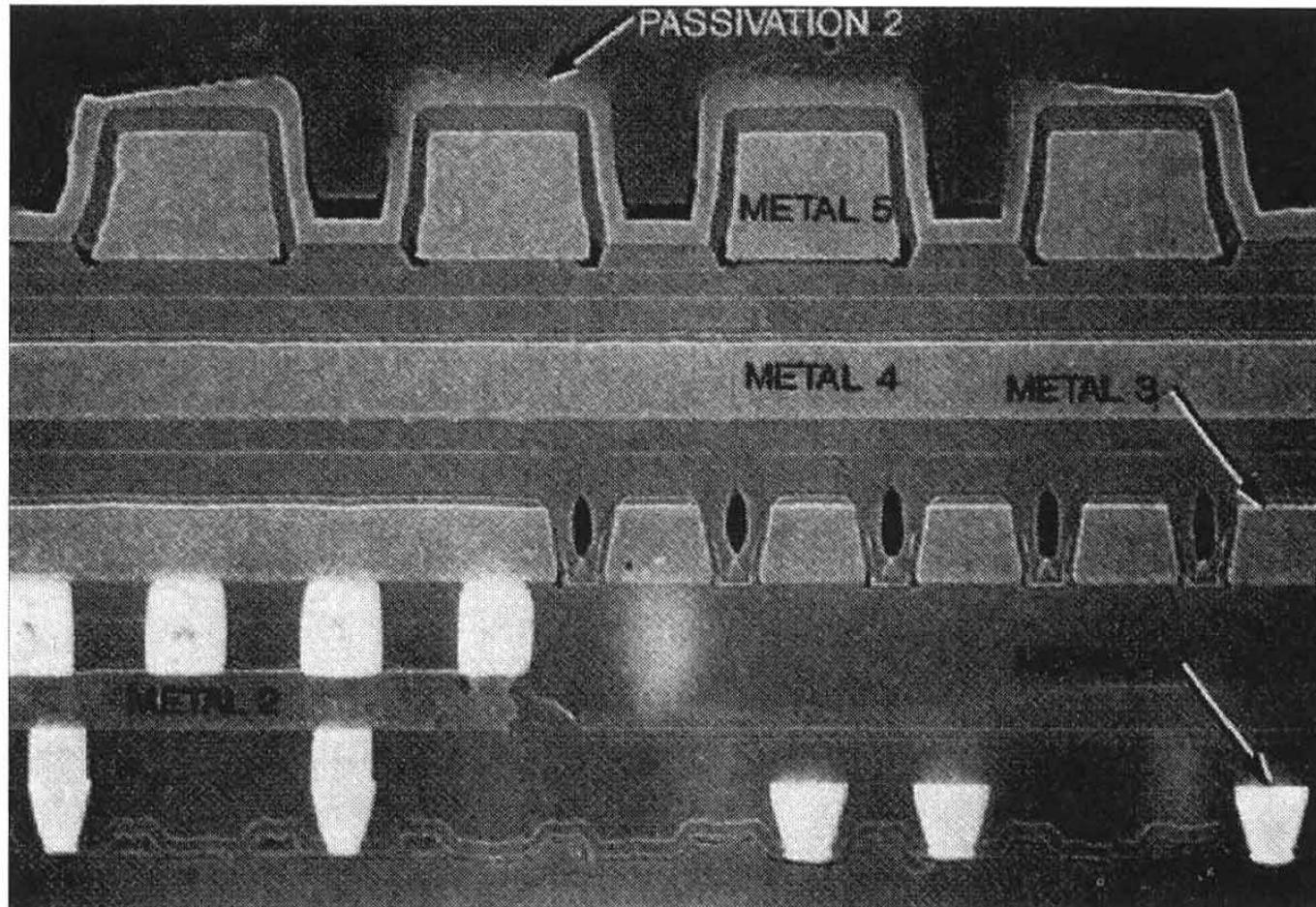
- ➊ Frank Wanlass at Fairchild Semiconductor originated and published the idea of complementary-MOS (CMOS).
 - ➋ It occurred to Wanlass that a complementary circuit of NMOS and PMOS would draw very little current. Initially Wanlass tried to make a monolithic solution, but eventually he was forced to prove the concept with discrete devices.
 - ➌ Amazingly CMOS **shrank standby power** by six orders of magnitude over equivalent bipolar or PMOS logic gates.
 - ➍ On June 18, 1963 Wanlass applied for a patent. On December 5th 1967 Wanlass was issued U.S. Patent # 3,356,858 for "Low Stand-By Power Complementary Field Effect Circuitry".
 - ➎ CMOS forms the basis of the vast majority of all high density ICs manufactured today.
-

Modern CMOS Integrated Circuit



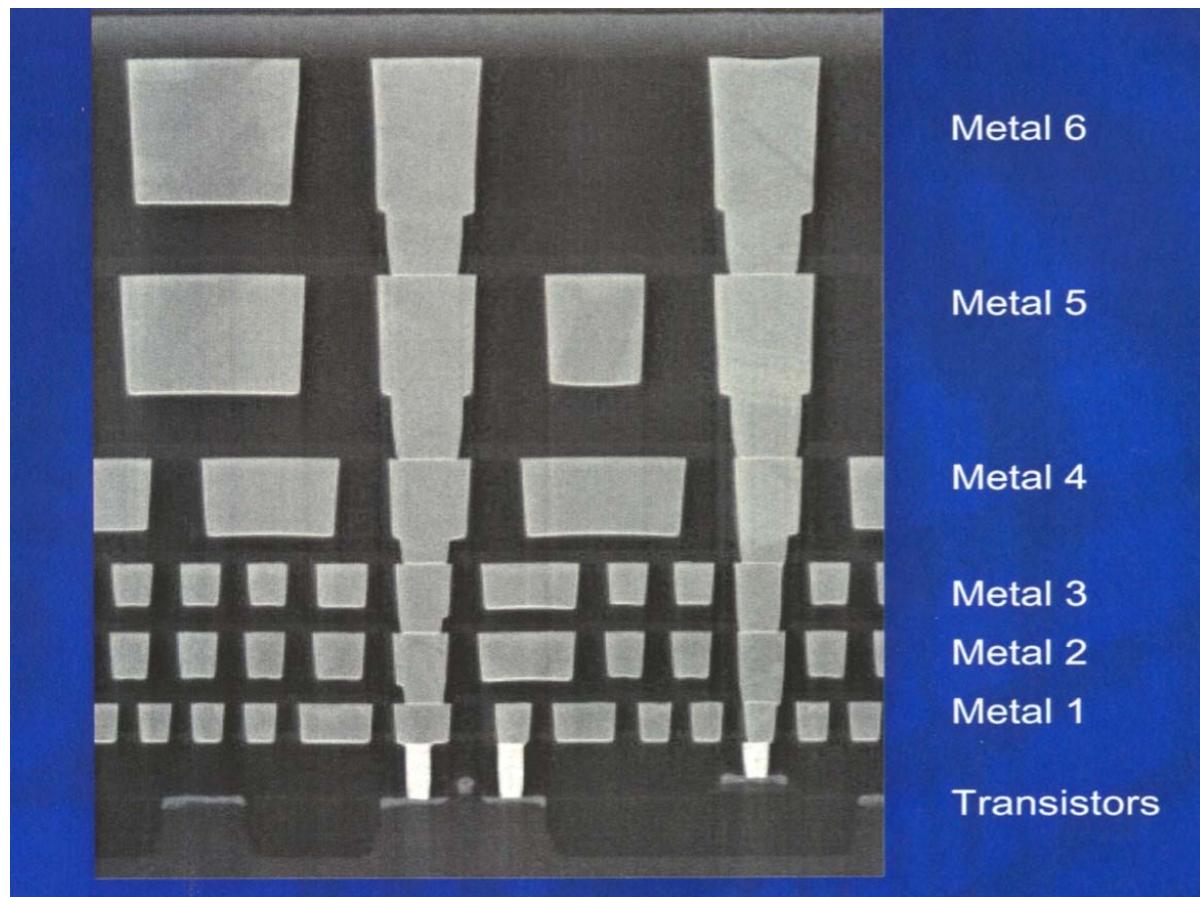
IC is located at the surface of a Si wafer (~500 μ m thick)

CMOS IC SEM



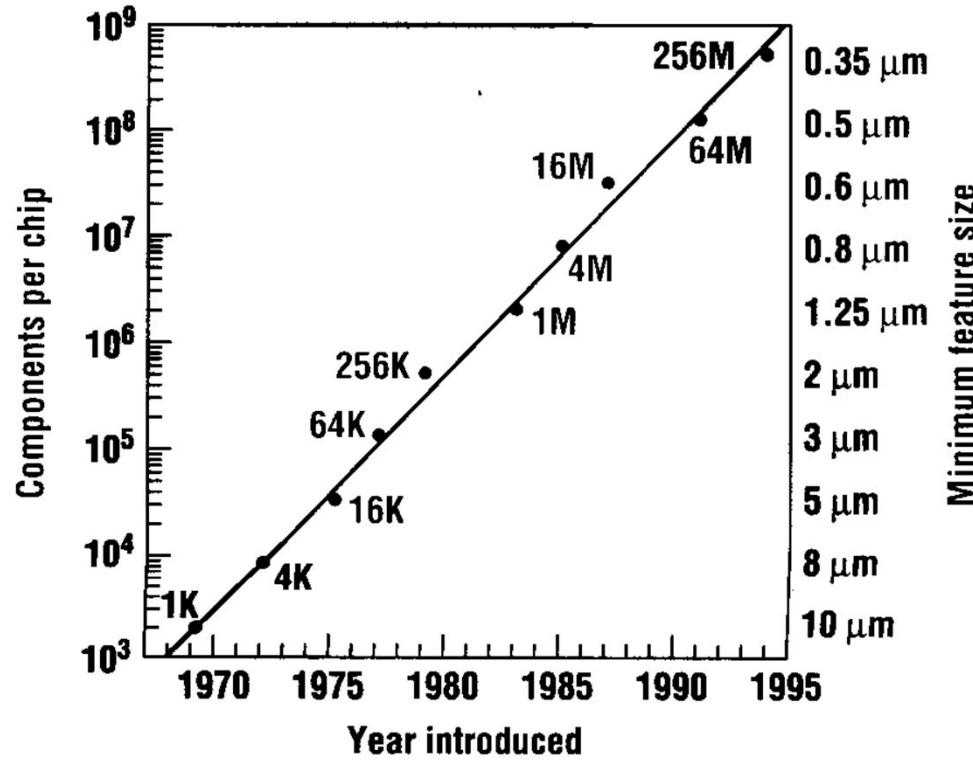
5 metal layers

CMOS IC SEM



Multiple levels of metal and planarization (Intel)

1965 - Moore's law



- ⦿ In 1965 Gordon Moore, director of research and development at Fairchild Semiconductor wrote a paper for Electronics entitled "Cramming more components onto integrated circuits".
- ⦿ In the paper Moore observed that "The complexity for minimum component cost has increased at a rate of roughly *a factor of two per year*". This observation became known as Moore's law, the number of components per IC double every year.
- ⦿ Moore's law was later amended to, the number of components per *IC doubles every 18 months (2 years)*.
- ⦿ Moore's law hold to this day.

1971 - Microprocessor invented

1971 - Intel 4004

- The combination of the Busicom (Japanese calculator company) and the Intel came together, and by 1971 the 4004 the first **4-bit microprocessor** was in production.
- The 4004 processor required roughly 2,300 transistors to implement, used a silicon gate PMOS process with 10µm linewidths, had a 108KHz clock speed.

1972 - Intel 8008

- The 8008 was the **8 bit successor** to the 4004 and was used in the Mark-8 computer, one of the first home computers.
- The 8008 had 3,500 transistors, a 200kHz clock speed and a 15.2mm² die size.

1974 - Intel 8080

- In 1974 Intel introduced the 8080, the first commercially successful microprocessor.

Same trend for integrated photonics

1993-first Pentium processor invented

1993 - Intel Pentium I

- The Pentium is the first processor from Intel capable of executing more than 1 instruction per clock cycle. The Pentium was manufactured in a silicon gate BiCMOS process with $0.8\mu\text{m}$ linewidths, required 18 mask layers and had 1 polysilicon layer and 3 metal layers, the Pentium had 3.1 million transistors, a 60 to 66MHz clock speed and a 264mm^2 die size.

1994 - 64Mbit DRAM

- The 64Mbit DRAM was produced on a CMOS process with 3 to 5 polysilicon layers, 2 to 3 metal layers and $0.35\mu\text{m}$ minimum features. The resulting product had a $1.5\mu\text{m}^2$ memory cell size.

1997 - Intel Pentium II

- The Pentium II was manufactured in a silicon gate CMOS process with $0.35\mu\text{m}$ linewidths, required 16 mask layers and had 1 polysilicon layer and 4 metal layers, the Pentium II had 7.5 million transistors, a 233 to 300MHz clock speed and a 209mm^2 die size.

1998 - 256Mbit DRAM

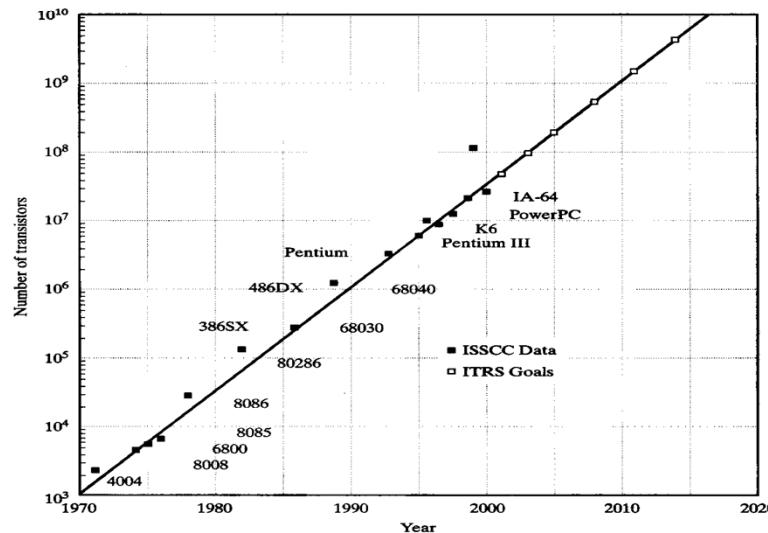
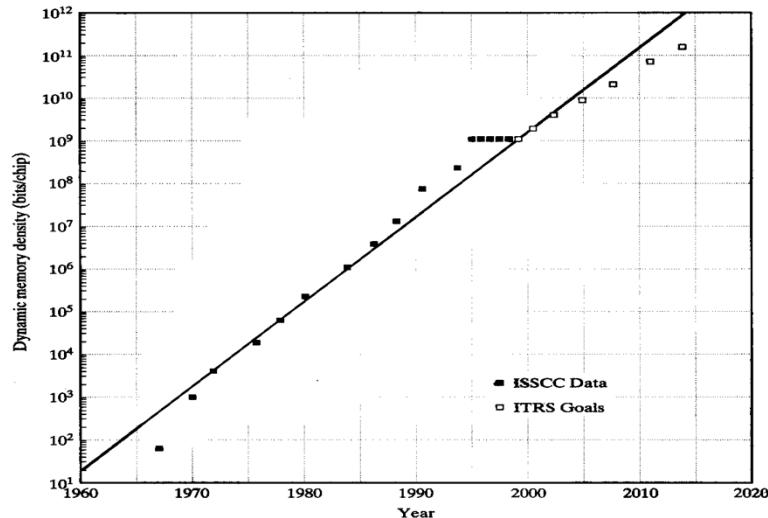
- The 256Mbit DRAM was produced on a CMOS process with 4 to 5 polysilicon layers, 2 to 3 metal layers and $0.25\mu\text{m}$ minimum features. The product had a die size of approximately 204mm^2 .

1999 - Intel Pentium III

- The Pentium III returned to a more standard PGA package and integrated the cache on chip. The Pentium III was manufactured in a silicon gate CMOS process with $0.18\mu\text{m}$ linewidths, required 21 mask layers and had 1 polysilicon layer and 6 metal layers, the Pentium III had 28 million transistors, a 500 to 900MHz clock speed and a 140mm^2 die size.
-

2000 - Intel Pentium 4

- The Pentium 4 introduced an integer unit running at twice the processor speed.
- Silicon gate CMOS process
 - ✓ 0.18 μ m linewidths
 - ✓ 21 mask layers (including 1 polysilicon layer and 6 metal layers)
 - ✓ 42 million transistors
 - ✓ 1,400 to 2,500MHz clock speed
 - ✓ 224mm² die size

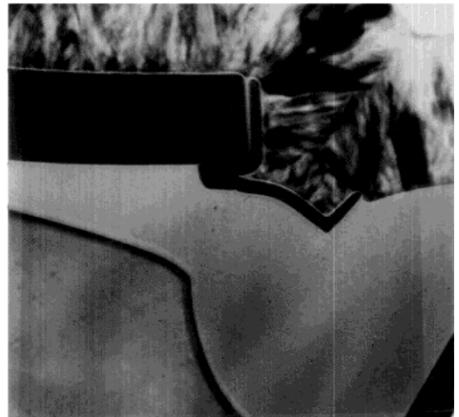
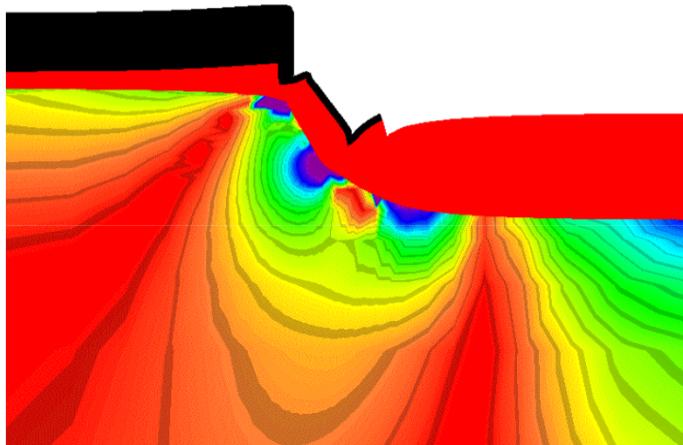


**Future trend:
Micro-core processor**

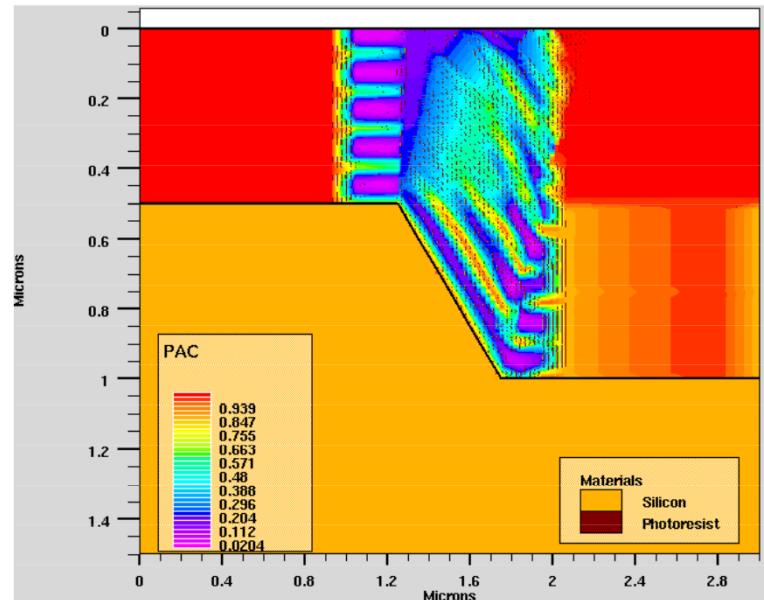
Computer Simulation Tools (TCAD)

Simulation is now used for:

- Designing new processes and devices
- Exploring the limits of semiconductor devices and technology (R&D)
- Solving manufacturing problems (what-if?)



Simulation of an advanced local oxidation process

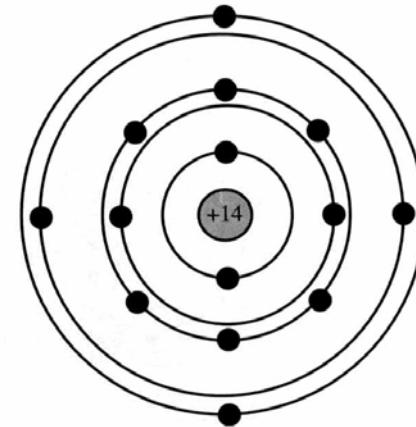
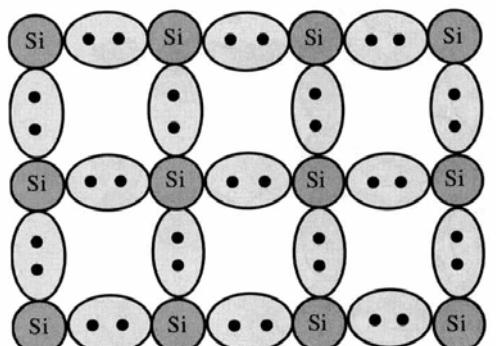


Simulation of photoresist exposure

Microelectronics Devices Review

Semiconductors: Si, Ge and Compound (III-V, II-VI)

Covalent bonding:
no free electrons
at 0K



Four
valence
electrons

N-type dopants

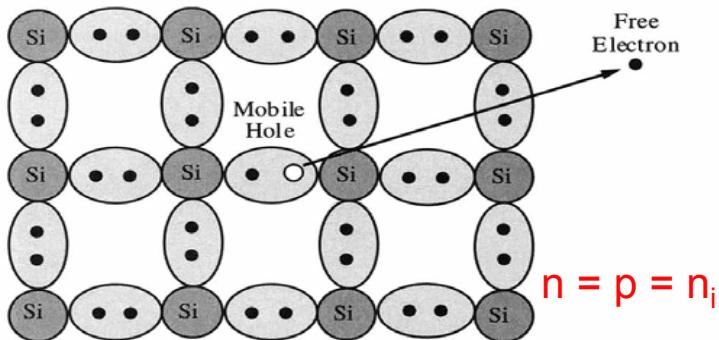
P-type dopants

III ^A	IV ^A	V ^A	VI ^A
5 B 10.81	6 C 12.01	7 N 14.01	8 O 16.00
II ^B	13 Al 26.98	14 Si 28.09	15 P 30.97
30 Zn 65.39	31 Ga 69.72	32 Ge 72.59	33 As 74.92
48 Cd 112.4	49 In 114.8	50 Sn 118.7	51 Sb 121.8
80 Hg 200.6	81 Tl 204.4	82 Pb 207.2	83 Bi 209.0
			84 Po 209

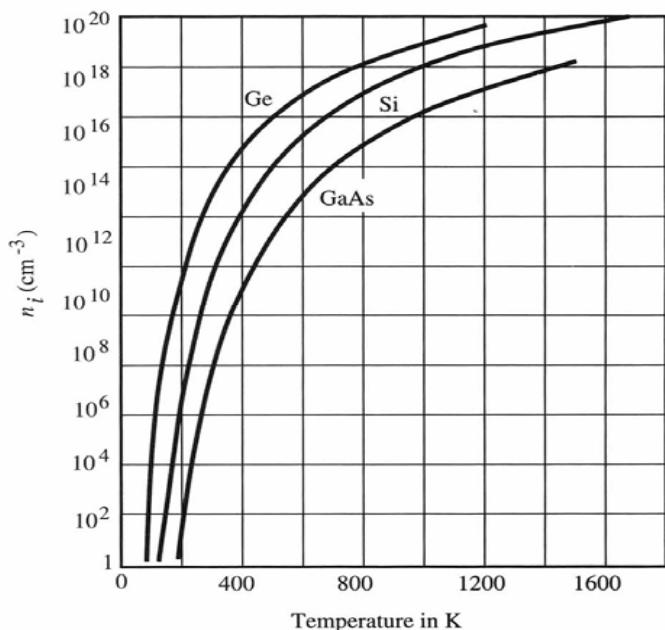
Dopants have

- to be compatible with processing (e.g., slow diffusion through oxide)
- to have high solubility in Si

Intrinsic Semiconductor



Intrinsic carrier concentration

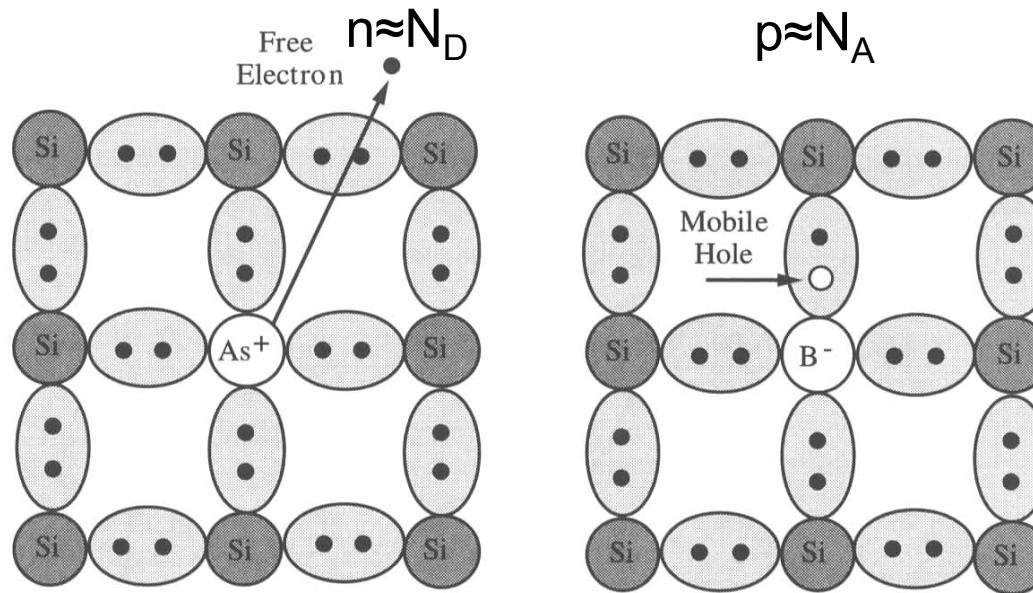


- Electron and hole generation occur at elevated temperature (above 0K)
- Electron and hole pair generation represented by a broken bond in the crystal
- Both carriers are mobile and can carry currents in devices

Energy Band Gap determines the intrinsic carrier concentration n_i $E_g(\text{Ge}) < E_g(\text{Si}) < E_g(\text{GaAs})$

For devices we need concentrations: n and $p \gg n_i$

N- and p-type semiconductor



Doping silicon using As (column V) or B (column III)

N^{--} or P^{--} :

N_D or $N_A < 10^{14} \text{ cm}^{-3}$ Ingot crystal

N^- or P^- : $10^{14} \text{ cm}^{-3} < N_D$ or $N_A < 10^{16} \text{ cm}^{-3}$

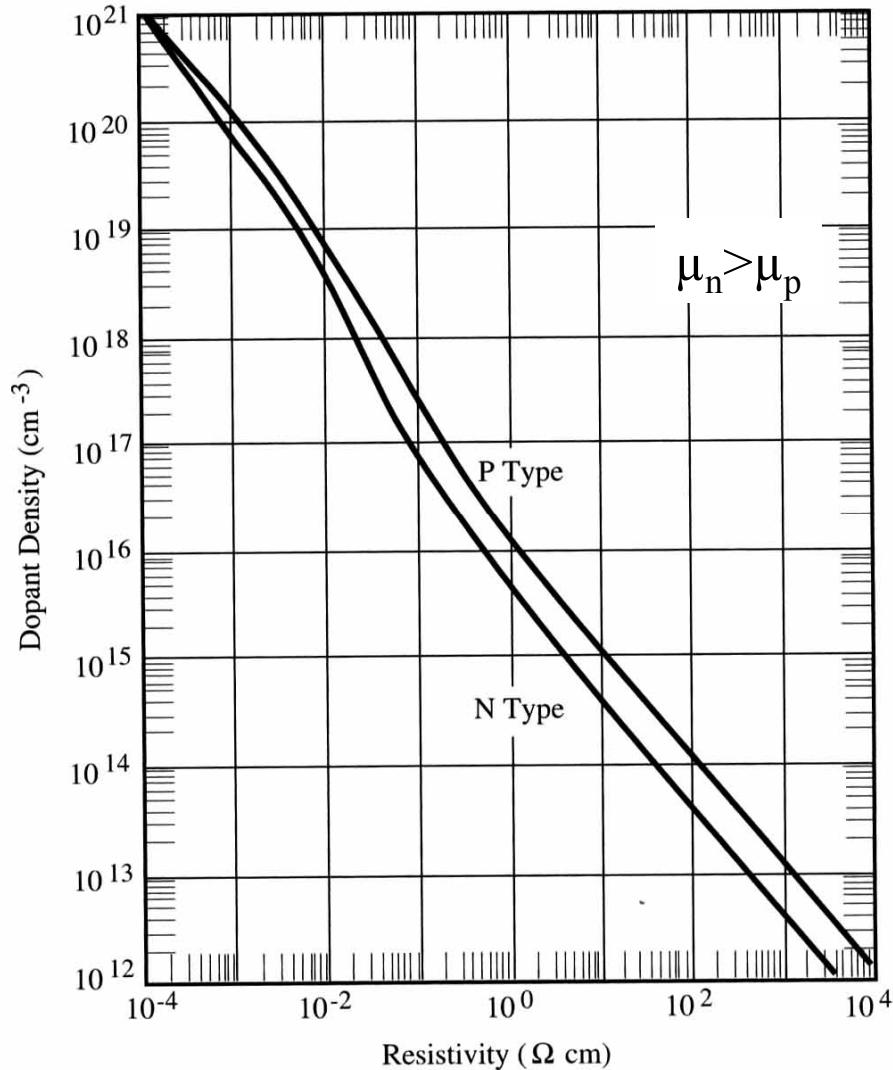
N or P : $10^{16} \text{ cm}^{-3} < N_D$ or $N_A < 10^{18} \text{ cm}^{-3}$

N^+ or P^+ : $10^{18} \text{ cm}^{-3} < N_D$ or $N_A < 10^{20} \text{ cm}^{-3}$

N^{++} or P^{++} :

N_D or $N_A > 10^{20} \text{ cm}^{-3}$

Resistivity VS. Dopant Concentration

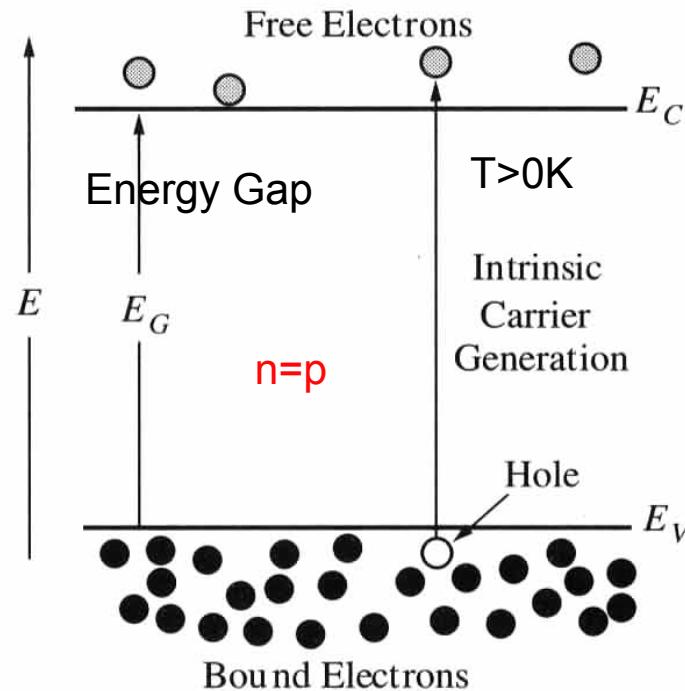


$$\rho = \frac{1}{q\mu_n n + q\mu_p p}$$

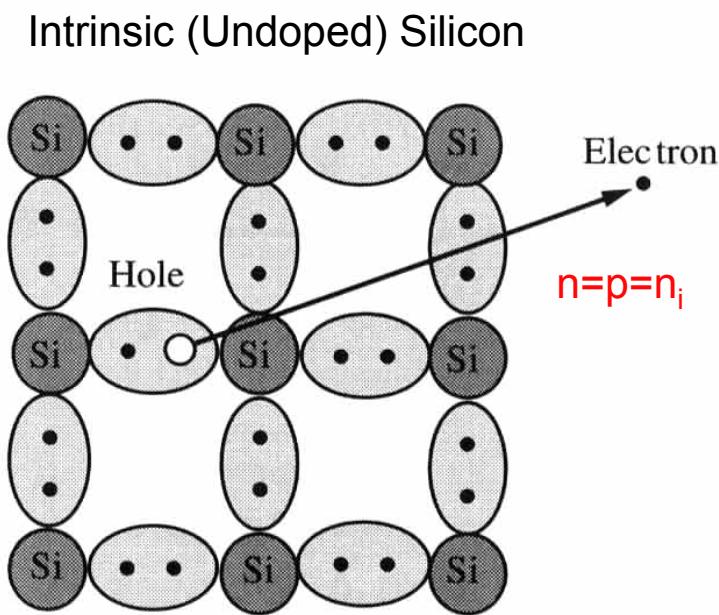
μ carrier mobility depends on scattering i.e. dopants, lattice imperfections (defects) and vibration (temperature)

Band Model and Bond Model of Semiconductors

Band Model



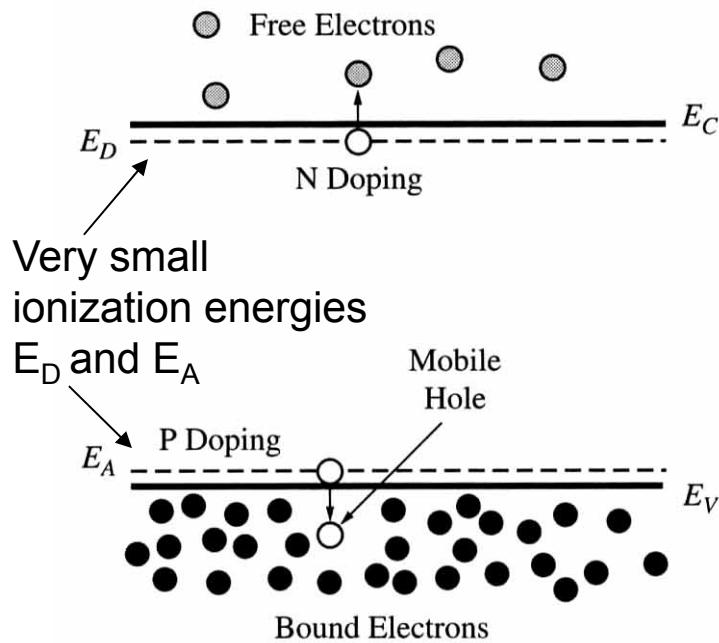
Bond Model



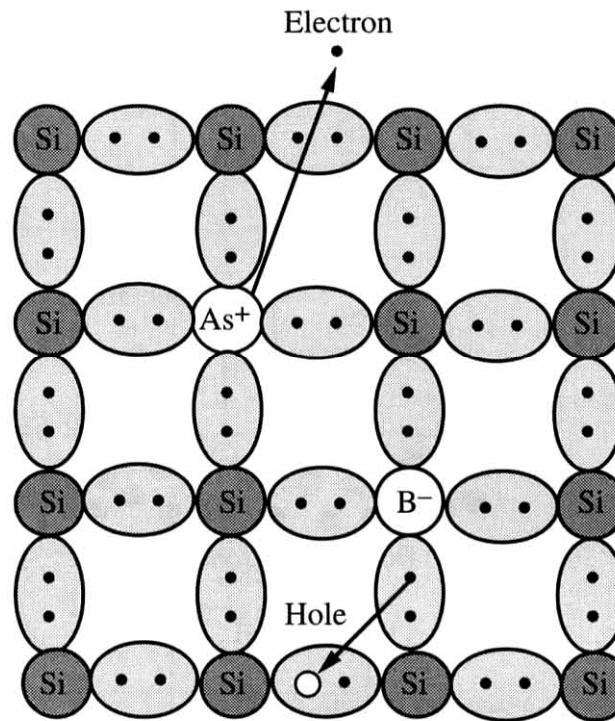
- Bonded electrons lie at energy levels below E_V
 - Free electrons lie at energy levels above E_C
-

Band Model and Bond Model of Semiconductors

Band Model

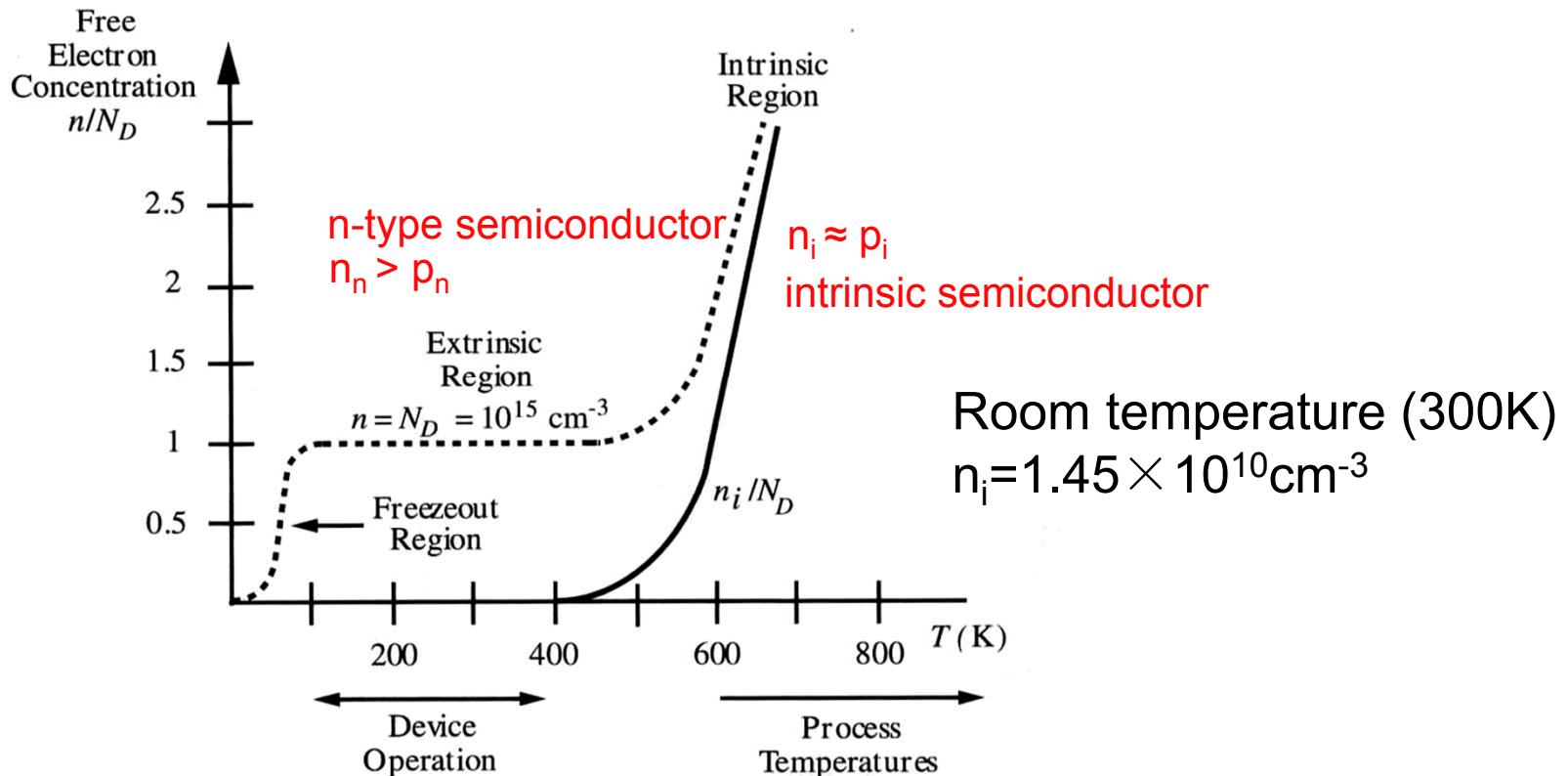


Bond Model



- n-type silicon doped with As with energy level E_D
- P-type silicon doped with B with energy level E_A

Dopant Ionization



- Arsenic doping in silicon ($N_D = 10^{15} \text{ cm}^{-3}$)
- At normal temperatures (device operation temperature), $n = N_D^+$
- At high temperatures, $n_i > 10^{15}$, $n = n_i$

Distribution of Free Carriers

Electrons are subject to the Pauli Exclusion Principle

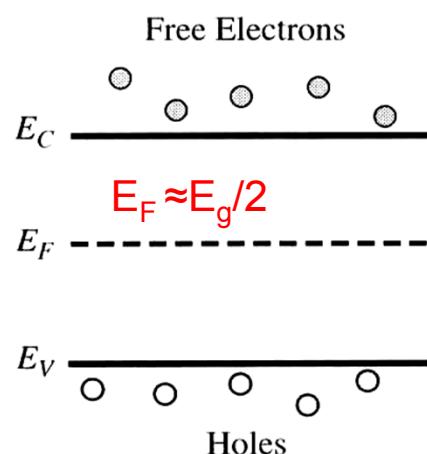
Fermi Dirac probability function:

$$F(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)}$$

Fermi level is the energy at which the probability of finding an electron $F(E)$ is 0.5

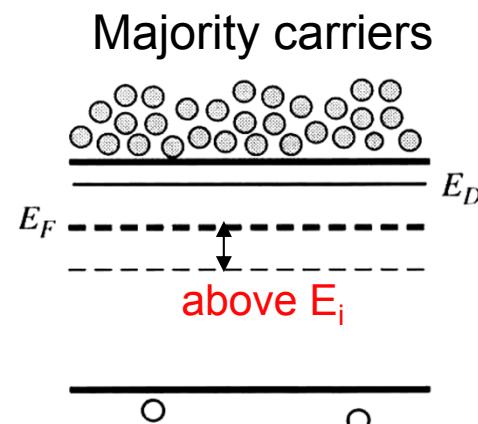
Intrinsic Semiconductor

$$n=p=n_i$$



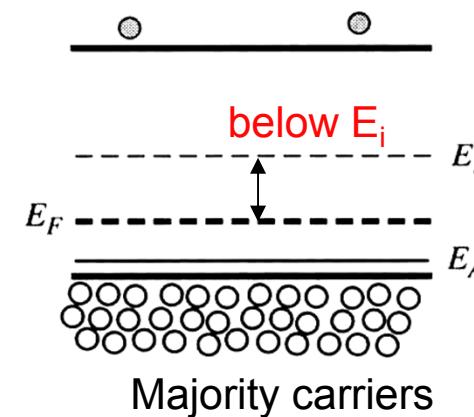
n-type Semiconductor

$$n=N_D$$

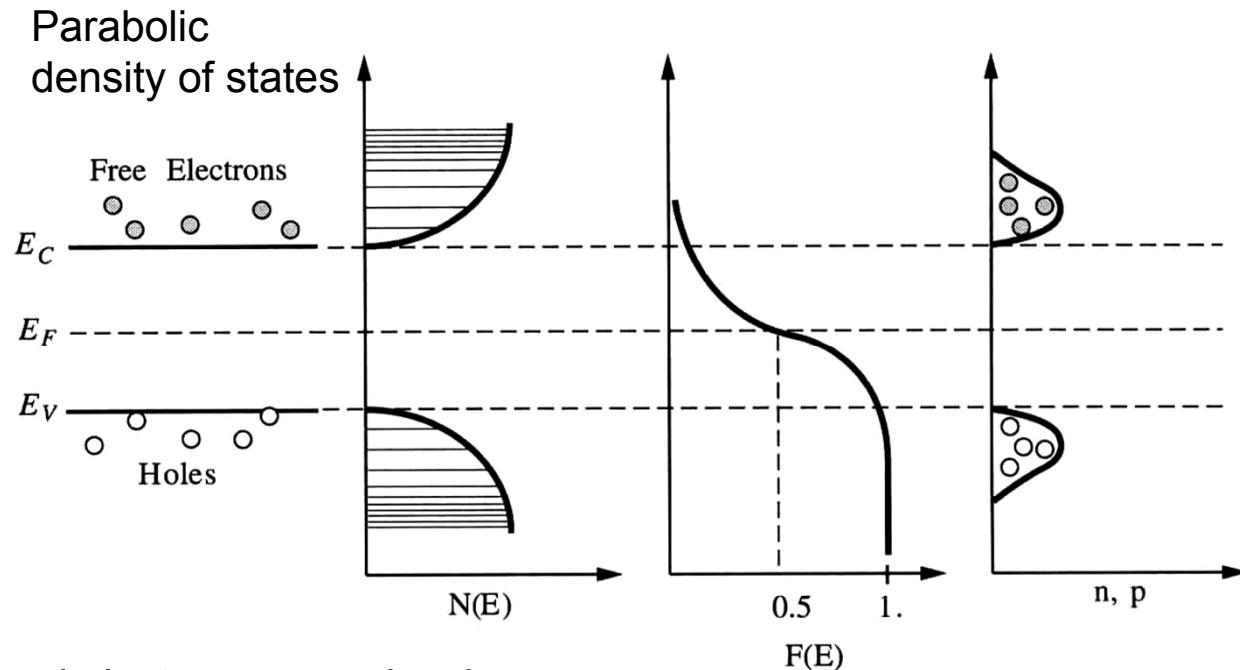


p-type Semiconductor

$$p=N_A$$



Carriers' Statistics



Allowed electron energy levels:

$$N(E) = \frac{4\pi}{h^3} (m_e^*)^{\frac{3}{2}} (E - E_C)^{\frac{1}{2}} \quad \text{For } E > E_C$$

$$N(E) = \frac{4\pi}{h^3} (m_h^*)^{\frac{3}{2}} (E_V - E)^{\frac{1}{2}} \quad \text{For } E < E_V$$

m_e^* Effective mass of electron

m_h^* Effective mass of hole

Total number of electrons and holes:

$$n = \int_{E_C}^{\infty} F(E) N(E) dE \cong N_C \exp\left(-\frac{E_C - E_F}{kT}\right)$$

$$p = \int_{-\infty}^{E_V} [1 - F(E)] N(E) dE \cong N_V \exp\left(-\frac{E_F - E_V}{kT}\right)$$

$$N_C = 2 \left(\frac{2\pi m_e^* k T}{h^2} \right)^{\frac{3}{2}} \quad N_V = 2 \left(\frac{2\pi m_h^* k T}{h^2} \right)^{\frac{3}{2}}$$

Carrier Concentrations

$$np = n_i^2 = N_c N_v \exp\left(-\frac{E_g}{kT}\right)$$

Room temperature (300K)
 $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$

$$\begin{cases} n = n_i \exp\left(\frac{E_F - E_i}{kT}\right) \\ p = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \end{cases}$$

Charge neutrality requires:

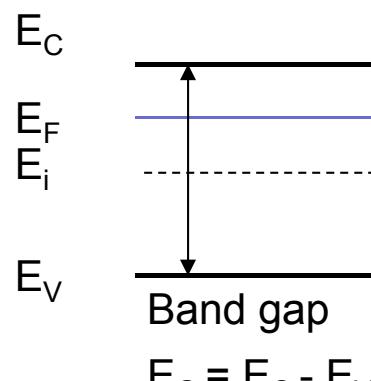
$$N_D^+ + p = N_A^- + n$$

Carrier concentration becomes

$$n = \frac{1}{2} \left[(N_D^+ - N_A^-) + \sqrt{(N_D^+ - N_A^-)^2 + 4n_i^2} \right]$$

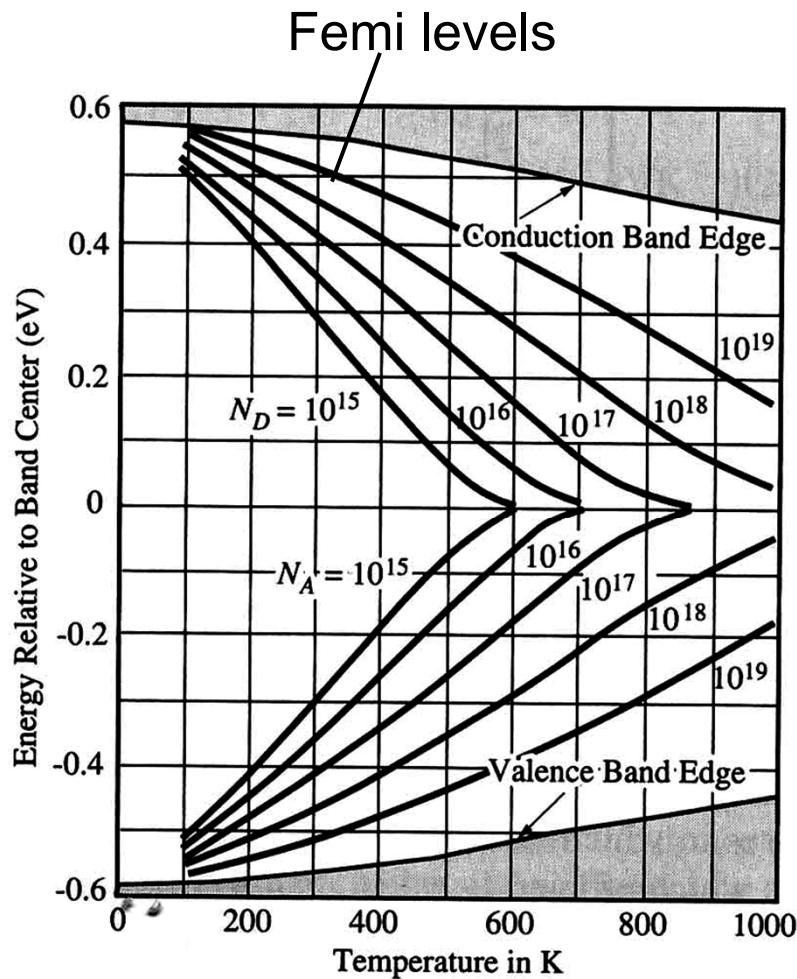
$$p = \frac{1}{2} \left[(N_A^- - N_D^+) + \sqrt{(N_A^- - N_D^+)^2 + 4n_i^2} \right]$$

Heavy doping moves E_F to E_C



$$E_G = E_C - E_V$$

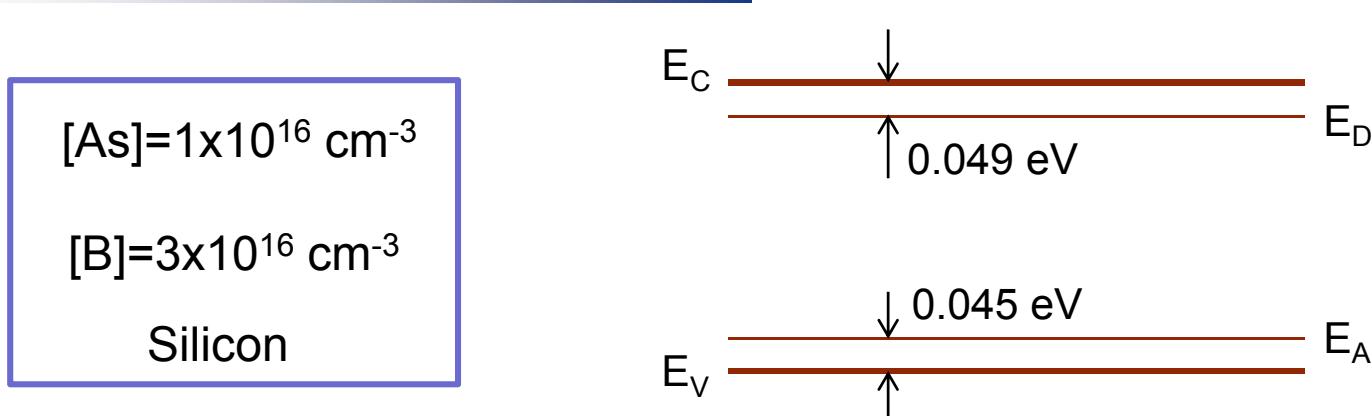
Energy Band Dependence on Temperature



- Lattice constant increases with temperature
- Larger lattice constant weakens the bonding between atoms causing the band gap energy E_G (energy needed to free e-h pairs) to decrease

$$E_G(eV) = 1.17 - \frac{4.73 \times 10^{-4} T^2}{T + 636} \approx 1.16 - (3 \times 10^{-4})T$$

Example



Calculate n, p and E_F for

- (a) room temperature – device operating condition
- (b) 1000°C – processing temperature

Example

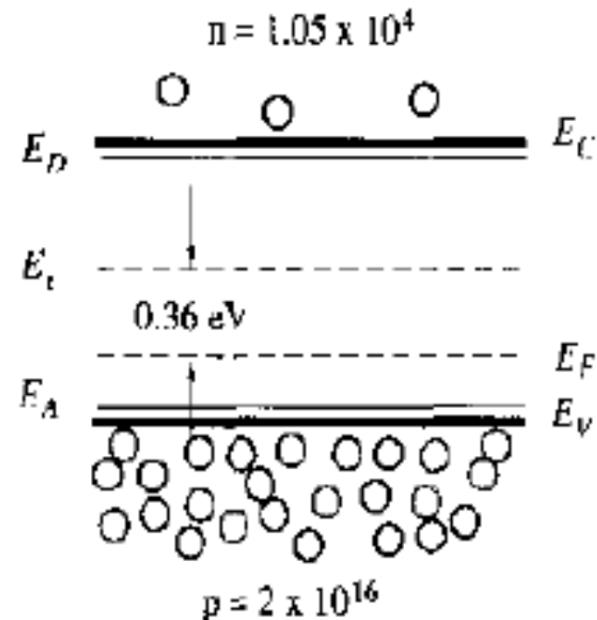
(a) room temperature – device operating condition

$$p = N_A - N_D = 2 \times 10^{16} \text{ cm}^{-3}$$

$$n = \frac{n_i^2}{p} = \frac{2.1 \times 10^{20}}{2 \times 10^{16}} = 1.05 \times 10^4 \text{ cm}^{-3}$$

$$p = n_i \exp\left(\frac{E_i - E_F}{kT}\right)$$

$$\therefore E_i - E_F = kT \ln \frac{p}{n_i} = (8.62 \times 10^{-5} \text{ eVK}^{-1})(298K) \ln \frac{2 \times 10^{16}}{1.45 \times 10^{10}} = 0.36 \text{ eV}$$



Example

(b) 1000°C – processing temperature

$$n_i^2 = N_c N_v \exp\left(-\frac{E_g}{kT}\right)$$

$$n_i = 3.1 \times 10^{16} T^{3/2} \exp\left(-\frac{0.603 \text{ eV}}{kT}\right) \text{ cm}^{-3}$$
$$= 7.14 \times 10^{18} \text{ cm}^{-3} \quad @ 1000^\circ\text{C}$$

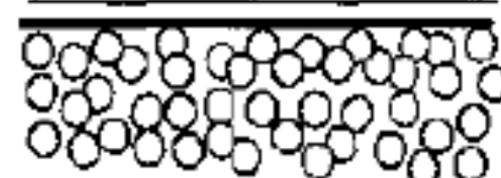
$n_i \gg p$, $n \rightarrow$ material is intrinsic
→ Fermi level in the middle of bandgap

E_g is significantly smaller at 1000°C than it is at room temperature

$$n = 7.14 \times 10^{18}$$



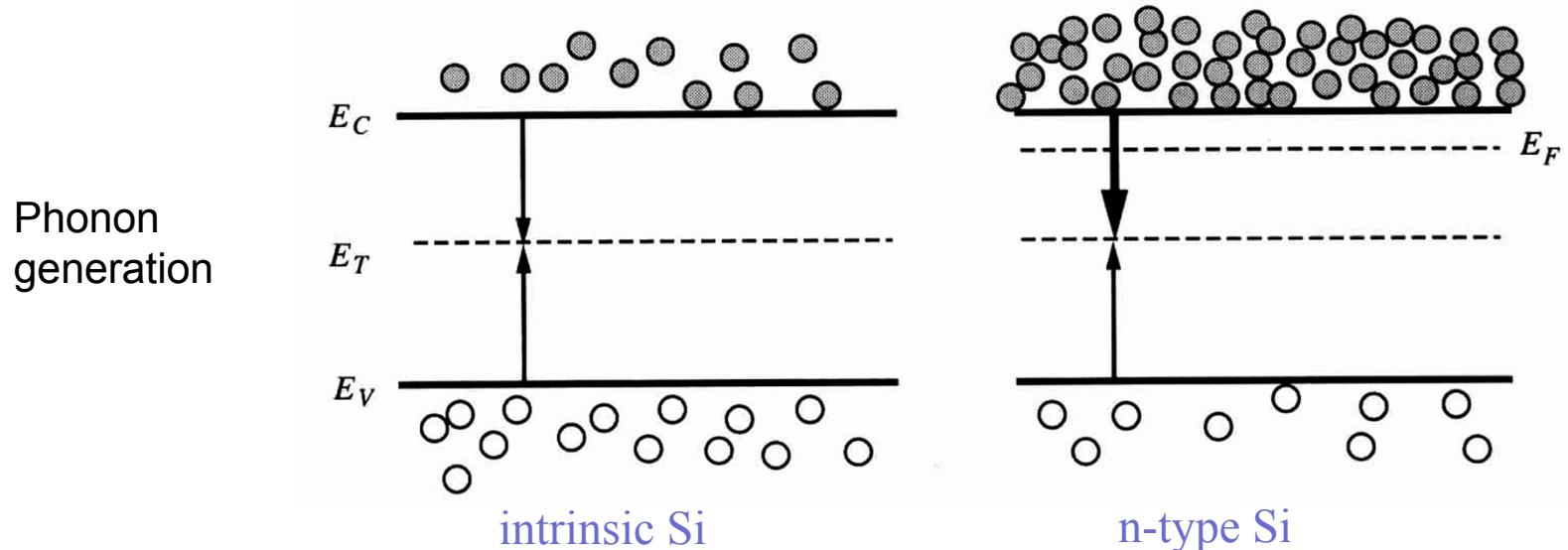
$$E_F = E_1$$



$$p = 7.14 \times 10^{18}$$

Recombination of Carriers

Si is an **indirect semiconductor** so indirect recombination (Shockley-Read-Hall) occurs through traps located in the mid-gap



$$\tau_R = \frac{1}{\sigma v_{th} N_t}$$

τ_R Recombination lifetime (sec) ← minority
 σ Capture cross section (cm^2)
 v_{th} Thermal velocity (cm/s)
 N_t Density of traps (cm^{-3})

Carrier Recombination and Generation

Traps (defects, metal impurities) present in silicon act either to **annihilate** carriers (recombination) or **produce** (generation) them.

SRH recombination/generation rate

$$U = \frac{np - n_i^2}{\tau(p + n + 2n_i \cosh(\frac{E_T - E_i}{kT}))}$$

τ dependent on material: GaAs, Si (trap density)

$np > n_i^2$ $U > 0$ recombination

$np < n_i^2$ $U < 0$ generation

lifetime $\tau_r \neq \tau_g$

U_{max} for $E_T = E_i$

Surface of silicon with traps lead to the surface recombination velocity, which affects carrier lifetime

$$s = \sigma_s v_{th} N_{it}$$

$$U = \frac{s(np - n_i^2)}{p + n + 2n_i \cosh(\frac{E_T - E_i}{kT})}$$

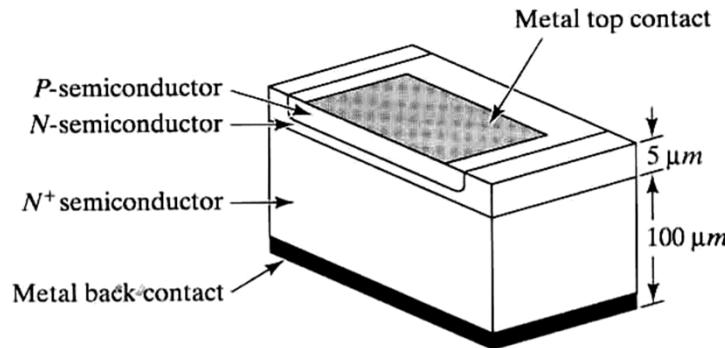
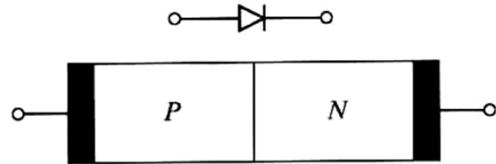
s Surface recombination velocity (cm/sec)

σ_s Cross section of surface trap (cm^2)

v_{th} Thermal velocity (cm/s)

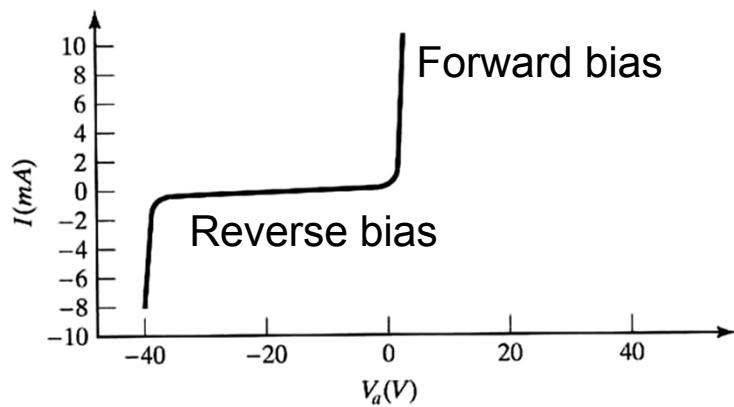
N_t Surface density of traps (cm^{-2})

p-n Diodes

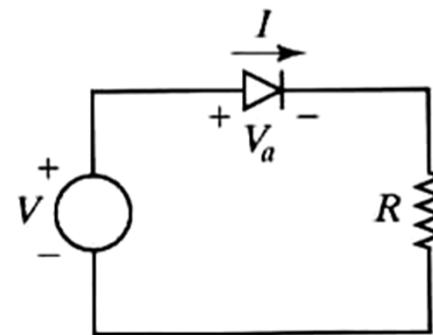


n^+ for low resistance

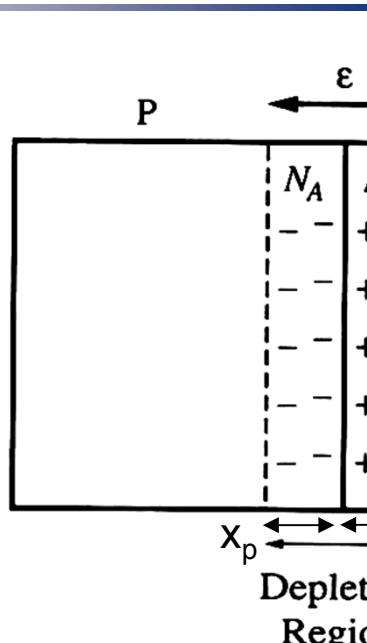
I-V curve



Equivalent circuit



p-n Diodes at Thermal Equilibrium



Electric field
only in the
depletion layer

At thermal equilibrium charge
neutrality

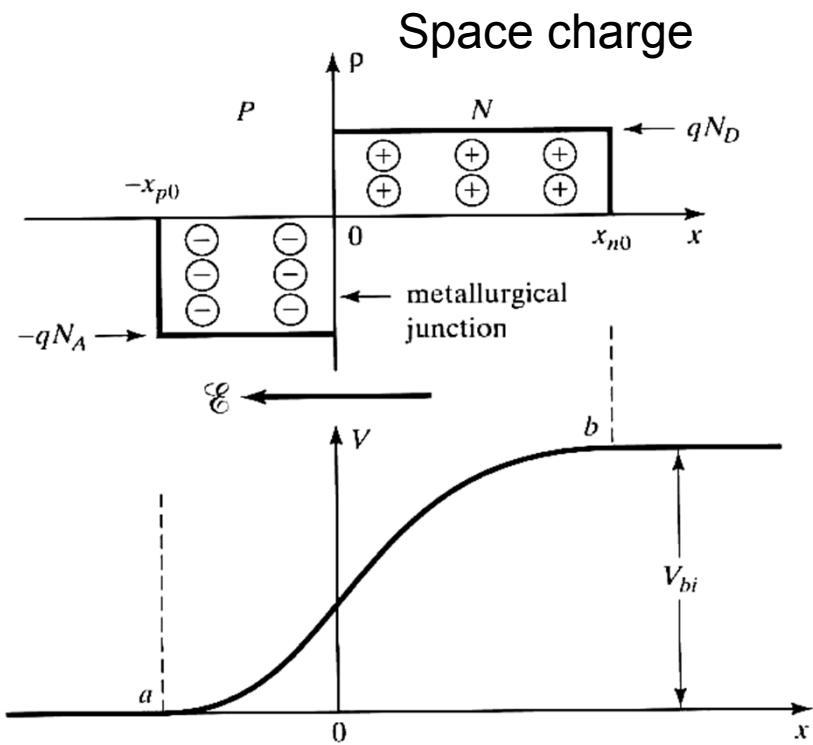
$$qN_d^+x_n = qN_A^-x_p$$

If $N_D \neq N_A$, asymmetrical depletion layers

Junction Capacitance

$$C = A \frac{\epsilon_s}{x_d} = A \sqrt{\frac{q\epsilon_s}{2} \left(\frac{N_A N_D}{N_A + N_D} \right) \frac{1}{(\phi_i \pm V)}}$$

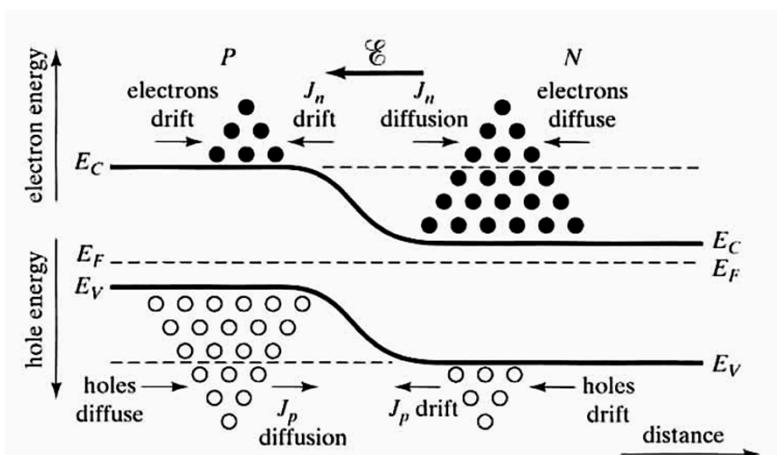
p-n Diodes at Thermal Equilibrium



Build-in voltage determined by doping on both sides of the p-n junction

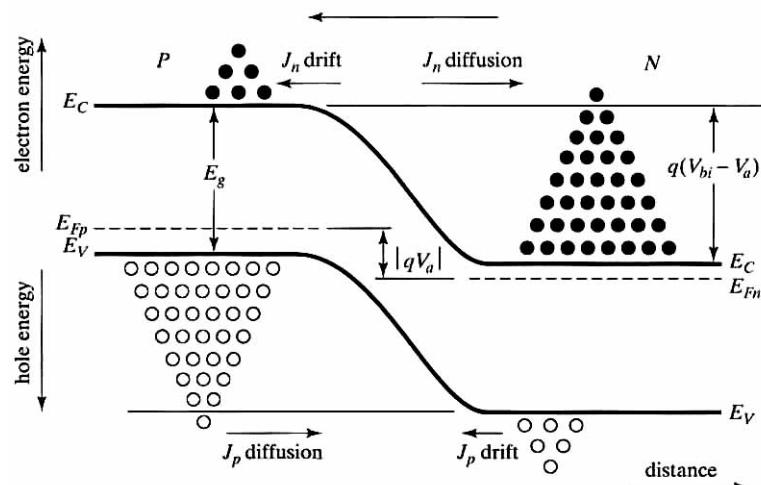
$$\phi_i = \frac{kT}{q} \ln \left(\frac{N_D N_A}{n_i^2} \right)$$

Carrier motion at equilibrium



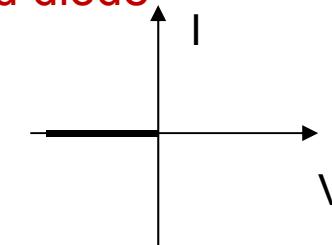
No current flows at thermal equilibrium

p-n Diodes Under Bias

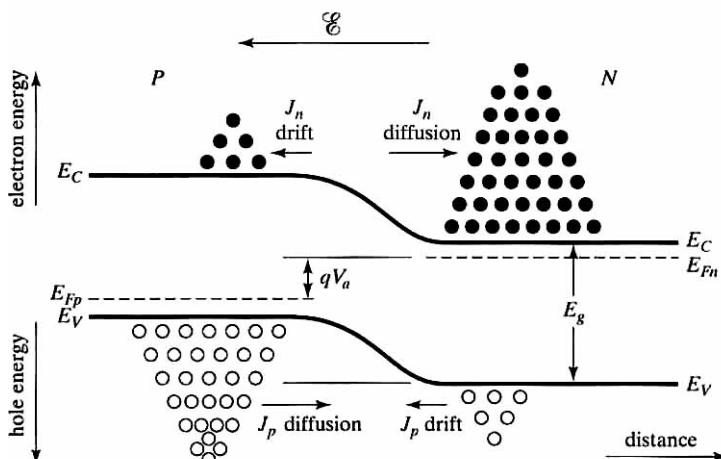


Reverse biased diode

(- +)

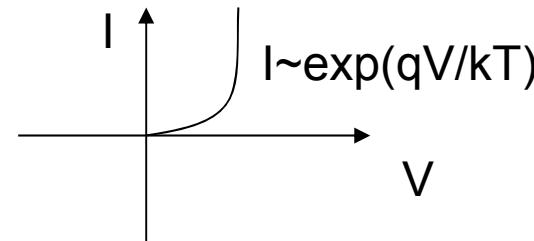


Minority electrons and holes drift
(small current)



Forward biased diode

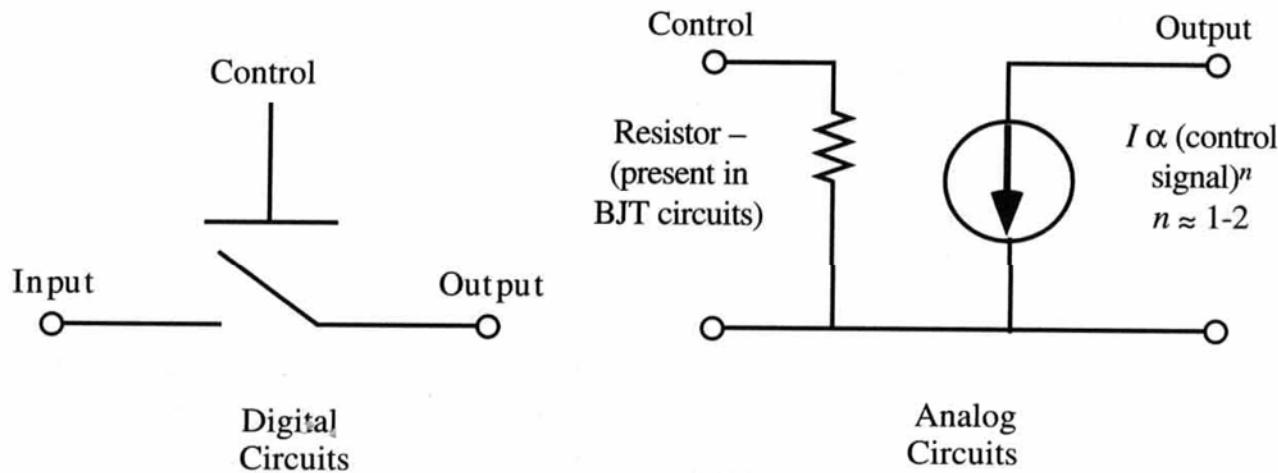
(+ -)



Majority electrons (and holes) diffuse,
become minority carriers and produce
large current

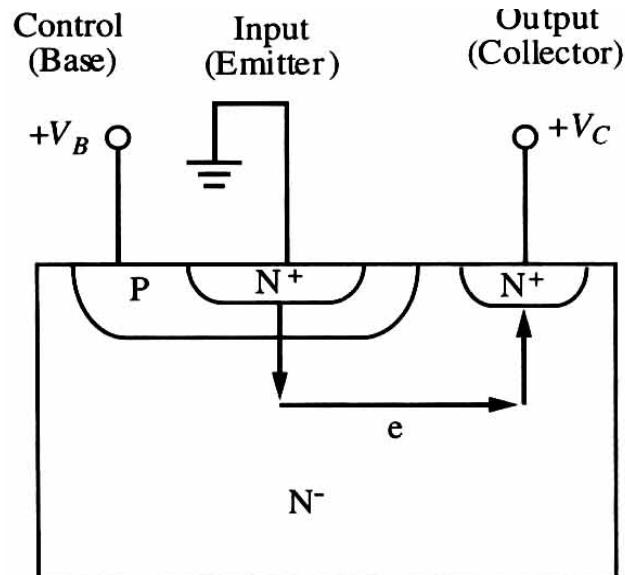
Transistors for Digital and Analog Applications

MOSFET and Bipolar Junction Transistors

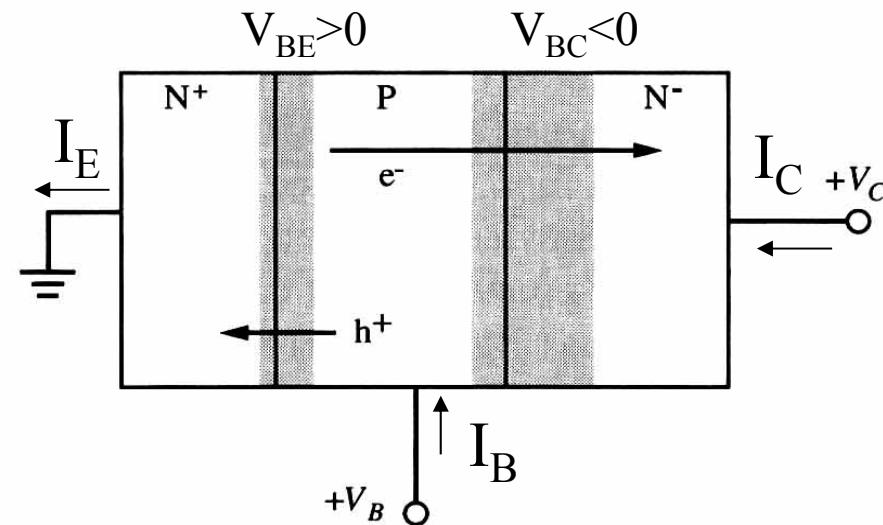


- In digital circuit, a switch is closed and opened by an isolated control terminal
 - In analog circuit, an input signal is amplified and transferred to the output
-

Bipolar Junction Transistors (BJT)

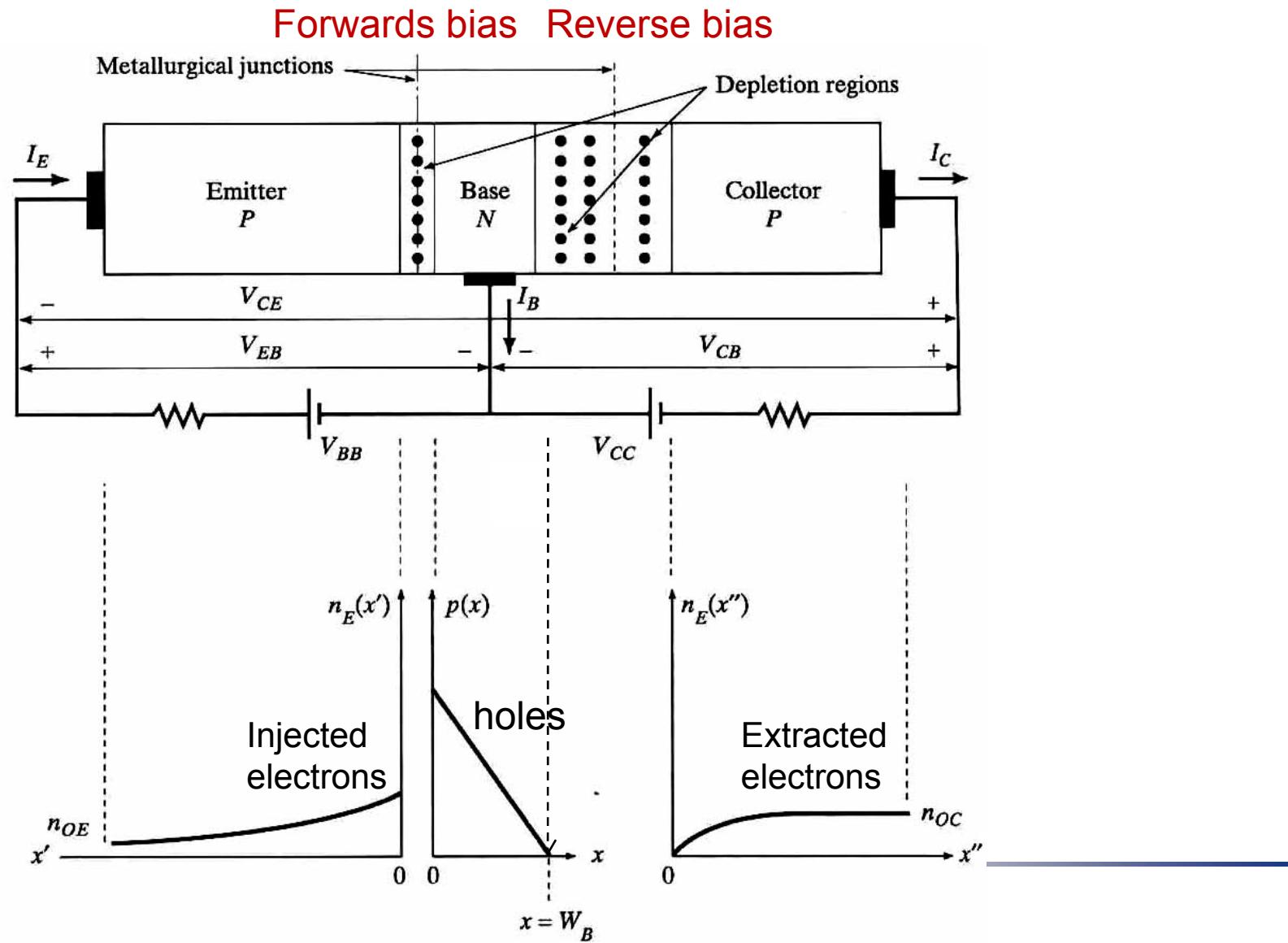


First investigated in 1940s

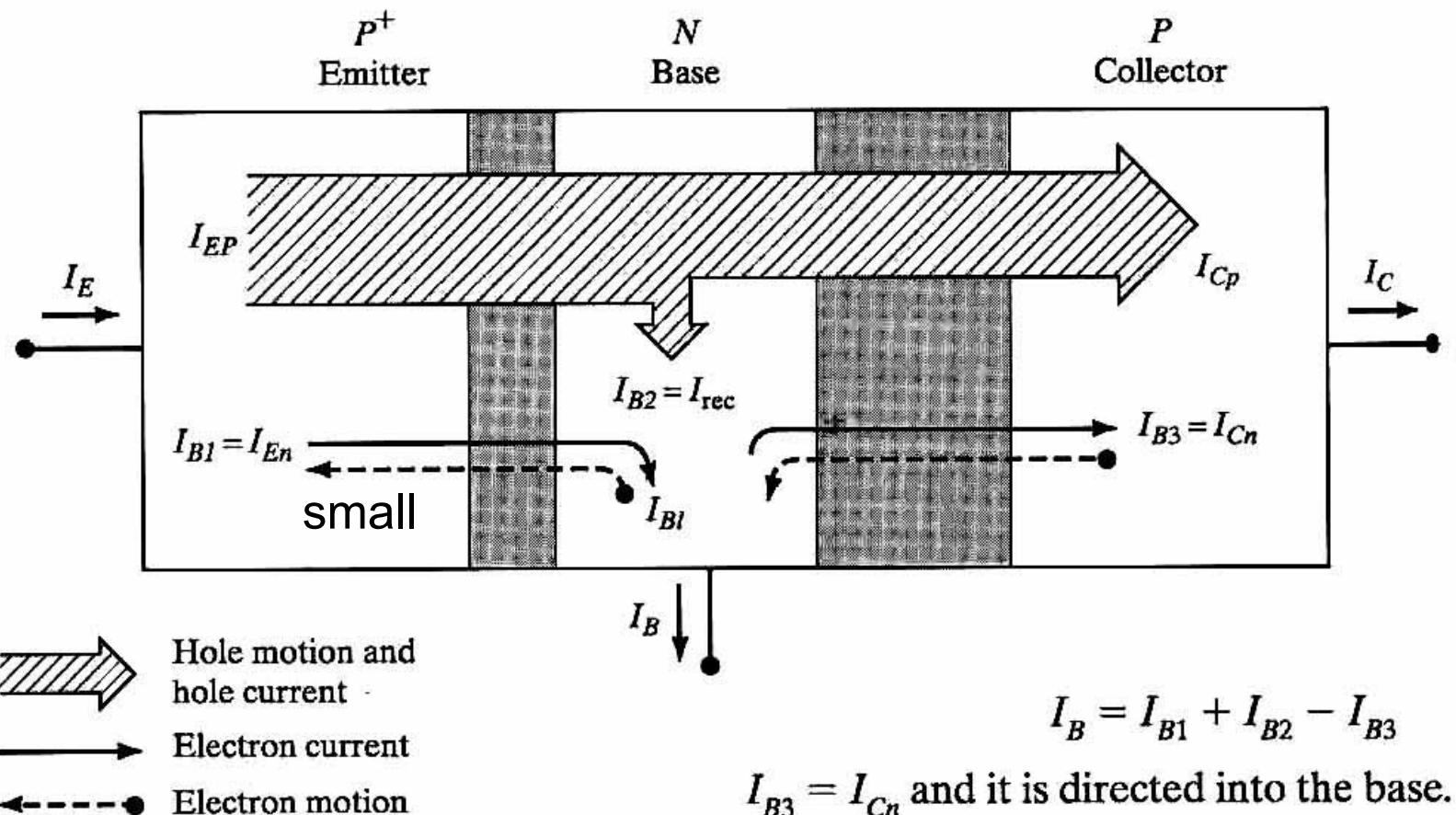


- E-B junction is forward biased and minority carriers are **injected** to the base
- Base is responsible for electron transport via **diffusion** to collector
- C-B diode is reverse biased and **collects** transported carries

Minority carriers distribution



Currents' Components



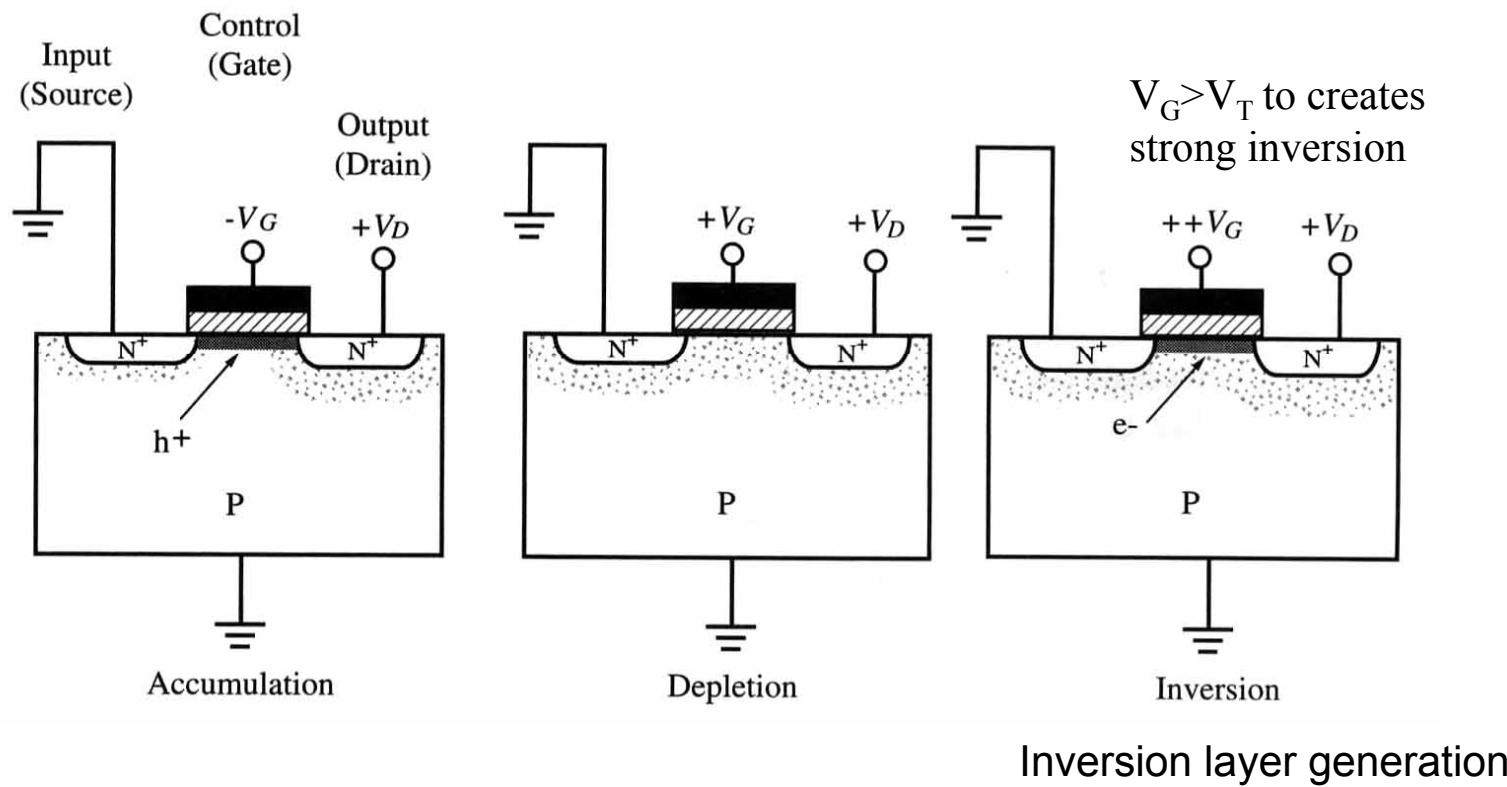
$$I_B = I_{B1} + I_{B2} - I_{B3}$$

$I_{B3} = I_{Cn}$ and it is directed into the base.

MOS Field Effect Transistors (MOSFET)

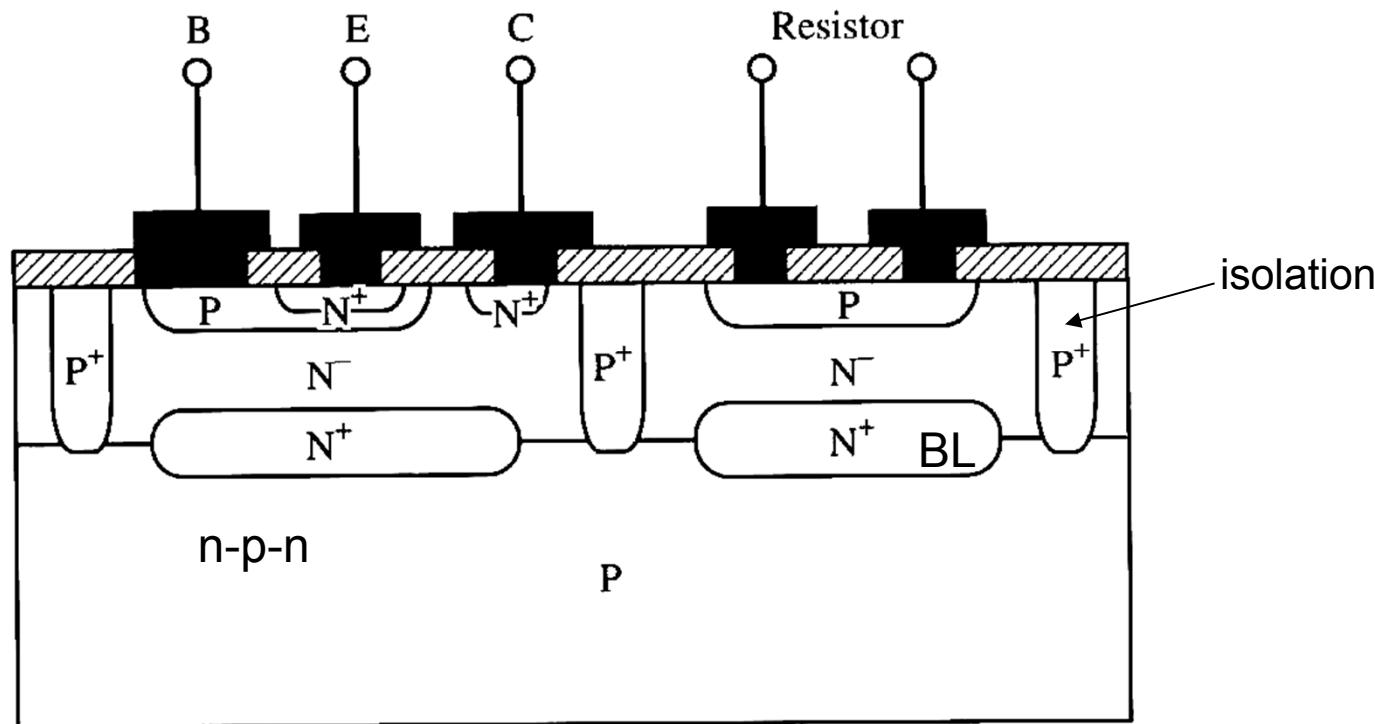
MOSFET includes NMOS and PMOS (used in CMOS circuits)

First investigated in 1930s



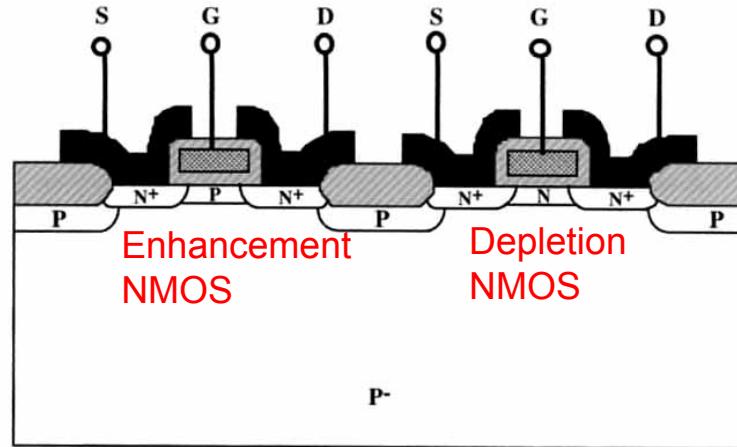
Semiconductor Technology Families

First circuits were based on BJT as a switch because MOS circuits limitations related to **large oxide charges**



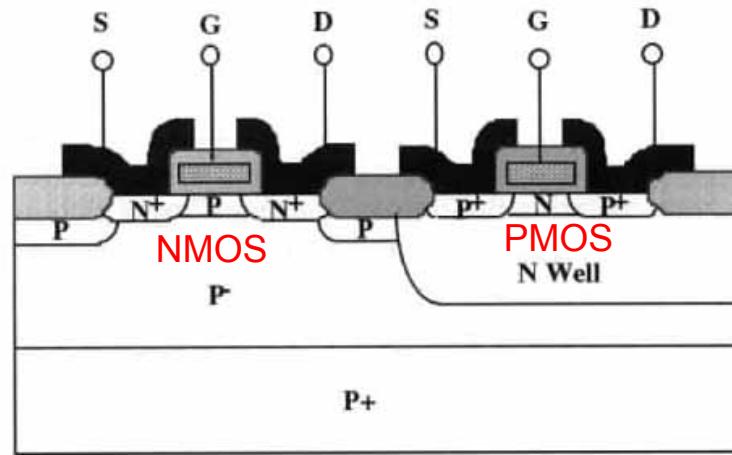
In 1960s, bipolar transistors and resistors were the dominant components

Semiconductor Technology Families



In 1970s, enhancement NMOS and depletion NMOS were the dominant components

Smaller power consumption



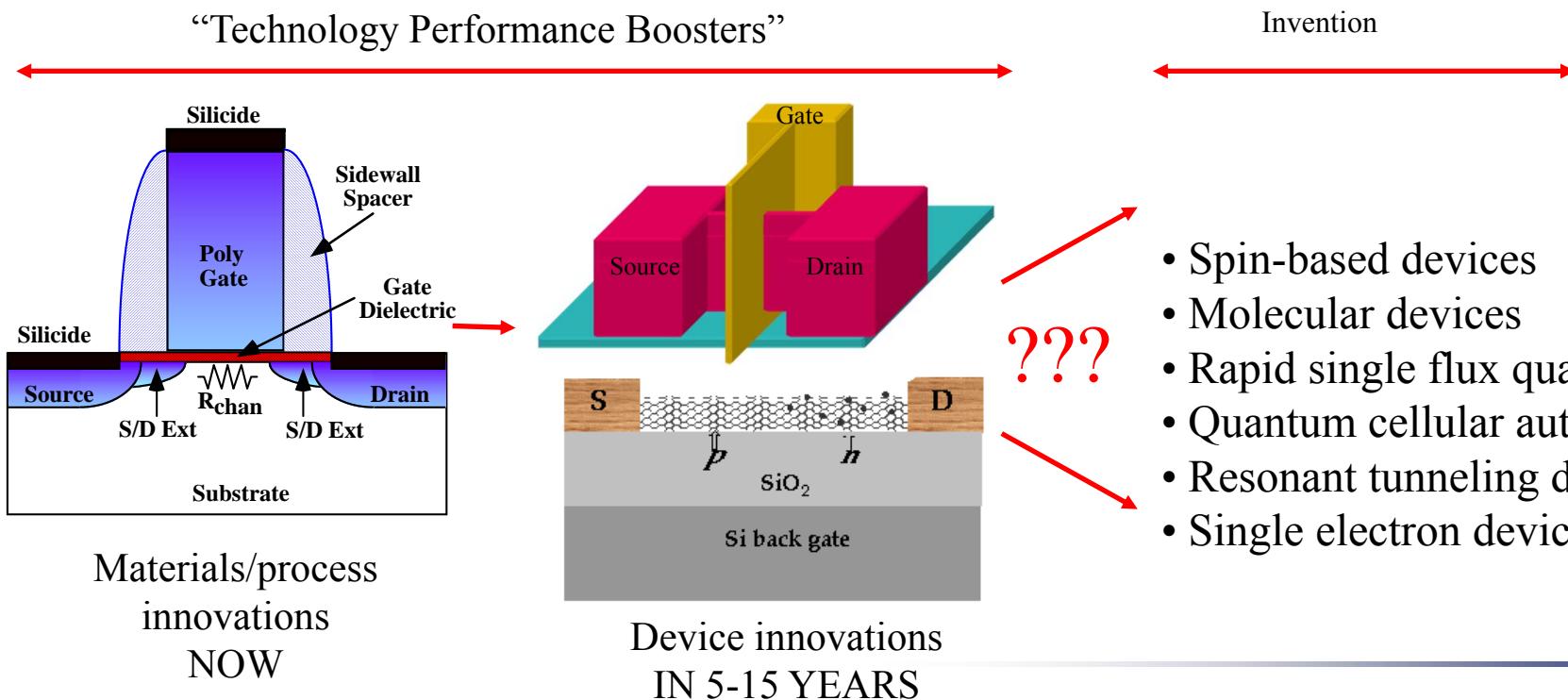
In 1980s, CMOS circuits with NMOS and PMOS devices were the dominant components

In 1990s, BiCMOS with internal circuitry of CMOS and output devices of BJT

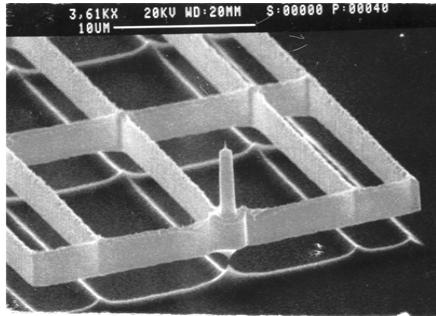
Challenges For The Future

- Having a “roadmap” suggests that the future is well defined and there are few challenges to making it happen.
- The truth is that there are enormous technical hurdles to actually achieving the forecasts of the roadmap. Scaling is no longer enough.

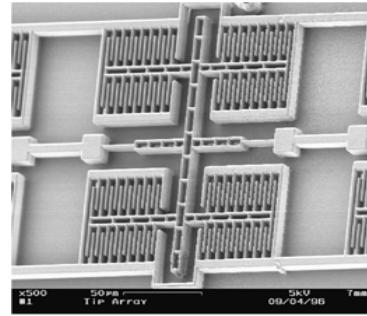
3 stages for future development:



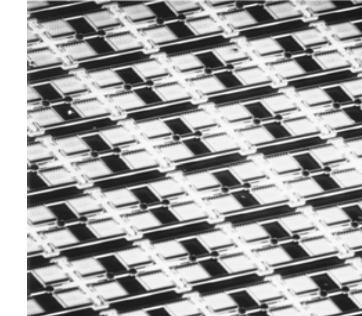
Broader Impact of Silicon Technology



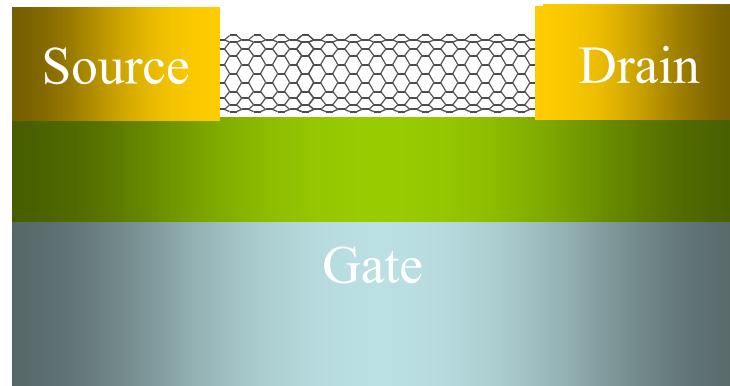
Tip on Stage



Individual Actuator



Part of 12 x 12 array



Many other applications e.g. MEMs and many new device structures e.g. carbon nanotube devices, all use basic silicon technology for fabrication.

Summary

- ICs are widely regarded as one of the key components of the information age.
 - Basic inventions between 1945 and 1970 laid the foundation for today's silicon industry.
 - For more than 40 years, "Moore's Law" (a doubling of chip complexity every 2 years) has held true.
 - CMOS has become the dominant circuit technology because of its **low DC power consumption, high performance** and **flexible design options**.
 - Silicon technology has become a basic “toolset” for many areas of science and engineering.
-