Winchester Zhang

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EDUCATION

M.Eng. in Electrical and Computer Engineering, Cornell University, NY — Aug. 2022 – Dec. 2023

Exchange Student in Computer Engineering&Physics, Linköping University, Sweden — Jan. 2021 – Jan. 2022

B.Eng. in Electrical Engineering, South China University of Technology, China — Sept. 2018 – July 2022

SKILLS

Languages: HDL(SystemVerilog/Verilog/VHDL), Python, C/C++, Assembly(RISC-V/x86/ARM), TCL, Perl, Ruby
Tools: Synopsys(ICC2/DC/PT/STAR-RC/VCS), Cadence(Innovus/Virtuoso/Allegro/OrCAD), MATLAB, Vivado, Quartus, Calibre, Redhawk
Equipment: Spectrum Analyzers, Oscilloscope, Power Supplies, Signal Generators, Logic Analyzers, SPICE
Knowledge: Linux, VLSI, UVM, OOP, DSP Processor, ECO, Out of Order, PnR, SRAM Design, STA, ASIC

PROFESSIONAL EXPERIENCE

LIN-RS232 Radar Transition Box: Allegro/DC-DC/LDO/SWD Debug/SoC interfaces **05/2023 – 08/2023**

Assistant Hardware Engineer Intern | VIA Technologies

- Engineered a Radar Transition Box integrating x4 LIN interface, UART, and RS232, enhancing system reliability through seamless data communication.
- Designed and optimized PCB with DC/DC converters and LDOs, complemented by a 3D-printed enclosure.
- Acquired in-depth insights into vehicle electronics, focusing on emerging trends, advanced technologies, and industry best practices, particularly in enhancing vehicle performance and safety.
- Led and managed the project lifecycle, coordinating cross-functional teams to achieve a 10% improvement in system optimization.

PROJECT EXAMPLE

RISC-V Processor and Cache System Development - Computer Architecture

- Developed a 5-stage pipelined processor based on the Tiny RISC-V instruction set, integrating advanced stall and bypass mechanisms for optimized performance and efficiency.
- Implemented a 2-way set associative write-allocate data cache (D-cache) and instruction cache (I-cache) with an LRU (Least Recently Used) replacement policy, enhancing memory access speed and efficiency.
- Designed sophisticated FSM-based cache controllers, crucial for managing the complexities of 2-way set associative caches and ensuring the effective implementation of the LRU policy.
- Skillfully handled both data and control hazards in the microarchitecture to maintain consistent and efficient execution of instructions.
- Employed a Verilog system integration testbench and a FL cache bypass module for system validation, using the latter as a benchmark for testing cache functionality.
- Executed comprehensive testing strategies, achieving 100% line and toggle coverage, to ensure the reliability and efficiency of both baseline and alternative cache designs.
- Adhered to core design principles, focusing on modularity, hierarchy, encapsulation, and a clear control/datapath split, following agile methodologies for iterative development and refinement.

FPGA-Based Digit Recognition System - High-Level Digital Design Automation

- Designed and implemented a k-NN based Digit Recognition System on Xilinx Zynq SoC, utilizing Vivado HLS for optimizations and deployment on ZedBoard.
- Operated within a Linux environment for development and testing.
- Created three design versions: a baseline model, a performance-enhanced unrolled design, and a version with advanced hardware-specific optimizations like pipelining.
- Enhanced hardware efficiency by minimizing communication overhead and streamlining FPGA implementation and bitstream generation for ZedBoard.

Physical Implementation of TSMC 28nm Low-Power Quad-Core A7 Top Hierarchical Flow - (Ongoing)

- Expert in TSMC 28nm low-power Quad-Core A7 CPU design, focusing on low-power strategies and UPF scripting.
- Managed floorplanning, power planning, and clock latency optimization for reduced power leakage.
- Proficient in Latten RC extraction, Flatten DRC checking, and PrimeTime timing adjustments.
- Ensured design integrity with various checks and implemented Dummy Insertion Flow for RC extraction.
- Maintained compliance with CPU subsystem power distribution and IR Drop specifications.
- Conducted timing consistency analyses between PrimeTime and Place&Route, ensuring optimal performance.