The NSP for Vayu library supports the following

- **NDK Hardware HAL implementation (NIMU APIs)**
- **High performance APIs for raw data RX/TX (bypassing NDK stack)**
- **Ethernet GMACSW driver**

Description

The Network Development Kit Support Package (NSP) contains the ethernet driver implementation which plugs into the TI Network Development Kit (NDK)

Summary of performance

Target Platform Name: TDA2xx (Vayu)
CPU Cores: IPU1 (Cortex M4)
Frequency: 212 MHz

Table 1. Configuration Table

COMPONENT CONFIGURATION DESCRIPTION	ID
Raw data API Data rate: 280Mbps	1
Raw data APIs Data rate: 800Mbps	2

Table 2. Cycles Information

CONFIGURATION ID	PERFORMANCE STATISTICS (PERCENTAGE)	
	TEST DESCRIPTION	AVERAGE
1	HWI Load	3%
2	HWI Load	7%

Table 3. Memory Statistics

CONFIGURATION ID	MEMORY STATISTICS [6]				
	PROGRAM MEMORY	DATA MEMORY			TOTAL
		INTERNAL	EXTERNAL	STACK	
ALL	20.2K	0	9.25	4	33.45

[6] All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes).

Table 4. Internal Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – INTERNAL [7]		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
ALL	0	0	0

[7] All memory requirements are expressed in kilobytes.

Table 5. External Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – EXTERNAL [8]		
	SHARED		INSTANCE
	CONSTANTS	DATA	
ALL	0	9.25	0

[9] All memory requirements are expressed in kilobytes.

Table 6. EDMA Channels Usage

CONFIGURATION ID	EDMA CHANNELS		
	CHANNEL NUMBER	INTERRUPT ENABLED	AVG. REQUEST (MBYTES/SEC)
ALL	NONE	NA	NA

Table 7. Peripheral Usages

CONFIGURATION ID	PERFORMANCE STATISTICS (NANO SECONDS / MICRO SECONDS)		
	TEST DESCRIPTION	LATENCY	THROUGH-PUT
NA	NA	NA	NA

Table 8. TASKs & Priorities Usage

CONFIGURATION ID	TASKS			
	PROCESSOR	TASK NAME	TASK PRIORITY	TASK LOAD
1	Cortex M4	rxPacketTask	14	21%
2	Cortex M4	rxPacketTask	14	57%

Table 9. HWI/SWI & Priorities

CONFIGURATION ID	HWI/SWI			
	PROCESSOR	HWI/SWI HANDLER	INTERRUPT VECTOR	XBAR SOURCE (IF ANY)
ALL	CORTEX M4	HwIntRx	58	NA
ALL	CORTEX M4	HwIntTx	59	NA

ALL	CORTEX M4	HwIntRxThresh	57	NA
ALL	CORTEX M4	HwIntMisc	60	NA

Table 10. MMU or AMMU CONFIGURATION

CONFIGURATION ID	MMU OR AMMU				
	PROCESSOR	SECTION TYPE	START ADDRESS	SIZE	POLICY (IF ANY)
NA	NA	NA	NA	NA	NA

Glossary

Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Data	Memory that go into .data and .bss sections
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

NSP	Network Support Package
NDK	Network Development Kit

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