hw4: The Memory Hierarchy

Due Oct 30 at 11:59pm **Points** 8 **Questions** 8
Available until Oct 30 at 11:59pm **Time Limit** 40 Minutes
Allowed Attempts 3

This quiz was locked Oct 30 at 11:59pm.

Attempt History

	Attempt	Time	Score
KEPT	Attempt 3	13 minutes	8 out of 8
LATEST	Attempt 3	13 minutes	8 out of 8
	Attempt 2	19 minutes	6 out of 8
	Attempt 1	22 minutes	7 out of 8

Score for this attempt: **8** out of 8
Submitted Oct 30 at 11:34pm
This attempt took 13 minutes.

Question 1

1 / 1 pts

Assume the following sequence of blocks are fetched into the *same set* of a 4-way set associative cache that is initially empty:

```
b7,b5,b1,b5,b4,b5,b7,b4,b8,b8,b7,b8,b9,b1,b1,b7,b1,b8,b1,b2,b9,b9,b5,b2
```

Assume the placement policy is increasing line order (i.e., line 0 to line 3), and the replacement policy is random. After the sequence completes, which one below lists a possible result for the lines ordered from line 0 to line 3?

`b1, --, b7, b2`

where -- means unused

Correct!

- [x] `b7, b2, b1, b4`
- [ ] `b2, b9, b2, b5`
- [ ] `b7, b5, b9, b1`
- [ ] `b2, b7, b6, b9`

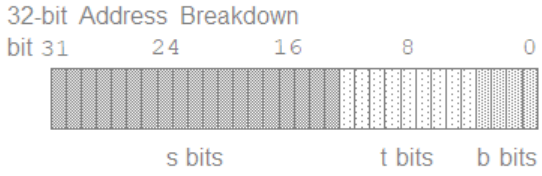
Question 2

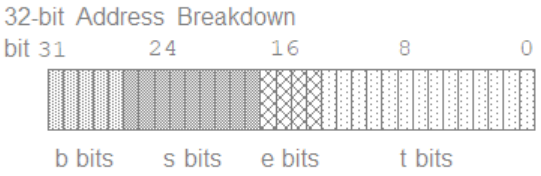
1 / 1 pts

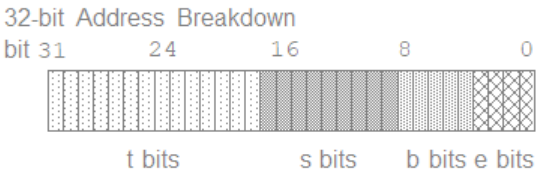
Consider the following characteristics of a cache memory system:

- Addresses are 32 bits.
- The memory is byte addressable.
- The CPU accesses 4-byte words.
- Blocks have 32 bytes.
- The cache is 16-way set associative with 512 sets.

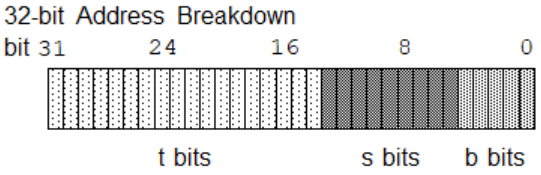
Which one of the following shows the address breakdown for an efficient cache implementation having the characteristics above?

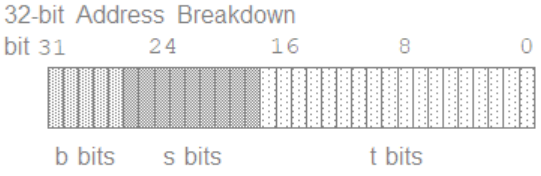
- [ ) 





Correct!





Question 3

1 / 1 pts

Which of the following exhibit spatial locality:

1. Sequencing control flow
2. Linear search on an array of integers
3. Accessing the first element of each row in a 2D array that is heap allocated as an array of arrays

- 1 only
- 1, 2 and 3
- 3 only

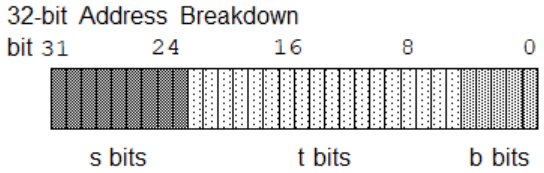
Correct!

- 1 and 2
- 1 and 3

Question 4

1 / 1 pts

Consider a 64KB cache that uses the following unusual address breakdown:



Assume the following code runs on this caching system:

```
int total = 0;
int *heapArray = malloc(sizeof(int) * 4096); //int is 4 bytes
for (int i = 0; i < 4096; i++)
    total += heapArray[i];
```

What is the maximum number of memory blocks for the array that are stored in the cache at any point in time?

- 1
- 2
- 512
- 256
- 1024

Correct!

- 4

Question 5

1 / 1 pts

Consider the following three code fragments; assume that the stack allocated array is initialized so that all indexing is in bounds.

```
//Code Fragment 1:
for (int hour = 0; hour < 24; hour += 2) {
    for (int elev = 0; elev < 16000; elev += 1) {
        for (int count = 0; count < 200; count += 1) {
            total = array[hour][elev][count];
        }
    }
}
```

```
//Code Fragment 2:
for (int hour = 0; hour < 24; hour += 1) {
    for (int elev = 0; elev < 16000; elev += 1) {
        for (int count = 0; count < 200; count += 1) {
            total = array[hour][elev][count];
        }
    }
}
```

```
//Code Fragment 3:
for (int hour = 0; hour < 24; hour += 1) {
    for (int elev = 0; elev < 16000; elev += 1) {
        for (int count = 0; count < 200; count += 50) {
            total = array[hour][elev][count];
        }
    }
}
```

Which one of the following orders the code fragments above from best to worst use of spatial locality?

- 1, 2, 3
- 3, 1, 2
- 1, 3, 2
- 2, 1, 3

Correct!

2, 3, 1

3, 2, 1

Question 6

1 / 1 pts

Consider a cache characterized as (8, 1, 8, 14). If the contents of the cache are as follows where the Tag and byte values are given in hexadecimal.

Set Index	Tag	Valid	Byte 0	Byte 1	Byte 2
0	09	0	A0	30	E0
1	45	1	9D	43	3F
2	EB	1	43	D4	84
3	06	0	64	45	99
4	C7	0	33	23	16
5	71	1	FF	74	CC
6	91	1	EB	A4	E2
7	46	1	4C	A7	DD

What byte value, if any, is accessed by the address `0x0E36`?

EF

23

CC

Correct!

cache miss

81

Question 7

1 / 1 pts

The following table gives the parameters for a cache.

C	S	E	B	m	t	s	b
W	512	4	**X**	**Y**	49	**Z**	6

Answer the following questions

1. The value of **W** is [Select]
2. The value of **X** is [Select]
3. The value of **Y** is [Select]
4. The value of **Z** is [Select]

Answer 1:

Correct!

128K

Answer 2:

Correct!

64

Answer 3:

Correct!

64

Answer 4:

Correct!

9

Question 8

1 / 1 pts

Consider an intentionally small cache characterized by (4, 2, 8, 16) that is initially empty. Given an array of 8 integers that starts at address 0x8090, accessing the array elements in this order:

```
array[0], array[1], array[2], array[3], array[1]
```

would result in which one of the following?

- miss, miss, hit, hit, miss
- hit, hit, hit, hit, hit
- **Correct!** miss, hit, miss, hit, hit
- miss, miss, miss, miss, hit
- miss, hit, hit, hit, hit

Quiz Score: **8** out of 8