1) **Cooperative multi-tasking** requires hardware support for a timer interrupt.

False: if cooperative, only switch when process enters OS through other means (e.g., system calls)

2) Two processes reading from the **same virtual address** will access the same contents.

False: processes have different address spaces, so different contents

3) The **convoy effect** occurs when longer jobs must wait for shorter jobs.

False: occurs when shorter jobs must wait for longer jobs

11)With pure segmentation (and no other support), fetching and executing an instruction that performs an

add of a constant value to a register will involve exactly **two memory references**.

False, just one memory reference; pure segmentation implies physical address can be computed by just

determing the segment and adding the virtual offset within this segment to the physical base for this segment

(i.e., no memory references needed to calculate physical address); fetching the instruction then takes one

memory reference and the add itself does not perform more memory references

16) A **TLB miss** is usually slower to handle than a **page miss**.

False; TLB miss just requires memory references to walk the page tables; a page miss requires fetching that

page from disk

17) A single page can be **shared** across two address spaces by having each process use the same page table.

False; to share a page, just share one entry of a page table (using the same page table would share the whole

address space).

18)If the **present bit** is clear (equals 0) in a PTE needed for a memory access, the running process is likely

to be killed by the OS.

False; present bit = 0 means the page is on disk and not in main memory, so the page just needs to be

fetched.

19)TLBs are more beneficial with **multi-level page tables** than with linear (single-level) page tables.

True; without a TLB, with multi-level page tables, many memory references are needed to translate each

address.

1)

Two processes reading from the same physical address will access the same contents.

**True – they must have a mapping so share a page so potentially different virtual addresses in**

**each of their address spaces point to the same physical address.**

4)

If all jobs have identical run lengths, a RR scheduler (with a time-slice much shorter than the jobs’ run

lengths) provides better average turnaround time than FIFO.

**False – with RR, identical jobs will all finish at nearly the same time (at the very end of the**

**workload time), which has very poor average turnaround time.**

5)

The longer the time slice, the more a RR scheduler gives similar results to a FIFO scheduler.

**True – In the extreme, when the time slice is >= the length of the job, RR degenerates to FIFO**

**(or FCFS).**

8)

With a single-level page table (and no other support), fetching and executing an instruction that performs

an add of a constant value to a register will involve exactly two memory references.

**True – 1st memory reference is to page table to translate vpn to ppn (no TLB support); 2nd**

**memory reference is to fetch the instruction.**

15)If the valid bit is clear (equals 0) in a PTE needed for a memory access, the desired page will be swapped

in from the backing store.

**False; if the present bit is 0, the page resides on the backing store; if the valid bit is 0, this isn’t a**

**valid virtual address at all.**

16) TLBs are more beneficial with multi-level page tables than with linear (single-level) page tables.

**True, because the cost of walking a multi-level page table is higher than walking a single level**

**(i.e., more memory accesses are needed)**

17)When the dirty bit is clear (equals 0) in a PTE needed for a memory access, an identical copy of the

desired page resides in the backing store.

**True; if dirty bit is clear, then the page is clean, which means the page in memory can be**

**discarded on replacement because its contents reside on the backing store (disk).**

18) LRU with N+1 pages of memory always performs better than LRU with N pages of memory.

**False; LRU performs as well or better with N+1 pages (might perform the same).**

19) FIFO with N+1 pages of memory always performs better than FIFO with N pages of memory.

**False; FIFO with N+1 pages can even perform worse.**

4) An MLFQ scheduler assumes the presence of an oracle that knows the length of a job’s CPU burst in advance. False; the schedule dynamically adjusts the time slice based on past behavior of that job 5) The fork() system call creates a child process whose execution begins at the entry point main(). False; child starts execution as if returning from fork(). 6) A process can close() the stdout file descriptor. True; this is how you can implement stdout redirection to a file 7) With dynamic relocation, the OS determines where the address space of a process is allocated in virtual memory. False; OS picks location in physical memory; compiler generates all addresses in virtual memory 8) With dynamic relocation, the OS can move an address space after it has been placed in physical memory. True; just copy data in physical memory and then change base register in MMU. 9) A Gantt chart illustrates how virtual pages are mapped to physical pages False; Gantt charts show scheduling of jobs over time. 10)With pure segmentation (with no paging or TLBs), each segment of each process must be allocated contiguously in physical memory. True; each segment must be contiguous with its own base and bounds register