Assignment #4
EECS 303: Advanced Digital Logic Design

Problem 1. 100 Points

1. **Background**: Design your own simple arithmetic logic unit (ALU). Refer to the slide 58 in Lecture 7 on Arithmetic Circuits as your reference.

2. **Description**:
    a. Inputs: a (8 bits, unsigned), b (8 bits, unsigned), F (3 bits, used to select the functions of ALU);
    b. Output: Q (8 bits, unsigned), Cout (1 bit, carry bit for Add or borrow bit for Sub);
    c. Realize the following function of ALU:
        i. F=000, Q=a+b;
        ii. F=001, Q=a-b;
        iii. F=010, Q=a OR b;
        iv. F=011, Q=a AND b;
        v. F=100, Q=a XOR b;
        vi. F=101, Q=NOT a;
        vii. F=110, Q=arithmetic left shift of a by 1 bit;
        viii. F=111, Q=arithmetic right shift of a by 1 bit;
    d. All the ALU operations have to be finished within 1ns;
    e. You don't have to follow the schematic of slide. As far as your functionalities are the correct, it will be fine.
    f. Watch out Cout signal. It is the carry out bit for Addition and borrow bit for Subtraction. For example, for calculation of "7-3", the Cout should be 0, but for calculation of "3-7", the Cout should be 1. For calculation of "250+5", the Cout should be 0, for calculation of "250+6", Cout should be 1. One possible way is to define 9^{th} bit of output for your internal Adder. And use the 9^{th} bit with some additional logic to build the final Cout signal.

3. Deliverable: please write a report with required information from below.

(1). Following the lectures and tutorial, create all required design files including RTL, testbench, timing constraint SDC file. Attach all files to your submission.

(2). Use Xcelium to simulate your RTL using your testbench. Show the snapshots of the simulated waveforms (show all inputs and outputs signals) for each of the eight functions of the ALU. At least show one testcase (your choice) for each function of ALU. Do not use trivial cases such as all 0 inputs. Clearly mark the testing cases (mark or cycle the location of signals for the test cases) in your waveform. Correct functions should be shown.

(3). Perform synthesis. Report your area, cell counts, and timing slack. Attach snapshot of report_area and report_timing output.

(4). Repeat the step (2) by simulating your generated gate level netlist. Correct functions should be shown.

(5). Please copy and paste into your report all supporting files your created/edited in your submission including Verilog, testbench, SDC file.