Midterm Practice
CompEng 303, Advanced Digital Design

Problem 1. Concepts
State whether the following statements are TRUE or FALSE or provide a short answer. **If you mark a statement as FALSE, you have to provide a clarification, correction, or a contradicting example to receive credit**.

1.1. Two-level logic minimization can be solved optimally in polynomial time, i.e., the amount of work required to solve this problem can be represented with a polynomial function with respect to the number of inputs of the logic function.

1.2. Assigning all decision variables to TRUE will provide a feasible (meaning functionally correct) answer to any unate covering problem.

1.3. MOS transistors operate at higher speed if their channels are as narrow as possible.

1.4. Procedural statements such as the "if … then … else" are used to code in RTL (a.k.a Dataflow) style of Verilog.

1.5. For NMOS transistor, if the gate voltage is low, the transistor switch is open.

1.6. How many transistors do the following standard cell gates need at the minimum: two-input OR2 gate _____ , three-input NOR3 gate _____.

1.7. To perform signed integer operations in Verilog, all operands and output need to be declared as signed integers.

1.8. In Verilog, "initial" statement is synthesizable.

Problem 2. 2-Level Logic Minimization Using KMaps

Given the truth table for the following function,

F(a, b, c, d)

a	b	c	d	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

a. Fill the K-Map given below
b. Identify all Prime Implicants
c. Identify the Essential Prime Implicants
d. Derive the minimal Sum of Products Expression for F

a.

cd

ab

	00	**01**	**11**	**10**
00				
01				
11				
10				

Problem 3. Unate Covering

We can generalize the unate covering problem by associating a **weight** (a nonnegative real number) with each column. The objective of this generalized problem then would be defined as ***minimizing the sum of the weights of the columns selected in the solution***.

Below is an example. The optimal solution to the unate covering problem for this table would be choosing Col1 and Col2, even though Col4 could cover all rows alone.

	Col1 (weight= 0.1)	Col2 (weight = 2)	Col3 (weight = 7.2)	Col4 (weight= 273.8)
Row1	1		1	1
Row2		1		1
Row3	1		1	1
Row4		1	1	1

How would you define the row dominance rule for this version of the problem?

Problem 4. Building custom CMOS Gates using transistors

Construct a custom CMOS transistor-based logic gate for the following logic operations: DO NOT SIMPLIFY EXPRESSION.

a. $F = \overline{(A+B)\,(B+C)\,(A'+C)}$

Problem 5. Verilog

Part a. Write a dataflow/RTL style module for the circuit described in Problem 2.

Part b. Write a structural style module for the circuit described in Problem 2 using basic logic gate primitives.