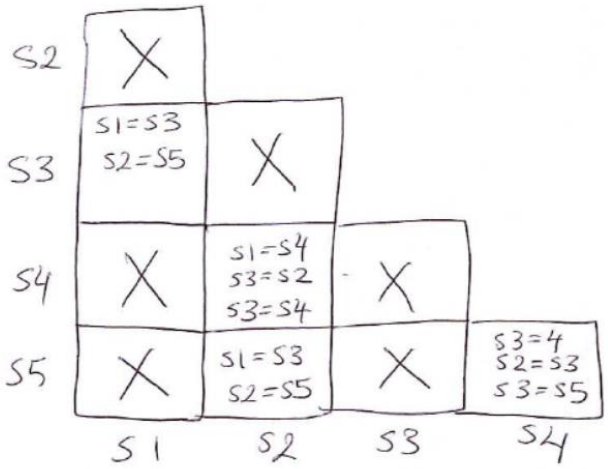
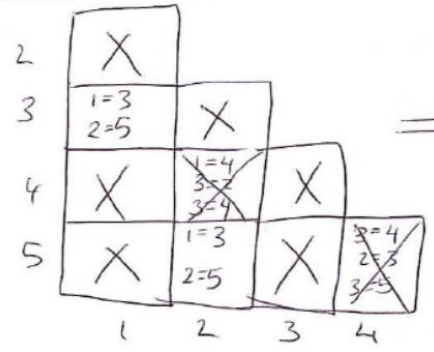
Problem. FSM Optimization Perform state reduction for the transition table below.

Present state	Next state				Output Z
	XY=00	XY=01	XY=10	XY=11	
S1	S3	S2	S4	S2	0
S2	S1	S3	S2	S4	1
S3	S1	S5	S4	S5	0
S4	S4	S2	S3	S3	1
S5	S3	S3	S5	S4	1

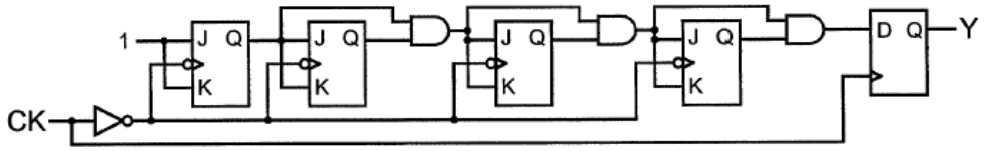


Second iteration :

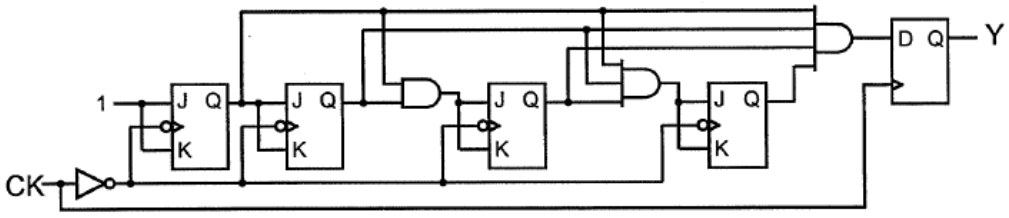


$\Rightarrow$ $S1 = S3$, $S2 = S5$ } equivalent states

Problem. Determine the minimum clock cycle time for each circuit shown below.



Circuit1



Circuit2

The gates and flip flops on the circuits have the following timing parameters:

JK Flip Flops: 6ns ≤ t_{pd} ≤ 20ns, t_{setup} = 22ns and t_{hold} = 5ns
D Flip Flops: 7 ns ≤ t_{pd} ≤ 25ns, t_{setup} = 15ns and t_{hold} = 8ns
All AND gates and inverters: 2 ns ≤ t_{pd} ≤ 5ns

Circuit 1:

The critical path for Circuit 1 starts at the second JK FF, goes through 3 AND gates (combinational data path) and ends at the input pin of the D FF

Since the first FF accepting the input is the JK FF, we use its propagation delay as the first term, followed by the delay of the combinational path (3xgate_delay_max) as the second term, followed by the setup time required by the FF (DD FF) that is accepting the output of the path. **Finally, there is an additive term equal to an inverter delay. This is the difference in the arrival time of clock between the first JK-FF at the head of this path and the DFF at the tail (notice that the CLK signal fed into the D-FF DOES NOT PASS THROUGH THAT INV). Since clock arrives at the JK-FF LATER than the D-FF at the end of the path, this will further constrain the path, because its end effect will be to "shorten" the total amount of time data has to "pass through the JK-FF and be processed by the combinational logic" and finally arrive at the D-FF within the expected limits of the setup time.**

$$T_c \geq t_{pd,\,JK} + 3t_{pd,\,AND} + t_{setup,\,D} + t_{pd,\,INV} = 5 + 20 + 15 + 15 = 55 \text{ ns}$$

Circuit 2:

In this circuit the longest path starts at one of the JK-FF passing through one AND gate and ends at another JK FF. The path between the second and the third JK-FF is one such path. The path starting at the third JK-FF and ending at the fourth is another one with same timing.

So, we start with the propagation delay of the first JK-FF, plus the combinational delay (one AND gate), plus the setup time of the JK-FF at the tail end of the path.

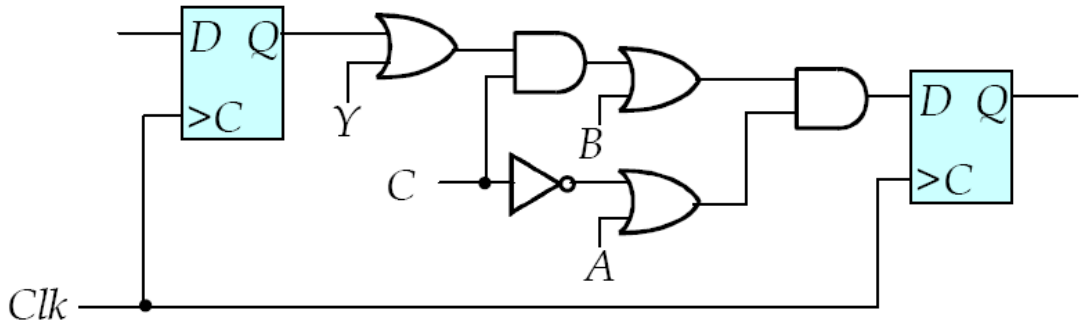
$$\mathbf{T_c \geq t_{pd,\,JK} + t_{pd,\,AND} + t_{setup,\,JK} = 20 + 5 + 22 = 47\ ns}$$

Notice that in this circuit clock signal delivered to both JK-FFs along the path experience the inverter delay for both Flip flops so that delay effect cancels out. Difference in clock arrival time exists between the first JK-FF and the D-FF, but that path is not the longest, hence does not determine clock period. Let's double check this fact:

$$\mathbf{Tc >= t_{pd,\,JK} + t_{pd,\,AND} + t_{setup,\,D} + t_{pd,\,INV} = 20 + 5 + 15 + 5 = 45}$$

This path is not the longest FF-to-FF path!

Problem Consider the circuit shown below. Assume that each gate has a maximum propagation delay of 2 ns and that the flip flop setup time constraint is 2 ns and that the flip flop propagation delay is 3 ns.

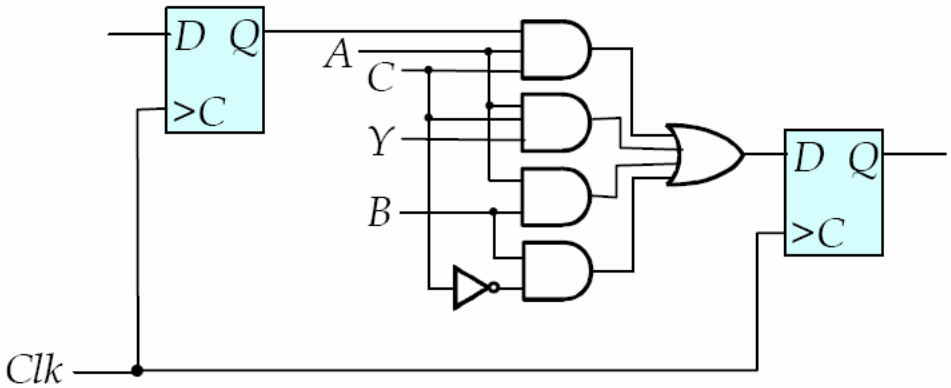


a. What is the fastest clock the circuit can run at?

Setup constraint: 4x2ns + 2ns + 3ns = 13ns <= Tclock

Fastest frequency is 76.92MHz

b. Show how to modify the circuit so that it can operate with a clock frequency of 100 MHz. You may restructure the circuit in any way you want. You may assume that any logic gate you may use will have 2ns propagation delay.



Problem PLA/PAL/ROM

(a) Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table for a BCD to seven segment decoder with enable input.

Problem Concepts

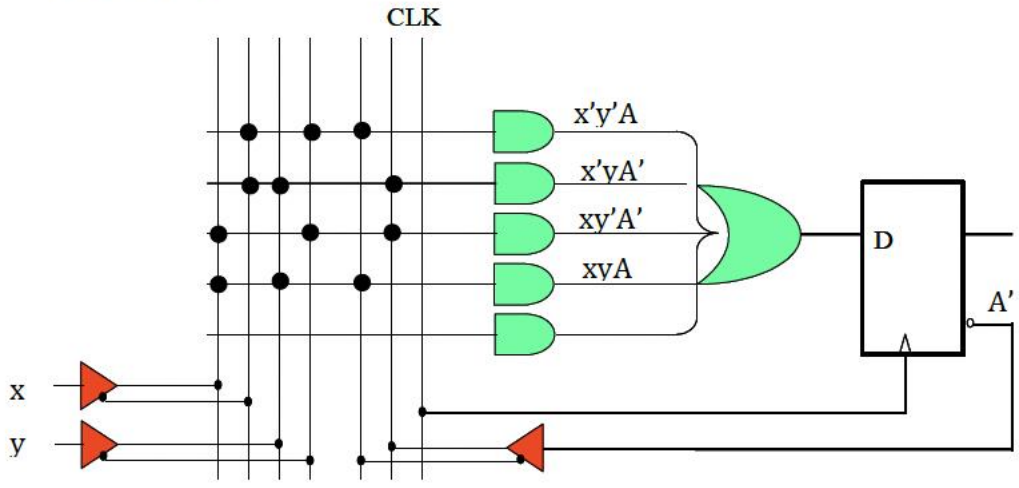
a. Is the Ripple Counter a synchronous circuit? Discuss Why or Why not.

b. Name two non-volatile memory technologies and briefly describe the concept behind their operation in a couple sentences each.

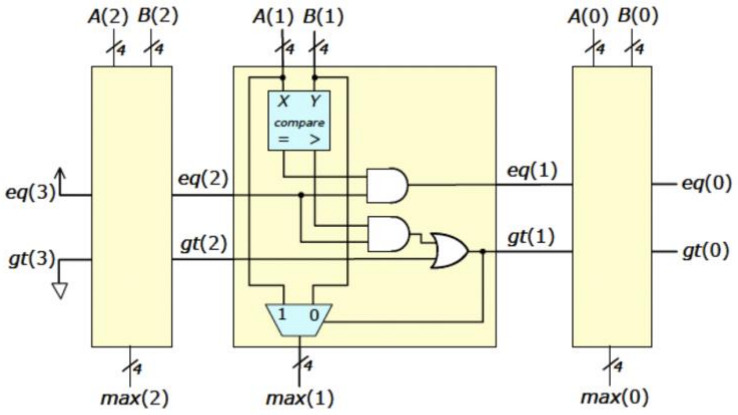
c. How can you remedy a hold time violation>

Problem. Programmable Logic Technology Using the macrocell shown below, show the fuse connections on the schematic to implement the sequential function F with two inputs x and y and one flip flop A described by the equation:

$D_A = x \oplus y \oplus A$



$D_A = x'y'A + x'yA' + xy'A' + xyA$



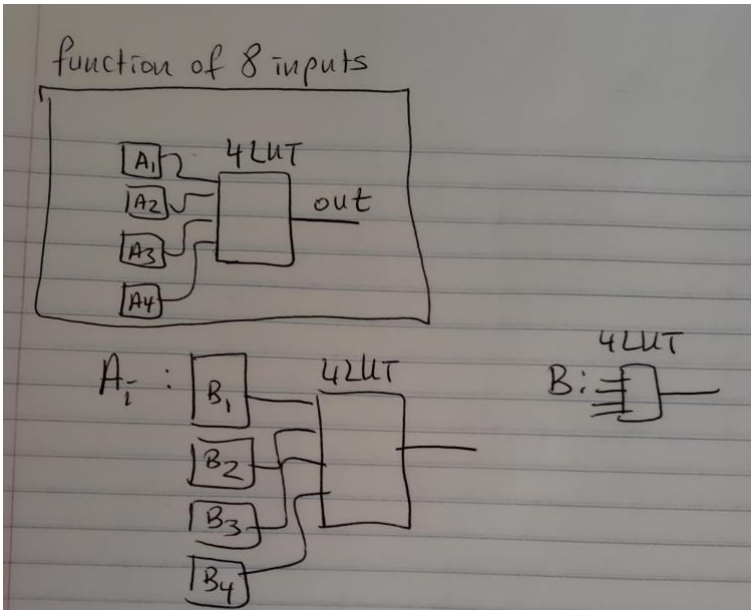
Estimate the number of 4 input LUTs needed to implement one stage of this circuit.

The compare block requires 21 4-LUTs for the equality comparison and another 21 for the greater-than comparison. The mux takes 4 LUTs: one 2x1 MUX is a function of three inputs, hence can be implemented with a single LUT. Since the inputs to the mux are 4-bits each we need to replicate this 4 times, and the outputs eq(1), gt(1) each require one LUT. So, the total is 48 LUTs per stage and 48x3 for the entire circuit.

See below the illustration of how the equal function (a function of 8 inputs which I have labeled as in0 through in 7, corresponding to the combination of 4 bits of A and 4 bits of B signals in the block diagram). Each block labeled Bi is 4LUT.

B1will be connected to (0, 0, in1, in0)
B2will be connected to (0, 1, in1, in0)
B3will be connected to (1, 0, in1, in0)
B4will be connected to (1, 1, in1, in0)

Bis will be connected to a 4LUT which configured as a 4x1 MUX
Ais, in turn, will also be connected to a 4LUT configured as a 4x1 MUX



Show how to build a 8-LUT using 4 6-LUTS and 3 2:1 MUX