Comp Eng 303 end of year quiz

19 plays • 87 players

A public kahoot

Questions (19)

1 - Quiz

Which of the following answers lists two types of programmable devices that are only combinational?

30 sec

- PLA, PAL ✓
- PAL, PLD ✗
- FPGA, ROM ✗
- ROM, PLD ✗

2 - Quiz

How can you remedy a hold time violation? Select all correct answers.

20 sec

- By increasing the clock frequency ✗
- By adding delay elements into logic paths. ✓
- By using FFs with larger hold time parameter values. ✗
- By decreasing the clock frequency. ✓

3 - Quiz

In the basic ROM structure, what does decoder input act as?

20 sec

- Data being written ✗
- Address ✓
- Enable Signal ✗
- Expander for scaling ROM capacity ✗

4 - Quiz

Given max delay D for a circuit, what is the maximum sampling frequency we can use?

20 sec

- 1/D ✗
- 1/(D+tcq+thold) ✗
- 1/(D+tcq+tsetup) ✓
- 1/(D+tcq-tsetup) ✗

5 - Quiz

Which of the following is the key advantage of Mealy machines over Moore?

20 sec

- Mealy machines have a simpler state transition diagram. ✗
- Mealy machines have a higher clock frequency. ✗
- Mealy machines typically include more states, with better error tolerance. ✗
- They can produce outputs dependent on both the current state and inputs. ✓

6 - Quiz

When designing a finite state machine, what is the purpose of state minimization?

20 sec

- To determine the input and output signals of the FSM. ✗
- To minimize the number of clock cycles required for operation. ✗
- To reduce the complexity and resource usage of the FSM implementation. ✓
- To map the states to their corresponding state transitions. ✗

7 - Quiz

Time necessary for data to be present and stable at the input of a sequential device ahead of the clock edge is ...

20 sec

- clock skew ✗
- hold time ✗
- setup time ✓
- clock jitter ✗

8 - Quiz

What is clock skew?

20 sec

- Random difference in clock arrival times at the same flip-flop ✗
- I made it up, It is not real and cannot hurt you. ✗
- Difference in arrival time btw. two clk edges at two different FF locations ✓
- Leakage current in the clock line causing accidental high signal in a FF ✗

9 - Quiz

What is not a property of Mealy machines?

20 sec

- the output is a function of current state & input ✗
- it is typically asynchronous ✗
- it takes longer to react to inputs than Moore machines do ✓
- it requires fewer states than Moore machines ✗

10 - Quiz

What is not a way to fix setup violations?

20 sec

- speed up the clock ✓
- improve circuit delay ✗
- decrease logic levels ✗
- choose faster gates ✗

11 - Quiz

What is not a term in the equation for setup time?

20 sec

- clock period ✗
- internal delay of FF ✗
- maximum logic delay ✗
- hold time ✓

12 - Quiz

Ripple counters are an example of a(n)

20 sec

- Arithmetic unit ✗
- Asynchronous counter ✓
- Synchronous sequential counter ✗
- Mealy FSM ✗

13 - Quiz

In terms of the relationship between DRAM and SRAM, which is true?

20 sec

- DRAM is faster than SRAM in terms of access time. ✗
- SRAM is more common in PCs, while DRAM is primarily used in IoT devices ✗
- They have the same level of complexity in terms of manufacturing and cost. ✗
- DRAM provides more storage density ✓

14 - Quiz

What are the pass transistors used in EPROM called?

20 sec

- Injection Gate MOS ✗
- Floating Gate MOS ✓
- FinFET ✗
- Double Gated MOS ✗

15 - Quiz

How can you remedy a hold time violation?

45 sec

- By increasing clock frequency ✗
- Using FFs with larger setup time parameters ✗
- Adding delay elements into paths of the combinational logic ✓
- By decreasing the clock frequency ✓

16 - Quiz

Verilog is objectively fun to use

20 sec

- Yes! ✓
- No! ✗
- only when coding FSMs ✗
- only when coding as a team ✗

17 - Quiz

Connecting a flip flop and latch to the same clock will synchronize when the two update

20 sec

- true ✗
- depends on input transition ✗
- false ✓
- depends on clock period width ✗

18 - Quiz

What is the primary similarity between a Parallel Prefix Adder (PPA) and the Carry Lookahead Adder (CLA)?

20 sec

- Both adders are based on the ripple carry concept ✗
- Both adders can perform addition in parallel ✗
- Both adders utilize a carry-propagate mechanism ✓
- Both adders require fewer logic gates compared to other adder achitectures ✗

19 - True or false

True or False: Moore Machine's outputs are a function of current state

20 sec

- True ✓
- False ✗

Resource credits