APPLICATION NOTE

AT03463: SAM4S Schematic Checklist

Atmel 32-bit Microcontroller

Introduction

A good hardware design comes from a proper schematic. Since the Atmel® | SMART™ SAM4S microcontrollers have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for a SAM4S design.

Features

- Power circuits
- ADC connection
- Clock and crystal oscillators
- JTAG and SWD debug ports
- USB connection
- Boot Program constraints
- Suggested reading

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1 Schematic Checklist

1.1 Single Power Supply Strategy

Figure 1-1. Single Power Supply Schematic Example

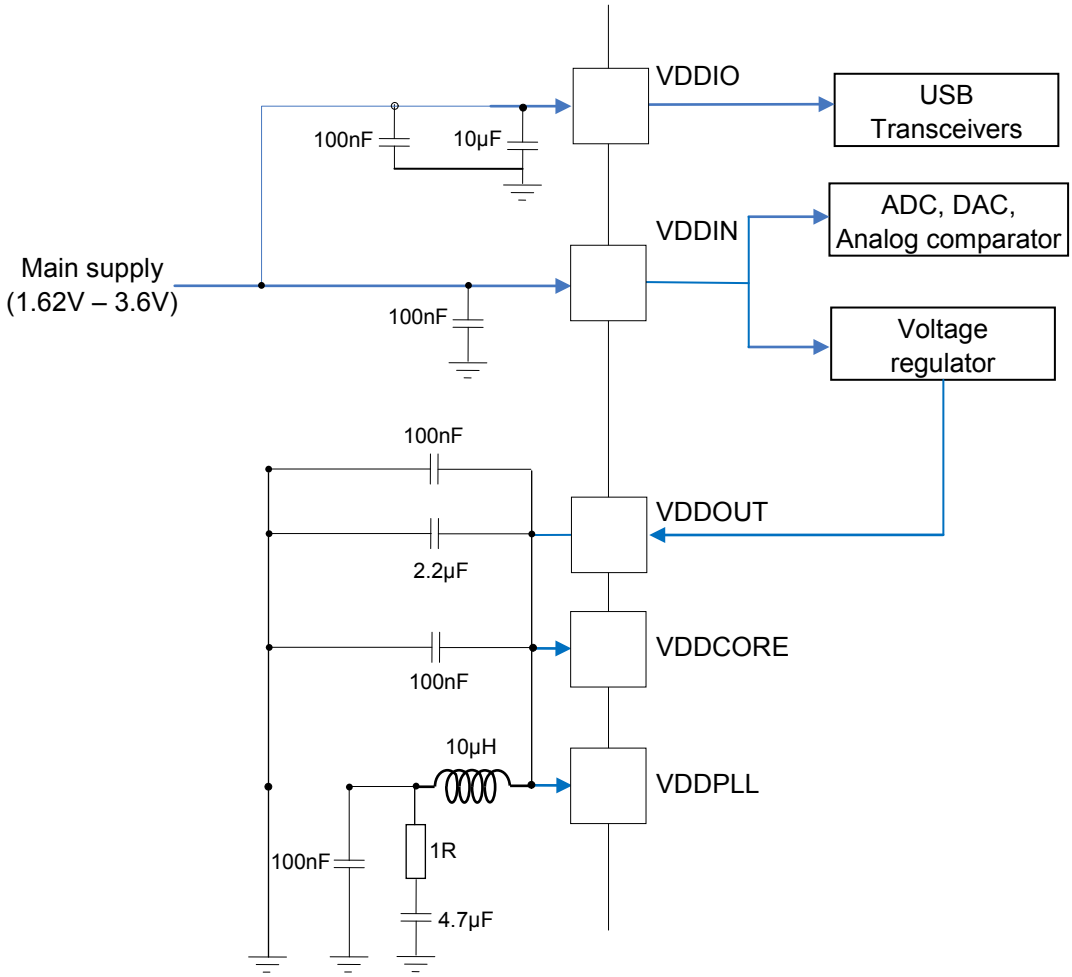


Table 1-1. Single Power Supply Checklist

☑	Signal name	Recommended pin connection	Description
	VDDIN	1.62V to 3.6V Decoupling/Filtering capacitors (100nF or higher ceramic capacitor) (Notes: 1)(Notes: 1.2)	Powers the voltage regulator, ADC, DAC, and Analog comparator power supply.
	VDDIO	1.62V to 3.6V Decoupling/Filtering capacitors (100nF and 10µF) (Notes: 1)(Notes: 1.2)	Powers the peripheral I/Os, USB transceiver, Backup part, 32kHz crystal oscillator and oscillator pads. De-coupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning:** At power-up VDDIO needs to reach 0.6V before VDDIN reaches 1.0V. **Warning:** VDDIO voltage needs to be equal or below to (VDDIN voltage +0.5V).

	VDDOUT	Decoupling/filtering capacitor (100nF and 2.2µF) (Notes: 1)(Notes: 1.2)	1.2V output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	1.08V to 1.32V Must be connected directly to VDDOUT pin. Decoupling capacitor (100nF) (Notes: 1)(Notes: 1.2)	Power the core, the embedded memories and the peripherals.
	VDDPLL	1.08V to 1.32V Decoupling/filtering RLC circuit (Notes: 1)(Notes: 1.2)	Powers PLLA, PLLB, the Fast RC and the 3 - 20MHz oscillator. Maximum voltage ripple is 10mV.
	GND	Ground	Ground pins GND are common to VDDIO, VDDPLL, and VDDCORE

Restrictions:

With Main Supply <2.0V, USB and ADC/DAC and Analog comparator are not usable.
With Main Supply ≥2.0V and <3V, USB is not usable.
With Main Supply ≥3V, all peripherals are usable.

Notes:
1. These values are given only as a typical example.
2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.

1.2 Dual Power Supply Strategy

Figure 1-2. Dual Power Supply Schematic Example

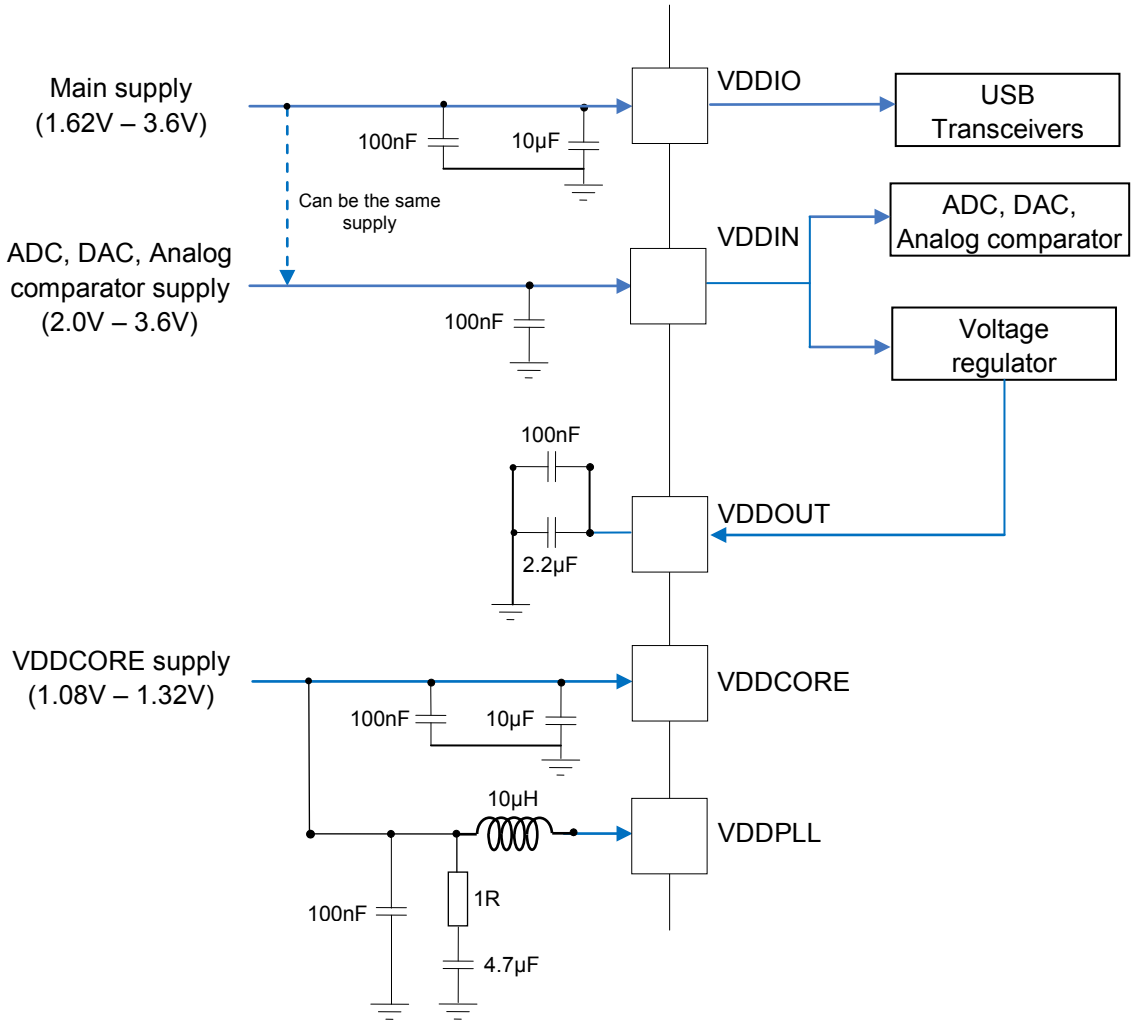


Table 1-2. Dual Power Supply Checklist

☑	Signal name	Recommended pin connection	Description
	VDDIN	2.0V to 3.6V Decoupling/Filtering capacitors (100nF or higher ceramic capacitor) (Notes: 1)(Notes: 1.2)	Powers the voltage regulator, ADC, DAC, and Analog comparator power supply.
	VDDIO	1.62V to 3.6V Connected to main supply Decoupling/Filtering capacitors (100nF and 10µF) (Notes: 1)(Notes: 1.2)	Powers the peripheral I/Os, USB transceiver, Backup part, 32kHz crystal oscillator and oscillator pads. De-coupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning:** At power-up VDDIO needs to reach 0.6V before VDDIN reaches 1.0V. **Warning:** VDDIO voltage needs to be equal or below to (VDDIN voltage +0.5V).

	VDDOUT	Decoupling/filtering capacitor (100nF and 2.2µF) (Notes: 1)(Notes: 1.2)	1.2V Output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	1.08V to 1.32V Connected to VDDCORE supply Decoupling capacitor (100nF) (Notes: 1)(Notes: 1.2)	Power the Core, the embedded memories and the peripherals.
	VDDPLL	1.08V to 1.32V Connected to VDDCORE supply Decoupling/filtering RLC circuit (Notes: 1)(Notes: 1.2)	Powers PLLA, PLLB, the Fast RC and the 3 - 20MHz oscillator. Maximum voltage ripple is 10mV.
	GND	Ground	Ground pins GND are common to VDDIO, VDDPLL, and VDDCORE

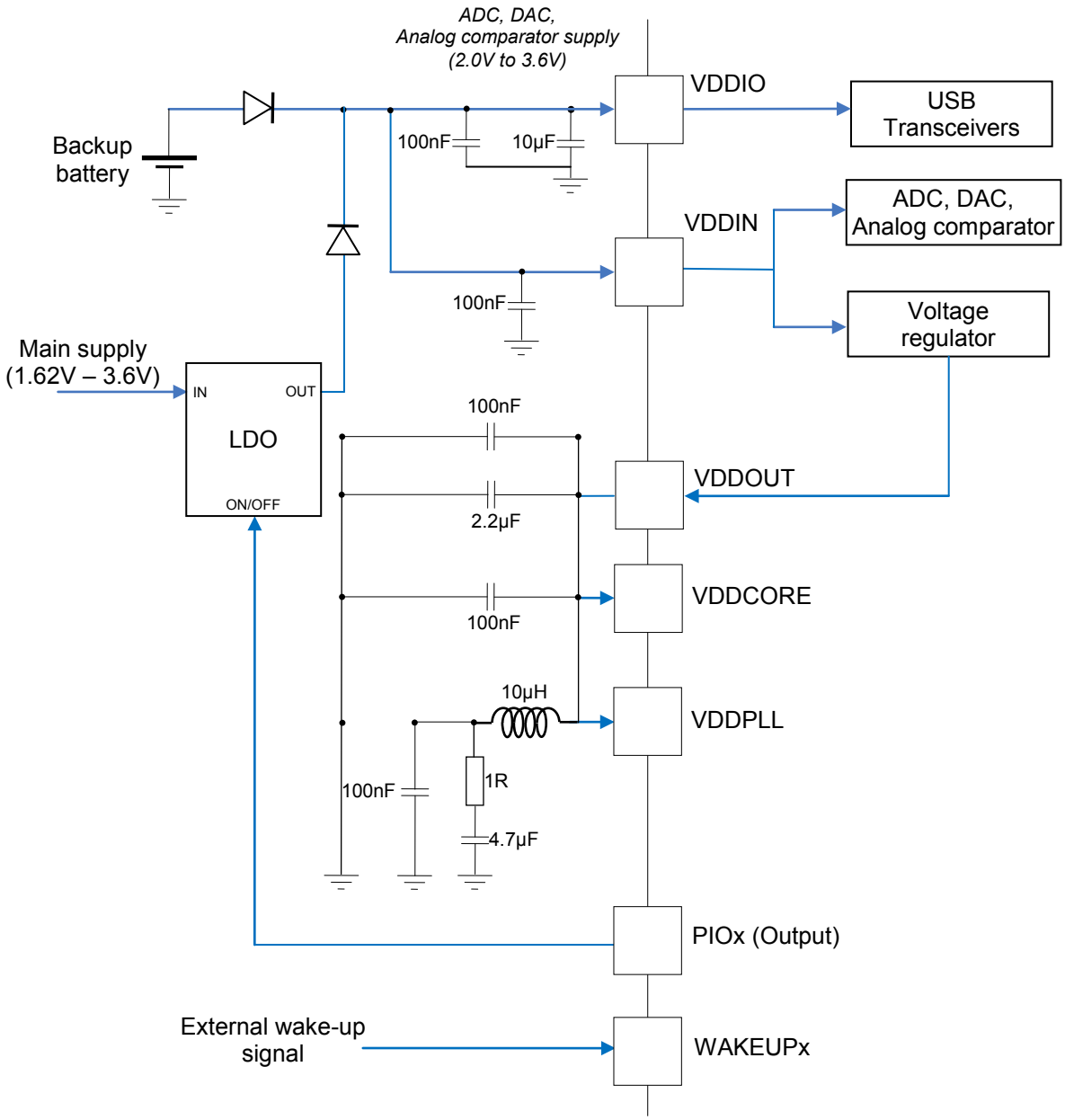
Restrictions:

For USB, VDDIO needs to be greater than 3.0V.
For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

Notes:
1. These values are given only as a typical example.
2. Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

1.3 Backup Unit Externally Supplied

Figure 1-3. Backup Unit Externally Supplied Schematic Example



The two diodes provide a “switchover circuit” (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

Table 1-3. Backup Unit Externally Supplied Checklist

☑	Signal name	Recommended pin connection	Description
	VDDIN	1.62V to 3.6V Decoupling/Filtering capacitors (100nF or higher ceramic capacitor) (Notes: 1)(Notes: 1.2)	Powers the voltage regulator

	VDDIO	1.62V to 3.6V Decoupling/Filtering capacitors (100nF and 10µF) (Notes: 1)(Notes: 1.2)	Powers the peripheral I/Os, USB transceiver, Backup part, 32kHz crystal oscillator, and oscillator pads. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning:** At power-up VDDIO needs to reach 0.6V before VDDIN reaches 1.0V. **Warning:** VDDIO voltage needs to be equal or below to (VDDIN voltage +0.5V).
	VDDOUT	Decoupling/filtering capacitor (100nF and 2.2µF) (Notes: 1)(Notes: 1.2)	1.2V output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	1.08V to 1.32V Connected to VDDOUT supply Decoupling capacitor (100nF) (Notes: 1)(Notes: 1.2)	Power the Core, the embedded memories and the peripherals.
	VDDPLL	1.08V to 1.32V Connected to VDDOUT supply Decoupling/filtering RLC circuit (Notes: 1)(Notes: 1.2)	Powers PLLA, PLLB, the Fast RC and the 3 - 20MHz oscillator. Maximum voltage ripple is 10mV.
	GND	Ground	Ground pins GND are common to VDDIO, VDDPLL, and VDDCORE

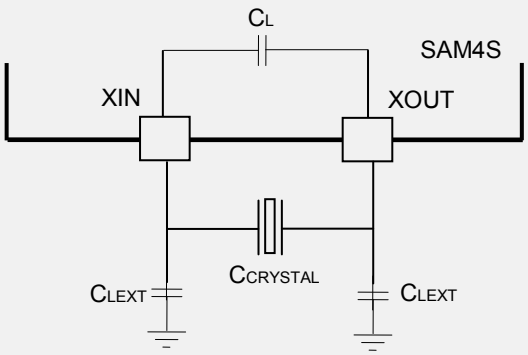
Restrictions:

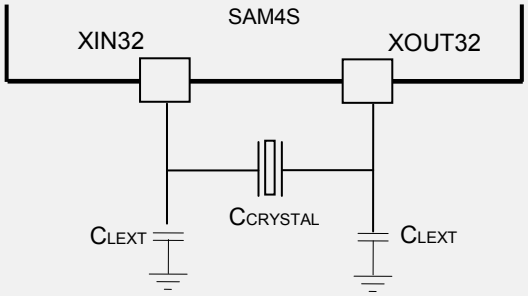
For USB, VDDIO needs to be greater than 3.0V.
For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

Notes:
1. These values are given only as a typical example.
2. Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

1.4 Clocks, Oscillator, and PLL

Table 1-4. Clocks, Oscillator, and PLL Checklist

☑	Signal name	Recommended pin connection	Description
	PB9/XIN PB8/XOUT Main Oscillator in Normal mode	Crystals between 3 and 20MHz Capacitors on XIN and XOUT (crystal load capacitance dependant) 1kΩ resistor on XOUT only required for crystals with frequencies lower than 8MHz.	Internal Equivalent Load Capacitance (C_L): C_L = 9.5pF Crystal Load Capacitance, ESR, Drive Level, and Shunt Capacitance to validate.  The external load capacitance is calculated with the following formula: $C_{LEXT}=2*(C_{crystal}-C_L)$ Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM4S Series Datasheet. **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4MHz.**
	PB9/XIN PB8/XOUT Main Oscillator in Bypass mode	PB9/XIN: external clock source PB8/XOUT: can be left unconnected or used as GPIO.	1.62V to 3.6V Square wave signal (V_{DDIO}) External Clock Source up to 50MHz Duty Cycle: 40 to 60%. **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4MHz.**
	4/8/12MHz Fast Internal RC oscillator	PB9/XIN and PB8/XOUT: can be left unconnected or used as GPIO	Powered up by V_{DDPLL} The output frequency is configurable through the PMC registers. The Fast RC oscillator is calibrated in production. The frequency can be trimmed by software. Duty Cycle: 40 to 60%. **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4MHz.**

	PA7/XIN32 PA8/XOUT32 32kHz Crystal used	32.768kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent).	Internal parasitic capacitance Cpara=0.7pF Crystal Load Capacitance, ESR, Drive Level, and Shunt Capacitance to validate.  CLEXTmax = 20pF CLEXT = 2 x (Ccrystal-Cpara- Cpcb) Refer to the Crystal Oscillators Design Consideration Information section of the SAM4S Series Datasheet. By default at start-up the chip runs out of the embedded 32kHz RC oscillator
	PA7/XIN32 PA8/XOUT32 32kHz Oscillator in bypass mode	PA7/XIN32: external clock source PA8/XOUT32: can be left unconnected or use as GPIO.	1.62V to 3.6V Square wave signal (VDDIO). External Clock Source up to 44kHz. Duty Cycle: 40 to 60%. By default at start-up the chip runs out of the embedded 32kHz RC oscillator

1.5 Serial Wire and JTAG

☑	Signal name	Recommended pin connection	Description
	TCK/SWCLK/PB7	Application dependant. If debug mode is not required this pin can be use as GPIO.	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TMS/SWDIO/PB6	Application dependant. If debug mode is not required this pin can be use as GPIO.	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TDI/PB4	Application dependant. If debug mode is not required this pin can be use as GPIO.	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TDO/TRACESWO/PB5	Application dependant. If debug mode is not required this pin can be use as GPIO.	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	JTAGSEL	Application dependant. Must be tied to V_{DDIO} to enter JTAG Boundary Scan. **In harsh environments, It is strongly recommended to tie this pin to GND.**	Permanent Internal pull-down resistor (15kΩ)

1.6 Flash Memory

☑	Signal name	Recommended pin connection	Description
	ERASE/PB12	Application dependant. If hardware erase is not required this pin can be use as GPIO	Internal pull-down resistor (100kΩ). Must be tied to V_{DDIO} to erase the General Purpose NVM bits (GPNVMx), the whole Flash content and the security bit. Reset state: Erase Input, with a 100kΩ Internal pull down and Schmitt trigger enabled

1.7 Reset and Test Pins

☑	Signal name	Recommended pin connection	Description
	NRST	Application dependant. If hardware erase is not required this pin can be use as GPIO	Internal pull-down resistor (100kΩ). Must be tied to V_{DDIO} to erase the General Purpose NVM bits (GPNVMx), the whole Flash content and the security bit. Reset state: Erase Input, with a 100kΩ Internal pull down and Schmitt trigger enabled. Minimum debouncing time is 220ms.
	TST	TST pin can be left unconnected in normal mode. To enter in FFPI mode TST pin must be tied to V_{DDIO}. **In harsh environments, it is strongly recommended to tie this pin to GND.**	Permanent internal pull-down resistor (15kΩ).

1.8 PIOs

☑	Signal name	Recommended pin connection	Description
	PAx - PBx-PCx	Application Dependant (Pulled-up on V_{DDIO})	At reset, all PIOs are in IO or System IO mode with Schmitt trigger inputs and internal pull-up enabled. To reduce power consumption, if not used, the concerned PIO can be configured as an output and driven at '0' with internal pull-up disabled.

1.9 Parallel Capture Mode

☑	Signal name	Recommended pin connection	Description
	PIODC0-PIODC7	Application Dependant (Pulled-up on V_{DDIO})	Parallel Mode capture Data

	PIODCCLK	Application Dependant (Pulled-up on V_{DDIO})	Parallel Mode capture Clock
	PIODCEN1-2	Application Dependant (Pulled-up on V_{DDIO})	Parallel Mode capture mode enable

1.10 Analog Reference

☑	Signal name	Recommended pin connection	Description
	ADVREF	2.0V to V_{DDIN}(*) Decoupling capacitor(s). *(*)2.0V is used for 10-bit ADC resolution only. In other case the minimum ADVREF value is 2.4V.*	ADVREF is a pure analog input. ADVREF is the voltage reference for the ADC, DAC and Analog comparator. To reduce power consumption, if analog features are not used, connect ADVREF to GND.

1.11 12-bit and 10-bit ADC [0]

☑	Signal name	Recommended pin connection	Description
	AD0-AD14	0 to ADVREF	ADC Channels
	ADTRG	V_{DDIO}	ADC External Trigger input

3. The ADC voltages in 10-bit mode resolution (ADC 12-bit in low resolution) can descend to 2.0V.

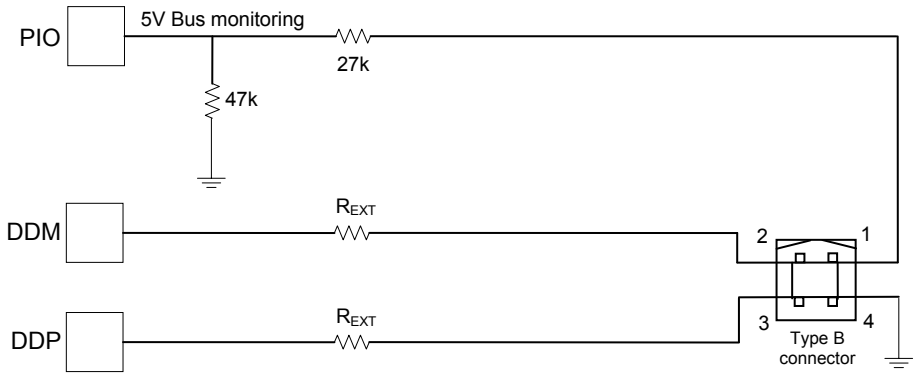
1.12 12-bit DAC

☑	Signal name	Recommended pin connection	Description
	DAC0-DAC1	1/6* ADVREF to 5/6* ADVREF	-
	DACTRG	V_{DDIO}	DAC External Trigger input

1.13 USB Device (UDP)

☑	Signal name	Recommended pin connection	Description
	DDP/PB11	Application dependent [0] If USB device support is not required this pin can be use as GPIO If UDP is not used, this pin can be left unconnected	Reset State: - USB Mode - Internal Pull-down
	DDM/PB10	Application dependent [0] If USB device support is not required this pin can be use as GPIO If UDP is not used, this pin can be left unconnected	Reset State: - USB Mode - Internal Pull-down

4. USB Device Typical connection:



1.14 Static Memory Controller (SMC)

☑	Signal name	Recommended pin connection	Description
	D0-D15	Application dependent	Data Bus (D0 to D15) *Note: Data bus lines are multiplexed with the PIOC controller. Their I/O line reset state is input with pull-up enabled.*
	A0-A23	Application dependent	Address Bus (A0 to A23) *Note: Data bus lines are multiplexed with the PIOA & PIOC controllers. Their I/O line reset state is input with pull-up enabled.*
	NWAIT	Application dependent	NWAIT pin is an active low input. *Note: NWAIT is multiplexed with PC13.*

2 SAM4S Boot Program Constraints

See AT91SAM Boot Program section of the SAM4S Series Datasheet for more details on the boot program.

2.1 SAM-BA Boot

The SAM-BA® Boot Assistant supports serial communication via the UART or USB device port:

- UART0 Hardware Requirements: none
- USB Device Hardware Requirements: external crystal or External clock(Note:Note:Note:Note:Notes: 1) with frequency of:

11.289MHz / 12.000MHz / 16.000MHz / 18.432MHz

Notes: 1. Must be 2500ppm and 1.62V to 3.6V (VDDIO) Square Wave Signal.

Table 2-1. Pins Driven During SAM-BA Boot Program Execution

Peripheral	Pin	PIO Line
UART0	URXD0	PA9
UART0	UTXD0	PA10

3 Suggested Reading

3.1 Device Datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. It also contains the electrical specifications and expected characteristics of the device.

The datasheet is available on http://www.atmel.com/products/microcontrollers/arm/sam4s.aspx in the Datasheets section of the product page.

3.2 Evaluation Kit User Guide

The SAM4S-EK user guide contains schematics that can be used as a starting point when designing with the SAM4S devices. This user guide is available on http://www.atmel.com/tools/SAM4S-EK.aspx in the documents section of the SAM4S-EK page.

3.3 USB Specification

The Universal Serial Bus specification is available from http://www.usb.org.

3.4 ARM Documentation on Cortex-M4 Core

- ARM® Cortex®-M4 Devices Generic User Guide for revision r0p1
- ARM Cortex-M4 Technical Reference Manual for revision r0p1

These documents are available at http://www.arm.com/ in the info center section.

4 Revision History

Doc Rev.	Date	Comments
42155D	12/2014	Figure 1-1, Figure 1-2, and Figure 1-3 are updated.
42155C	10/2013	Figure 1-1, Figure 1-2, and Figure 1-3 are updated.
42155B	08/2013	Updated recommended decoupling/filtering capacitor for VDDIN in: Table 1-1, Table 1-2, and Table 1-3.
42155A	07/2014	Initial document release.

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