

# Multifunctional complementary field-effect transistors based on MoS<sub>2</sub>/SWNTs heterostructures



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## ABSTRACT

The rapid evolution of devices based on low-dimensional materials such as MoS<sub>2</sub> and single-walled carbon nanotubes (SWNTs) has garnered significant interest for high-performance field-effect transistor (FET) applications. We present a multifunctional MoS<sub>2</sub>/SWNT device exhibiting non-monotonic current modulation with a rectifying ratio of up to 600. The device also demonstrates remarkable optoelectronic memory performance, including fast erasing/writing times (20.1/1.9 ms), a high erasing/writing ratio ( $10^4$ ), multilevel data storage, robust retention (10 000 s), and excellent endurance (1000 cycles). Additionally, we demonstrate ternary inverters combining SWNTs FETs with MoS<sub>2</sub>/SWNTs heterostructure FETs, highlighting their potential in advanced logic applications.

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Ultrathin low-dimensional materials such as graphene,<sup>1</sup> carbon nanotubes (CNTs),<sup>2,3</sup> transition-metal dichalcogenides (TMDCs),<sup>4</sup> and black phosphorus,<sup>5</sup> along with their heterostructures,<sup>6,7</sup> exhibit promising properties like excellent interface matching and resistance to short-channel effects.<sup>8,9</sup> These qualities make them ideal candidates for advanced electronic and optoelectronic applications. Over recent years, various van der Waals heterostructure devices, including tunneling field-effect transistors,<sup>10</sup> programmable rectifiers,<sup>11</sup> floating-gate memory devices,<sup>12</sup> optoelectronics,<sup>13</sup> and complementary field-effect transistors (CMOS),<sup>14</sup> have been demonstrated. In these functional devices, information is stored or computed as either “0” or “1” based on binary systems. The development of multivalue logic devices operating with ternary logic can significantly reduce the number of devices and the overall complexity of the system.

In heterostructures, rectifying properties are influenced by Fermi level modulation and the conduction band-valence band offset, which determines where electrons and holes can accumulate or deplete. High rectifying and on-off ratios are challenging to be achieved with 2D materials.<sup>15</sup> In addition, a transition from traditional binary inverters

to ternary inverters could be realized by regulating Fermi level modulation and the conduction band-valence band offset. Currently, van der Waals heterostructure featured with negative differential transconductance<sup>14</sup> and three distinct flat conductance states<sup>16</sup> in the transfer characteristics have been utilized in the design of ternary inverters.

MoS<sub>2</sub>, an n-type semiconductor with a large bandgap and good electron mobility,<sup>9,17</sup> paired well with SWNTs (single-walled carbon nanotubes), offers a promising combination.<sup>18</sup> The resulting MoS<sub>2</sub>/SWNTs heterostructure enables high rectifying behavior and strong on-off ratios.<sup>19</sup> Additionally, the optoelectronic properties of MoS<sub>2</sub><sup>7</sup> and charge-trapping states in SWNTs<sup>20</sup> facilitate photoinduced memory, enhancing the multifunctionality of the device. The wafer-level preparation technology of MoS<sub>2</sub> and SWNT network has become mature,<sup>2,21</sup> which is very conducive to industrial integration. Although many studies on MoS<sub>2</sub>/SWNTs heterostructures have been reported, few studies on CMOS based on MoS<sub>2</sub>/SWNTs have been discovered, especially how to design and prepare more advanced functional devices based on the characteristics of MoS<sub>2</sub>/SWNTs, such as the fabrication of multivalue logic devices.

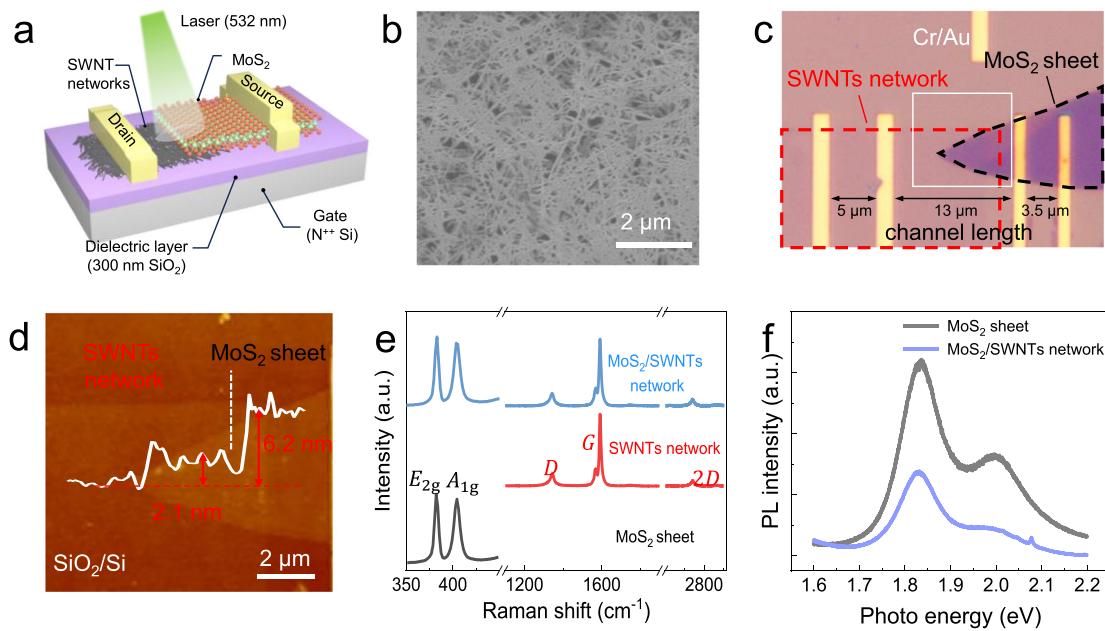
Here, we fabricated MoS<sub>2</sub>/SWNTs network heterostructure using a dry transfer method. The device shows non-monotonic current modulation, a high rectifying ratio ( $\sim 600$ ), and excellent optoelectronic performance. Furthermore, ternary inverters based on this heterostructure showcase the benefits of switching from binary to ternary logic, reducing device complexity and enhancing performance.

Figure 1(a) presents the schematic illustration of the MoS<sub>2</sub>/SWNTs network heterostructure device. The uniform SWNTs network was deposited onto a 300 nm SiO<sub>2</sub>/Si substrate using a solution process (Fig. S1). The morphology and density of the SWNTs network are shown in the SEM image [Fig. 1(b)], with a bandgap of 0.99 eV measured by UV-visible absorption spectrum shown in Fig. S2. An isolated SWNTs network stripe was isolated using reactive ion etching, facilitating the construction of the MoS<sub>2</sub>/SWNT heterostructure, and effectively suppressing leakage current. The MoS<sub>2</sub> sheet, selected as the light absorption layer due to its visible-range bandgap (1.2 eV),<sup>22,23</sup> was transferred onto the SWNTs stripe using a dry transfer method.<sup>24</sup> To ensure a high-quality interface, the MoS<sub>2</sub> sheet was transferred at a speed of  $\sim 0.2 \mu\text{m/s}$  using a precision displacement stage, expelling molecules from the interface.<sup>25</sup> Electrodes were patterned using standard electron beam lithography followed by thermal evaporation. The schematic diagram of the device fabrication process can be seen in Fig. S3 in the supplementary material.

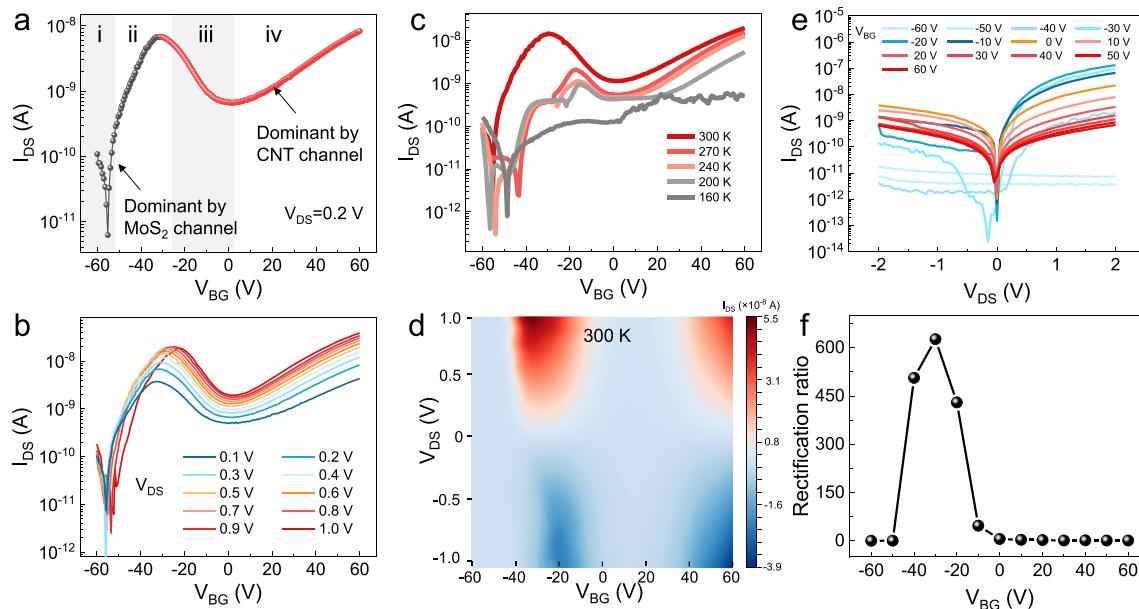
Figure 1(c) shows an optical image of the device, with the MoS<sub>2</sub> sheet and SWNTs network stripe delineated by black and red dashed lines, respectively. AFM image in Fig. 1(d) reveals a clean interface between the MoS<sub>2</sub> sheet and SWNTs network, with thicknesses of 4.1 and 2.1 nm, respectively [inset in Fig. 1(d)]. Raman spectra [Fig. 1(e)] confirmed the fabrication of the MoS<sub>2</sub>/SWNTs heterostructure, with

characteristic peaks for MoS<sub>2</sub> (382 and 404 cm<sup>-1</sup> corresponding to peaks of the MoS<sub>2</sub> sheet) and SWNTs (1344, 1591, and 2682 cm<sup>-1</sup> corresponding to D, G, and 2D mode of the SWNTs network). Additionally, photoluminescence (PL) spectra [Fig. 1(f)] indicate that the PL intensity of the MoS<sub>2</sub>/SWNTs network is about 2.36 times lower than that of the MoS<sub>2</sub> sheet. The PL intensity is typically a direct indicator of the recombination of photoexcited electron-hole pairs. The reduction of PL intensity in MoS<sub>2</sub>/SWNTs can be attributed to the presence of trapping states (structural defects during growth<sup>26</sup> and absorbed residual surfactants) in SWNTs network, which hinder the recombination of photoexcited electron-hole pairs.

The individual electrical properties of the MoS<sub>2</sub> and SWNTs FETs (field-effect transistors) were first characterized. The SWNTs FET exhibited bipolar behavior, with a switching ratio reaching 10<sup>3</sup>, while the MoS<sub>2</sub> FET showed n-type characteristics with a switching ratio of 10<sup>6</sup>, as shown in Fig. S4. For the MoS<sub>2</sub>/SWNTs device, the transfer characteristics are presented in Fig. 2(a). The band diagram shown in Fig. S5 indicates that the Fermi level of MoS<sub>2</sub> is higher than that of the SWNTs before contact. After contact, electrons can spontaneously transfer from MoS<sub>2</sub> into the SWNTs until the Fermi level alignment. The MoS<sub>2</sub>/SWNTs device displays non-monotonic current modulation, with electric current transport occurring in four distinct regions (i-iv) based on gate voltage ( $V_{BG}$ ). Region i ( $V_{BG} < -50 \text{ V}$ ) corresponds to full depletion of the MoS<sub>2</sub> channel, while in region ii ( $-50 \text{ V} < V_{BG} < -30 \text{ V}$ ), both the MoS<sub>2</sub> channel and the heterostructure start to turn on. In region iii ( $-30 \text{ V} < V_{BG} < 0 \text{ V}$ ), the heterostructure is fully activated, and current is dominated by the non-overlapped SWNTs network and the MoS<sub>2</sub> transistor (the current in the depleted SWNTs channel decreases more quickly than the increase



**FIG. 1.** Basic characterization of MoS<sub>2</sub>/SWNTs heterostructure. (a) Schematic of the device based on MoS<sub>2</sub>/SWNTs heterostructure on a 300 nm SiO<sub>2</sub>/Si substrate. (b) SEM image of the SWNTs network. (c) Optical image of MoS<sub>2</sub>/SWNTs heterostructure device. (d) AFM image of the MoS<sub>2</sub>/SWNTs heterostructure in the white frame of (c). The inset gives the height profiles along the white dashed line. (e) Raman spectra of MoS<sub>2</sub> sheet, SWNTs network, and MoS<sub>2</sub>/SWNTs heterostructure. (f) The PL spectra of MoS<sub>2</sub> sheet and MoS<sub>2</sub>/SWNTs heterostructure.



**FIG. 2.** Rectification behavior and nonlinear modulation characteristics in MoS<sub>2</sub>/SWNTs heterostructure. (a) Transfer characteristics in four regions of typical MoS<sub>2</sub>/SWNTs network devices. (b) Transfer curves of the device under different biases in the dark. (c) The transfer characteristics of the MoS<sub>2</sub>/SWNTs heterostructure device under different temperatures. (d) The mapping of  $I_{DS}$  under different  $V_{BG}$  and  $V_{DS}$  at 300 K. (e) The output characteristic of the device under different gate voltages. (f) Rectification ratio under different gate voltages.

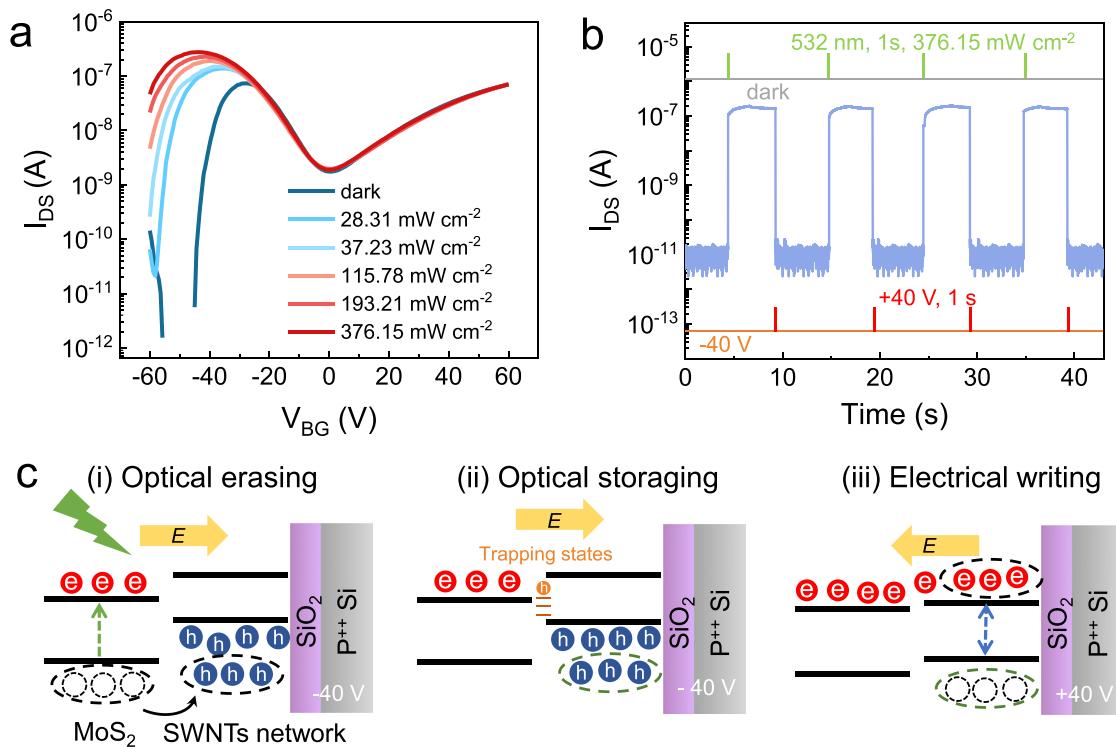
in the MoS<sub>2</sub> channel). In region iv ( $V_{BG} > 0$  V), ambipolar behavior in SWNTs FET emerges, with current increasing in entire channels. The channel current in regions ii and iv increases with the biases ranging from 0.1 to 1.0 V. Figure 2(b) shows the transfer curves of the device under different biases. The device has an on-off ratio of up to  $1.3 \times 10^3$  (current at  $V_{BG} = 60$  V vs current at  $V_{BG} = -55$  V) at  $V_{DS} = 0.2$  V. Temperature-dependent measurements for MoS<sub>2</sub>/SWNTs heterostructure [Figs. 2(c), 2(d), and S6] indicate that the channel current decreases as temperature decreases. In MoS<sub>2</sub> devices, carrier mobility typically increases as temperature decreases, primarily due to reduced phonon scattering.<sup>27</sup> In contrast, in the case of a one-dimensional carbon nanotube, Luttinger liquid states are typically anticipated, and its resistance increases with the decreasing temperature,<sup>28</sup> which is a key factor leading to the increase in resistance for MoS<sub>2</sub>/SWNTs. In addition, with reduced thermal excitation at low temperatures, carriers trapped in SWNTs face greater difficulty in overcoming the barriers associated with defects or interface states.

For output characteristics, as  $V_{BG}$  increases to  $-30$  V, holes accumulate greatly in the SWNTs network, while the MoS<sub>2</sub> FET behaves as a depletion-type transistor due to the Fermi pinning effect<sup>29</sup> (primarily caused by the metal contacts and interfacial states). Therefore, a p-n junction is formed, yielding diode-like behavior with a high rectification ratio (up to 600), as shown in Figs. 2(e) and 2(f). Under positive  $V_{BG}$ , the device is doped as an n-n junction because of the ambipolar nature of SWNTs network, exhibiting Ohmic-like behavior with rectification ratio close to 1.

Figure 3(a) presents the transfer characteristics of the MoS<sub>2</sub>/SWNTs heterostructure under laser illumination (MaxPhotonics; wavelength: 532 nm; spot diameter: 3 mm) with various power densities. The device achieves a high photocurrent-to-dark current ratio

( $I_{ph}/I_{dark}$ ) of up to  $10^4$  at  $V_{BG} = -50$  V, demonstrating strong optoelectronic performance. The excellent photoresponse of heterostructure is mainly attributed to the excellent photoresponse characteristics of MoS<sub>2</sub> [Figs. S7(a) and S7(b)]. The reason for the weak photoelectric response of SWNTs [Figs. S7(c) and S7(d)] is that the electron-hole pairs (excitons) under excitation are not easily separated, and the free carriers are relatively few due to the one-dimensional limited property. On the other hand, the presence of defects and interface states result in rapid recombination of photogenerated carriers.<sup>30</sup> In addition, based on the  $I_{DS}$ - $V_{DS}$  characteristics, Schottky barrier between metal (Cr/Au) and semiconductor (MoS<sub>2</sub> and SWNTs) can be extracted, which influences the process of dissociation of photogenerated electron-hole pairs in the device. As the gate voltage varies, the range of Schottky barrier height changes between the SWNTs and Cr/Au shifts to a smaller value compared to that with MoS<sub>2</sub> (Fig. S8), which is consistent with the weaker photocurrent response of the SWNTs (seeing more detailed discussion about Schottky barrier in the Supporting Information). The erasing, storage, and writing processes of the photoinduced memory device using laser pulses and gate voltage pulses are shown in Fig. 3(b). The green line represents the laser pulse, which is  $376.15 \text{ mW cm}^{-2}$  with a duration of 1 s, which corresponds to the erasing process. The red line is a gate voltage pulse (40 V, duration = 1 s), which corresponds to the writing process. The gray shade indicates a dark environment.

The underlying mechanism is detailed in Fig. 3(c). Upon laser excitation, MoS<sub>2</sub> absorbs photonic energy, generating electron-hole pairs due to its strong optical absorption and light-matter interactions.<sup>31</sup> Photogenerated holes migrate to the SWNTs network under a negative electric field, while electrons accumulate in the MoS<sub>2</sub> sheet.<sup>22</sup> The structural defects of SWNTs during growth and the inevitable



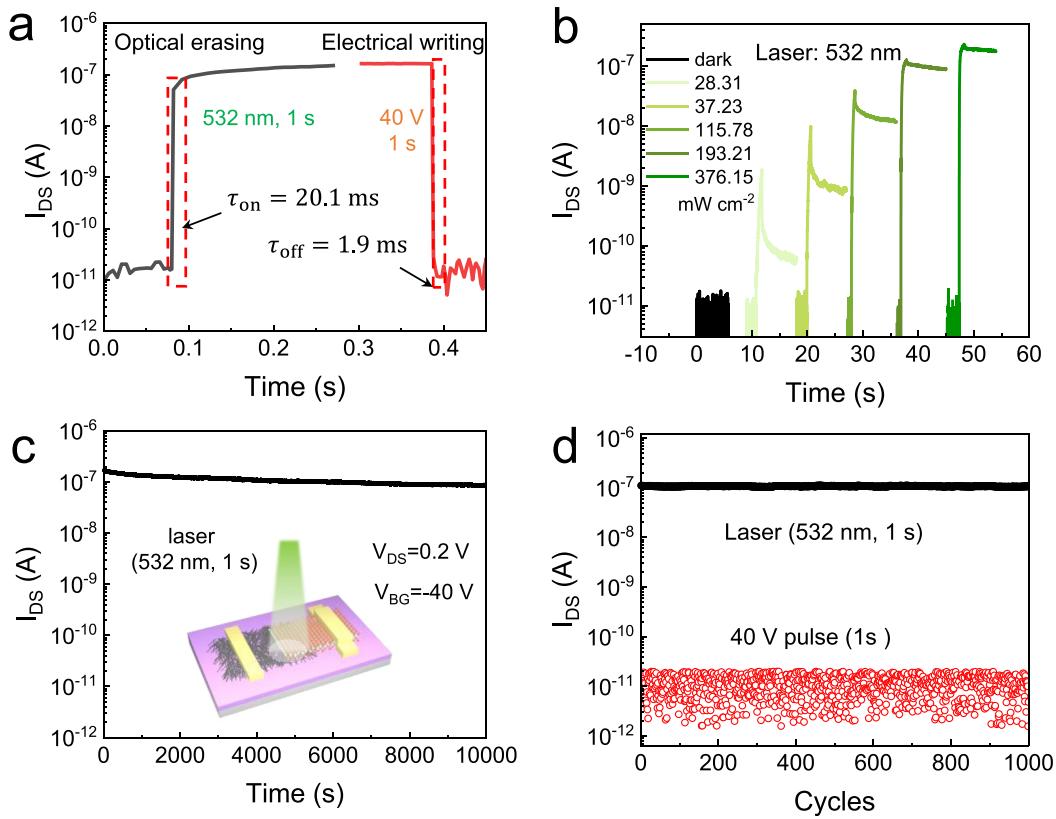
**FIG. 3.** Mechanism of the optoelectronic nonvolatile memory. (a) The transfer characteristics of the device at different light powers under 532 nm illumination, duration = 1 s,  $V_{DS} = 0.2$  V. (b) The erasing, storage, and writing processes of the photoinduced memory device. (c) The schematic illustration of the mechanism of the photoinduced memory device.

adsorbed surfactants in the solution during the deposition of SWNTs networks can both generate localized states in the electronic structure that serve as trapping sites for charge carriers. Photogenerated holes are still captured in SWNTs network by these trapping states after the light disappears. Meanwhile, the photogenerated holes in the SWNTs network can screen and weaken the negative gate voltage in the MoS<sub>2</sub> sheet.<sup>32</sup> This process leads to a p-n junction formation, which persists even after the laser is turned off, due to charge trapping in the SWNTs network.<sup>33</sup> Under a positive  $V_{BG}$ , both MoS<sub>2</sub> and SWNTs become n-type conductive. The previously trapped holes in SWNTs can be released through the recombination with the excess electron, and the gate screening effect disappears. Consequently, the MoS<sub>2</sub> channel recovers to the low current state under a negative gate voltage.

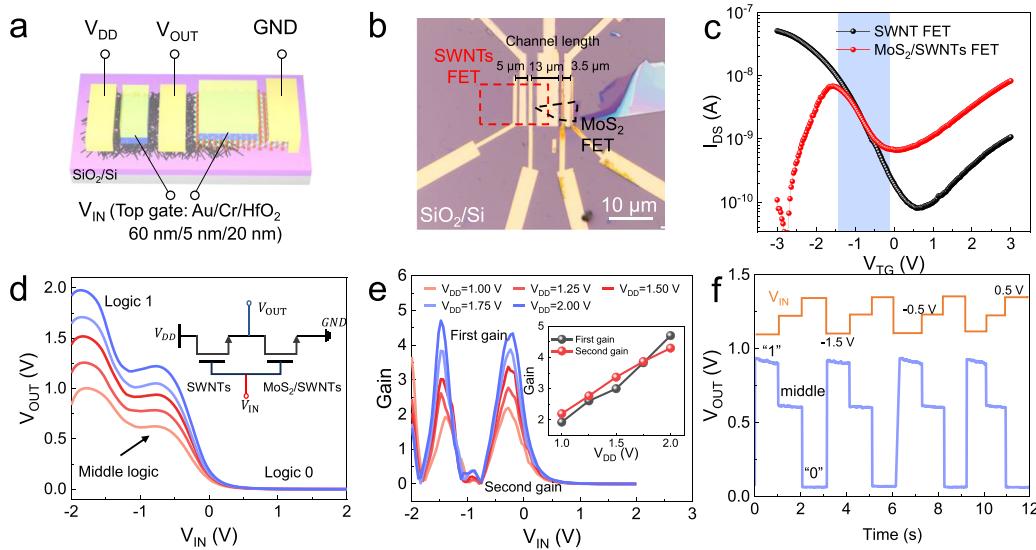
We then analyzed the speed of the optical erasing and electrical writing operation of the photoinduced memory. Although both erasing and writing operations were accomplished using a 1 s pulse, the response time for optical erasing and electrical operation is determined to be 20.1 and 2.3 ms, respectively, as shown in Fig. 4(a). This high speed of erasing/writing operation results from the strong interlayer electronic coupling<sup>34</sup> and the presence of a valence band offset<sup>35</sup> (high carrier redistribution efficiency). In addition, the bipolar nature of the SWNTs network allows significant tuning of the Fermi level by an external gate voltage, achieving a nearly transparent band alignment with the MoS<sub>2</sub> sheet.<sup>36</sup> Figures 4(b) and S9 show the optical erasing operation at different light pulse power levels for 1 s under 532 nm illumination at  $V_{DS} = 0.2$  V, demonstrating multilevel storage capacity

and excellent stability of optoelectrical nonvolatile memory. It is worth noting that the optical storage performance basically disappears when the laser power density is reduced to 2.82 mW/cm<sup>2</sup>. In addition, reliable retention characteristics and writing/erasing endurance are crucial for data storage reliability of optoelectrical nonvolatile memory. When a 532 nm laser pulse is applied to this device for 1 s, the erasing state current retains a value of  $10^{-7}$  A, without any attenuation after 10 000 s [Fig. 4(c)], indicating long retention characteristics. The endurance test also presents stable performance after 1000 cycles of repeated optical erasing/electrical writing processes [Fig. 4(d)].

Binary and ternary inverters based on MoS<sub>2</sub>, SWNTs, and MoS<sub>2</sub>/SWNTs heterostructures are demonstrated. To achieve the matching of  $V_{IN}$  and  $V_{OUT}$ , a top gate structure with high-dielectric permittivity HfO<sub>2</sub> was designed and fabricated (Fig. S10). The thickness of HfO<sub>2</sub> and Au/Cr is approximately 20 and 5/60 nm, respectively. For binary inverters, SWNTs FETs and MoS<sub>2</sub> FETs were combined to produce typical CMOS inverter behavior, with rail-to-rail voltage transfer curves and a high voltage gain (11.5 at  $V_{DD} = 2$  V), as shown in Fig. S11. Ternary inverters were constructed by combining MoS<sub>2</sub>/SWNTs FETs and SWNTs FETs [Figs. 5(a) and 5(b)]. The individual transfer characteristic curves of MoS<sub>2</sub>/SWNTs and SWNTs at a bias voltage of 1 V are shown in Fig. 5(c). The unique overlap of transfer characteristics between the SWNT and MoS<sub>2</sub>/SWNT channels is observed, which introduces a middle logic state in addition to conventional logic 1 and 0, as shown in Fig. 5(d). Figure 5(e) and the inset show voltage gain for both switching state at different  $V_{DD}$  for the ternary inverter. The first gain and second



**FIG. 4.** Optical storage properties of MoS<sub>2</sub>/SWNTs. (a) The speed of erasing process and writing process. (b) Optical erasing process at different light powers under 532 nm illumination with 1 s duration. Retention characteristic (c) and endurance performance (d) of the photoinduced memory.



**FIG. 5.** Ternary inverter based on SWNTs FET and MoS<sub>2</sub>/SWNTs FET. (a) Structure diagram of ternary inverter based on SWNTs and MoS<sub>2</sub>/SWNTs. (b) Optical image of ternary inverter with top gate. (c) The transfer characteristics of the SWNTs FET and MoS<sub>2</sub>/SWNTs FET with the top gate structure. (d)  $V_{OUT}$ - $V_{IN}$  of ternary inverter. (e) Voltage gain for the switching state at different  $V_{DD}$ . (f) The ternary logic output waveform of the ternary inverter.

gain are above 4 at  $V_{DD} = 2$  V. The dynamic performance of the ternary inverter is depicted in Fig. 5(f), where three-level input voltages (1.5, 0.5, and 0.5 V) trigger clear transitions between logic states.

In summary, we have fabricated a multifunctional MoS<sub>2</sub>/SWNTs heterostructure that demonstrates non-monotonic current modulation and excellent rectifying behavior. The device also exhibits high-speed optoelectronic memory performance, with robust retention and endurance. Furthermore, binary and ternary inverters based on SWNTs, MoS<sub>2</sub>, and MoS<sub>2</sub>/SWNTs are designed and constructed, highlighting the potential of this heterostructure for logic applications. The integration of ternary logic systems promises to reduce the complexity of traditional device architectures, paving the way for more efficient computing solutions.

See the [supplementary material](#) and additional experimental data (PDF) for materials and methods.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

**Wenxiang Wang:** Conceptualization (lead). **Zheng Wei:** Data curation (equal); Formal analysis (equal). **Yong Jun Li:** Writing – review & editing (supporting). **Jiawang You:** Writing – review & editing (supporting). **Xiaohuan Li:** Formal analysis (supporting); Investigation (supporting). **Jinjin He:** Methodology (supporting). **Han Mao:** Writing – original draft (supporting). **Jiyou Jin:** Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Lianfeng Sun:** Methodology (equal); Project administration (equal); Validation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Zhaohui Dai:** Conceptualization (equal); Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Writing – original draft (equal); Writing – review & editing (equal).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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