## 1 Appendix - Opcodes

In this Appendix we list the opcodes for decoded instructions on each of the distinct ISAs we have explored. We group Compute Capability 3.0 with 2.x, rather than the rest of the 3.x generation. The first column in each table is the opcode's string and the operand types. We use 'reg' for general register operands, 'p' for predicate registers, 'lit' for literal (hexadecimal or decimal) values, 'mem' for memory, 'const' for constant memory, 'tex' for texture shapes, 'channel' for texture channels, 'bitfield' for bitfield operands, and 'misc' for operands without a clear type.

The second column is the binary, with zeros and ones for opcode bits, and the character 'x' in place of bits that are not controlled by the opcode, with the least significant bit on the left. Bits which affect the types of the operands are treated as opcode bits.

## 1.1 Opcodes on Compute Capabilities 2.x and 3.0

TODO (We didn't decode this one automatically, we mostly got it from asfermi's wiki, so formatting it like the tables below is going to be time-consuming.)

## 1.2 Opcodes on Compute Capability 3.x

Table 1. Opcode lookup table: opcodeTable3x

Instruction	Bits
MOV reg reg lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100100
MOV reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111xxxx
MOV reg const lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100100
MOV reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111xxxx
MOV32I reg lit lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
MOV32I reg lit	01xxxxxxxxxx1111xxxxxxxxxxxxxxxxxxxxxxx
LD reg mem	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
LDL reg mem	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
LDS reg mem	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
LDC reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
ST mem reg	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
STL mem reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
STS mem reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101011110
FADD reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101010011
FADD reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101000110
FADD reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101000111
FADD32I reg reg lit	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FMUL reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FMUL reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FMUL reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FMUL32I reg reg lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FFMA reg reg const reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FFMA reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FFMA reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FFMA reg reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FSETP p p reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FSETP p p reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FSETP p p reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
DSETP p p reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
DSETP p p reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
DSETP p p reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FCMP reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FCMP reg reg const reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
MUFU reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
DADD reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

DADD reg reg lit DADD reg reg reg DMUL reg reg reg DMUL reg reg lit DMUL reg reg const DFMA reg reg lit reg DFMA reg reg reg const DFMA reg reg const reg DFMA reg reg reg IADD reg reg const IADD reg reg reg IADD reg reg lit IADD32I reg reg lit IMNMX reg reg lit p IMNMX reg reg p IMNMX reg reg const p IMUL reg reg const IMUL reg reg lit IMUL reg reg reg IMUL32I reg reg lit IMAD reg reg lit reg IMAD reg reg const reg IMAD reg reg reg IMAD reg reg reg const ISCADD reg reg lit lit ISCADD reg reg lit ISCADD reg reg const lit ISET reg reg const p ISETP p p reg lit p ISETP p p reg reg p ISETP p p reg const p ICMP reg reg lit reg ICMP reg reg reg ICMP reg reg const reg I2F reg const I2F reg reg I2I reg const I2I reg reg I2I reg lit F2I reg reg F2I reg const F2F reg reg F2F reg const LOP reg reg const LOP reg reg lit LOP reg reg reg LOP32I reg reg lit SHL reg reg const SHR reg reg lit SHR reg reg const BFE reg reg lit BFE reg reg const BFI reg reg lit reg SEL reg reg p 

111	CEI	100010100011
111	SEL reg reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
112	SEL reg reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
113	SSY const SSY lit	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
114		00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
115	BRA const	00111101xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
116	BRA misc const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
117	BRA lit	00111100xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
118	BRA misc lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
119	BRX misc reg lit	00xxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
120	BRX reg lit	00111100xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
121	BRX const	00111101xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
122	BRX misc const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010010
123	PCNT const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxx110101000
124	PCNT lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
125	CONT misc	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
126	CONT	0011110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
127	PBK lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
128	PBK const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxx010101000
129	BRK misc	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
130	BRK	0011110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
131	CAL const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
132	CAL lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
133	RET misc	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
134	RET	0011110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
135	EXIT misc	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
136	EXIT	0011110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
137	NOP misc lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
138	NOP lit	01xxxxxxx11110xxxxxxxxxxxxxxxxxxxxxxxx
139	BPT lit	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
140	S2R reg sreg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
141	PSETP p p p p p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
142	PSET reg p p p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
143	FLO reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
144	FLO reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
145	P2R reg misc reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
146	P2R reg misc reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
147	R2P misc reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
148	R2P misc reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
149	TEX reg reg lit tex lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
150	TEX reg reg lit tex lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
151	TEXDEPBAR lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
152	RRO reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
153	RRO reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
154	PRMT reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
155	DMNMX reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
156	DMNMX reg reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
157	FMNMX reg reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
158	FMNMX reg reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
159	FMNMX reg reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
160	VOTE p p	011111111111111111111111111111111111111
161	VOTE reg p p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
162	POPC reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
163	POPC reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
164	MEMBAR	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
165		3

CSETP p p misc p ISCADD32I reg reg lit lit TLD reg reg lit tex lit TLD reg reg lit tex lit SHF reg reg reg reg SHF reg reg lit reg FCHK p reg reg FCHK p reg const ISUB reg const reg ISUB reg reg const ISUB reg reg reg ISUB reg lit reg ISUB reg reg lit LDG reg mem 

## 1.3 Opcodes on Compute Capabilities 5.x and 6.x

Table 2. Opcode lookup table: opcodeTable5x6x

Instruction	Bits
MOV reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111
MOV reg const lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
MOV reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111
MOV reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
MOV32I reg lit	xxxxxxxxxxx1111xxxxxxxxxxxxxxxxxxxxxxx
MOV32I reg lit lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
LD reg mem p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
LDL reg mem	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
LDS reg mem	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
LDC reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
ST mem reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
STL mem reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
STS mem reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FADD reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FADD reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FADD reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FADD32I reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FMUL reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FMUL reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FMUL reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FMUL32I reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FFMA reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FFMA reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FFMA reg reg const reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FFMA reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FSET reg reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FSET reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FSETP p p reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FSETP p p reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FSETP p p reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
DSETP p p reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
DSETP p p reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
DSETP p p reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
FCMP reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

FCMP reg reg const reg FCMP reg reg lit reg MUFU reg reg DADD reg reg reg DADD reg reg lit DADD reg reg const DMUL reg reg reg DMUL reg reg lit DMUL reg reg const DFMA reg reg reg DFMA reg reg lit reg DFMA reg reg const reg DFMA reg reg reg const IADD reg reg reg IADD reg reg const IADD reg reg lit IADD32I reg reg lit IMNMX reg reg const p IMNMX reg reg p IMNMX reg reg lit p ISCADD reg reg lit ISCADD reg reg lit lit ISCADD reg reg const lit ISET reg reg reg p ISET reg reg const p ISET reg reg lit p ISETP p p reg reg p ISETP p p reg lit p ISETP p p reg const p ICMP reg reg reg ICMP reg reg lit reg ICMP reg reg const reg I2F reg reg I2F reg const I2I reg lit I2I reg reg I2I reg const F2I reg reg F2F reg reg F2F reg const F2F reg lit LOP reg reg lit LOP p reg reg reg LOP reg reg reg LOP p reg reg const LOP reg reg const LOP p reg reg lit LOP32I reg reg lit SHL reg reg lit SHL reg reg reg SHR reg reg lit SHR reg reg reg BFE reg reg lit BFI reg reg lit reg

SEL reg reg reg p SEL reg reg lit p SEL reg reg const p SSY lit SSY const BRA const BRA misc const BRA lit BRA misc lit BRX const BRX misc const BRX reg lit BRX misc reg lit PCNT lit PCNT const CONT CONT misc PBK lit PBK const BRK BRK misc CAL lit CAL const RET **RET** misc **EXIT** EXIT misc NOP lit NOP misc lit NOP NOP misc BAR lit BAR lit lit S2R reg sreg PSETP ppppp PSET reg p p p FLO reg reg TEX reg reg lit tex lit TEX reg reg lit tex lit RRO reg reg PRMT reg reg lit reg DMNMX reg reg p DMNMX reg reg lit p FMNMX reg reg p FMNMX reg reg lit p RED mem reg VOTE reg p p VOTE p p POPC reg reg CSETP p p misc p ISCADD32I reg reg lit lit SHF reg reg lit reg SHF reg reg reg reg FCHK p reg reg 

**ICAL** lit JCAL const LDG reg mem ATOM reg mem reg reg XMAD reg reg reg XMAD reg reg lit reg XMAD reg reg reg const XMAD reg reg const reg **SYNC** SYNC misc STG mem reg IADD3 reg reg reg IADD3 reg reg lit reg IADD3 reg reg const reg VABSDIFF reg reg reg VABSDIFF reg reg lit reg DEPBAR sb lit bitfield DEPBAR sb lit DEPBAR bitfield DEPBAR LOP3 reg reg reg lit LOP3 p reg reg reg lit LOP3 reg reg const reg lit LOP3 reg reg lit reg lit TLDS reg reg lit tex channel TLDS reg reg reg lit tex channel TEXS reg reg lit tex channel TEXS reg reg reg lit tex channel LEA reg reg reg lit LEA reg reg reg LEA p reg reg lit LEA p reg reg reg LEA reg reg reg lit LEA reg reg reg LEA p reg reg reg LEA p reg reg reg lit LEA reg reg lit LEA reg reg lit lit LEA p reg reg lit LEA p reg reg lit lit DSET reg reg p DSET reg reg const p DSET reg reg lit p