1 Appendix - Opcodes

In this Appendix we list the opcodes for decoded instructions on each of the distinct ISAs we have explored. We group Compute Capability 3.0 with 2.x, rather than the rest of the 3.x generation. The first column in each table is the opcode's string and the operand types. We use 'reg' for general register operands, 'p' for predicate registers, 'lit' for literal (hexadecimal or decimal) values, 'mem' for memory, 'const' for constant memory, 'tex' for texture shapes, 'channel' for texture channels, 'bitfield' for bitfield operands, and 'misc' for operands without a clear type.

The second column is the binary, with zeros and ones for opcode bits, and the character 'x' in place of bits that are not controlled by the opcode, with the least significant bit on the left. Bits which affect the types of the operands are treated as opcode bits.

1.1 Opcodes on Compute Capabilities 2.x and 3.0

TODO (We didn't decode this one automatically, we mostly got it from asfermi's wiki, so formatting it like the tables below is going to be time-consuming.)

1.2 Opcodes on Compute Capability 3.x

Instruction	Bits
MOV reg reg lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100100111
MOV reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111xxxxxxxx1100100111
MOV reg const lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100100110
MOV reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111xxxxxxxx1100100110
MOV32I reg lit lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000101110
MOV32I reg lit	01xxxxxxxxxxxx1111xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000101110
LD reg mem	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx100100011
LDL reg mem	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001011110
LDS reg mem	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001011110
LDC reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100111110
ST mem reg	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx100100111
STL mem reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101011110
STS mem reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101011110
FADD reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101010011
FADD reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101000110
FADD reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101000111
FADD32I reg reg lit	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000010
FMUL reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011000110
FMUL reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011000011
FMUL reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011000111
FMUL32I reg reg lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000100
FFMA reg reg const reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx00110010
FFMA reg reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000110011
FFMA reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000111001
FFMA reg reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000110001
FSETP p p reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx110111010
FSETP p p reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110111011
FSETP p p reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110101101
DSETP p p reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000101101
DSETP p p reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000111010
DSETP p p reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000111011
FCMP reg reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010111011
FCMP reg reg const reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx010111010
MUFU reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000100001
DADD reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111000110
DADD reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111000011
DADD reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111000111

1	DMUL reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000100111	56
2	DMUL reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000110011	57
3	DMUL reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000100110	58
4	DFMA reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111001101	59
5	DFMA reg reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx111011001	60
6	DFMA reg reg const reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx111011010	61
7	DFMA reg reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111011011	62
8	IADD reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100000110	63
9	IADD reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100000111	64
10	IADD reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100000011	65
11	IADD32I reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000010	66
12	IMNMX reg reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010000011	67
13	IMNMX reg reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010000111	68
14	IMNMX reg reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010000110	69
15	IMUL reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110000110	70
16	IMUL reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110000011	71
17	IMUL reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110000111	72
18	IMUL32I reg reg lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx001110100	73
19	IMAD reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010000101	74
20	IMAD reg reg const reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx10001010	75
21	IMAD reg reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010001011	76
22	IMAD reg reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx010001001	77
23	ISCADD reg reg lit lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100000011	78
24	ISCADD reg reg reg lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100000111	79
25	ISCADD reg reg const lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100000110	80
26	ISET reg reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx101011010	81
27	ISETP p p reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011001101	82
28	ISETP p p reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011011011	83
29	ISETP p p reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx011011010	84
30	ICMP reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001011101	85
31	ICMP reg reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001011011	86
32	ICMP reg reg const reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx001011010	87
33	I2F reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110100110	88
34	I2F reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110100111	89
35	I2I reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001100110	90
36	I2I reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001100111	91
37	I2I reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001110011	92
38	F2I reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110100111	93
39	F2I reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110100110	94
40	F2F reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010100111	95
41	F2F reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010100110	96
42	LOP reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001000110	97
43	LOP reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001000011	98
44	LOP reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001000111	99
45	LOP32I reg reg lit	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000100	100
46	SHL reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001000110	101
47	SHR reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010000011	102
48	SHR reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010000110	103
49	BFE reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000000011	104
50	BFE reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000000110	105
51	BFI reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111101101	106
52	SEL reg reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010100111	107
53	SEL reg reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010100011	108
54	SEL reg reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010100110	109
55			110

#	Instruction	Encoding	#
111	SSY const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx100101000	166
112	SSY lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100101000	167
113	BRA const	00111101xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx001001000	168
114	BRA misc const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx001001000	169
115	BRA lit	00111100xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001001000	170
116	BRA misc lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001001000	171
117	BRX misc reg lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101001000	172
118	BRX reg lit	00111100xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101001000	173
119	BRX const	00111101xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx101001000	174
120	BRX misc const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx101001000	175
121	PCNT const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx110101000	176
122	PCNT lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110101000	177
123	CONT misc	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101011000	178
124	CONT	0011110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101011000	179
125	PBK lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010101000	180
126	PBK const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx010101000	181
127	BRK misc	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001011000	182
128	BRK	0011110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001011000	183
129	CAL const	00xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx011001000	184
130	CAL lit	00xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011001000	185
131	RET misc	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010011000	186
132	RET	0011110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010011000	187
133	EXIT misc	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000011000	188
134	EXIT	0011110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000011000	189
135	NOP misc lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110100001	190
136	NOP lit	01xxxxxxxx11110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110100001	191
137	BPT lit	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000000000	192
138	S2R reg sreg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001100001	193
139	PSETP p p p p p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100100001	194
140	PSET reg p p p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000100001	195
141	FLO reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110000111	196
142	FLO reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110000110	197
143	P2R reg misc reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001100011	198
144	P2R reg misc reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001100110	199
145	R2P misc reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000101100011	200
146	R2P misc reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx100101100110	201
147	TEX reg reg lit tex lit	10xxxxxxxxxxxxxxxxxxxxx11111111xxxxxxxxxxxxxxxxxxxxxxxxxxxx110	202
148	TEX reg reg reg lit tex lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx110	203
149	TEXDEPBAR lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011101110	204
150	RRO reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100100111	205
151	RRO reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100100110	206
152	PRMT reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001101101	207
153	DMNMX reg reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101000111	208
154	DMNMX reg reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101000110	209
155	FMNMX reg reg lit p	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011000011	210
156	FMNMX reg reg reg p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011000111	211
157	FMNMX reg reg const p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011000110	212
158	VOTE p p	0111111111xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101100001	213
159	VOTE reg p p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101100001	214
160	POPC reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000000111	215
161	POPC reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000000110	216
162	MEMBAR	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100111110	217
163	CSETP p p misc p	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010100001	218
164	ISCADD32I reg reg lit lit	00xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0xxxxx101	219
165			220

Instruction	Bits
TLD reg reg lit tex lit	01xxxxxxxxxxxxxxxxxxxxx11111111xxxxxxxxxxxxxxxxxxxxxxxxxxx1110
TLD reg reg reg lit tex lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110
SHF reg reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111111011
SHF reg reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111101101
FCHK p reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000100111
FCHK p reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000100110
ISUB reg const reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx01x0100000110
ISUB reg reg const	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx10x0100000110
ISUB reg reg reg	01xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx10x0100000111
ISUB reg lit reg	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx01x0100000011
ISUB reg reg lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx10x0100000011
LDG reg mem	10xxxxxxxxxxxxxxxxxxxxx111111110xx1111xxx000100011xxxxxxxxxxx110

1.3 Opcodes on Compute Capabilities 5.x and 6.x

Instruction	Bits
MOV reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111xxxxxxxxx1100100110010
MOV reg const lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100100110010
MOV reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111xxxxxxxxx1100100111010
MOV reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100100111010
MOV32I reg lit	xxxxxxxxxxxx1111xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000010000000
MOV32I reg lit lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000010000000
LD reg mem p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001xxxxxxxx1
LDL reg mem	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001011110111
LDS reg mem	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001011110111
LDC reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100111110111
ST mem reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx101
STL mem reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101011110111
STS mem reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101011110111
FADD reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101000111010
FADD reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101000110010
FADD reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101010011100
FADD32I reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000010000
FMUL reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011000111010
FMUL reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011000011100
FMUL reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011000110010
FMUL32I reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000001111000
FFMA reg reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000110001010
FFMA reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000101001100
FFMA reg reg const reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000110010010
FFMA reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000110011010
FSET reg reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001100001100
FSET reg reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000100011010
FSETP p p reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110101101100
FSETP p p reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110111011010
FSETP p p reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110111010010
DSETP p p reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000111011010
DSETP p p reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000101101100
DSETP p p reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000111010010
FCMP reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010111011010
FCMP reg reg const reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010111010010
FCMP reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010101101100
MUFU reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000100001010
DADD reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111000111010

#	Instruction	Encoding	#
331	DADD reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111000011100	386
332	DADD reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111000110010	387
333	DMUL reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000100111010	388
334	DMUL reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000110011100	389
335	DMUL reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000100110010	390
336	DFMA reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111011011010	391
337	DFMA reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111001101100	392
338	DFMA reg reg const reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111011010010	393
339	DFMA reg reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111011001010	394
340	IADD reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100000111010	395
341	IADD reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100000110010	396
342	IADD reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100000011100	397
343	IADD32I reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000111000	398
344	IMNMX reg reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010000110010	399
345	IMNMX reg reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010000111010	400
346	IMNMX reg reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010000011100	401
347	ISCADD reg reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100000111010	402
348	ISCADD reg reg lit lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100000011100	403
349	ISCADD reg reg const lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100000110010	404
350	ISET reg reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101011011010	405
351	ISET reg reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101011010010	406
352	ISET reg reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101001101100	407
353	ISETP p p reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011011011010	408
354	ISETP p p reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011001101100	409
355	ISETP p p reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011011010010	410
356	ICMP reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001011011010	411
357	ICMP reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001011101100	412
358	ICMP reg reg const reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001011010010	413
359	I2F reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110100111010	414
360	I2F reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110100110010	415
361	I2I reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011110011100	416
362	I2I reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011100111010	417
363	I2I reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011100110010	418
364	F2I reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110100111010	419
365	F2F reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010100111010	420
366	F2F reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010100110010	421
367	F2F reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010100011100	422
368	LOP reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110001000011100	423
369	LOP p reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000111010	424
370	LOP reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110001000111010	425
371	LOP p reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000110010	426
372	LOP reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110001000110010	427
373	LOP p reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000011100	428
374	LOP32I reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx000000100000	429
375	SHL reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001000011100	430
376	SHL reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001000111010	431
377	SHR reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010000011100	432
378	SHR reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1010000111010	433
379	BFE reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000000011100	434
380	BFI reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111101101100	435
381	SEL reg reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010100111010	436
382	SEL reg reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010100011100	437
383	SEL reg reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010100110010	438
384	SSY lit	xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100101000111	439
385			440

441	SSY const	xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100101000111	496
442	BRA const	111101xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001001000111	497
443	BRA misc const	xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001001000111	498
444	BRA lit	111100xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001001000111	499
445	BRA misc lit	xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001001000111	500
446	BRX const	111101xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101001000111	501
447	BRX misc const	xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101001000111	502
448	BRX reg lit	111100xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101001000111	503
449	BRX misc reg lit	xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101001000111	504
450	PCNT lit	xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110101000111	505
451	PCNT const	xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110101000111	506
452	CONT	11110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101011000111	507
453	CONT misc	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101011000111	508
454	PBK lit	xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010101000111	509
455	PBK const	xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010101000111	510
456	BRK	11110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001011000111	511
457	BRK misc	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001011000111	512
458	CAL lit	xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011001000111	513
459	CAL const	xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011001000111	514
460	RET	11110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010011000111	515
461	RET misc	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010011000111	516
462	EXIT	11110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000011000111	517
463	EXIT misc	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000011000111	518
464	NOP lit	xxxxxxxx11110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110100001010	519
465	NOP misc lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110100001010	520
466	NOP	xxxxxxxx11110xxxxxxx000000000000000xxxxxxxxxxxxxx0110100001010	521
467	NOP misc	xxxxxxxxxxxxxxxxxxx000000000000000xxxxxxxxxxxxxx0110100001010	522
468	BAR lit	xxxxxxxxxxxxxxxxxx00000000000000000011101100000010110100001111	523
469	BAR lit lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx11101100000010110100001111	524
470	S2R reg sreg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1001100001111	525
471	PSETP p p p p p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100100001010	526
472	PSET reg p p p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000100001010	527
473	FLO reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110000111010	528
474	TEX reg reg lit tex lit	xxxxxxxxxxxxxxxxxx11111111xxxxxxxxxxxxxxxxxxxxxx1110000000011	529
475	TEX reg reg reg lit tex lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110000000011	530
476	RRO reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0100100111010	531
477	PRMT reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001101101100	532
478	DMNMX reg reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101000111010	533
479	DMNMX reg reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101000011100	534
480	FMNMX reg reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011000111010	535
481	FMNMX reg reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011000011100	536
482	RED mem reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111111010111	537
483	VOTE reg p p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101100001010	538
484	VOTE p p	11111111xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101100001010	539
485	POPC reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000000111010	540
486	CSETP p p misc p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010100001010	541
487	ISCADD32I reg reg lit lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0xxxxx101000	542
488	SHF reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111101101100	543
489	SHF reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111111011010	544
490	FCHK p reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000100111010	545
491	JCAL lit	xxxxx0xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx010001000111	546
492	JCAL const	xxxxx1xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010001000111	547
493	LDG reg mem	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0101101110111	548
494	ATOM reg mem reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111101110111	549
495		6	550

XMAD reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000011011010	
XMAD reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0010001101100	
XMAD reg reg reg const	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0110010001010	
XMAD reg reg const reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000001110010	
SYNC	11110xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111100001111	
SYNC misc	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111100001111	
STG mem reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101101110111	
IADD3 reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001100111010	
IADD3 reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001100011100	
IADD3 reg reg const reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001100110010	
VABSDIFF reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx10010000101010	
VABSDIFF reg reg lit reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx00010000101010	
DEPBAR sb lit bitfield	xxxxxxxxxxxxxxxxxxxxxxxxxxx1xxxxxxxxxxxxxxxxxxx0111100001111	
DEPBAR sb lit	000000xxxxxxxxxxxxxxxxxxxxxx1xxxxxxxxxxxxxxxxxxx0111100001111	
DEPBAR bitfield	xxxxxxxxxxxxxxxxxxxxxxxxxxxx0xxxxxxxxxxxxxxxxxxx0111100001111	
DEPBAR	000000xxxxxxxxxxxxxxxxxxxxxx0xxxxxxxxxxxxxxxxxxx0111100001111	
LOP3 reg reg reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110011111011010	
LOP3 p reg reg reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx11111011010	
LOP3 reg reg const reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000000	
LOP3 reg reg lit reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx111100	
TLDS reg reg reg lit tex channel	xxxxxxxxxxxxxxxx11111111xxxxxxxxxxxxxxxxxxxxxxxxxxxx1011011	
TLDS reg reg reg reg lit tex channel	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1011011	
TEXS reg reg reg lit tex channel	xxxxxxxxxxxxxxxx11111111xxxxxxxxxxxxxxxxxxxxxxxxxxxx0011011	
TEXS reg reg reg reg lit tex channel	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011011	
LEA reg reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx11101011111011010	
LEA reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx00000xxxx1110101111011010	
LEA p reg reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx101111011010	
LEA p reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx00000xxxxxxxx101111011010	
LEA reg reg reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111101111011010	
LEA reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111101111011010	
LEA p reg reg reg reg	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101111011010	
LEA p reg reg reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1101111011010	
LEA reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110101101101100	
LEA reg reg lit lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110101101101100	
LEA p reg reg lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx101101101100	
LEA p reg reg lit lit	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx101101101100	
DSET reg reg reg p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1000010011010	
DSET reg reg const p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000010010010	
DSET reg reg lit p	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0001001001100	