

1 Appendix - Opcodes

In this Appendix we list the opcodes for decoded instructions on most of the distinct ISAs we have explored. We omit Compute Capabilities 3.x with 2.0, which have previously had their opcodes detailed in Asfermi [1]. The first column in each table is the opcode's string and the operand types. We use 'reg' for general register operands, 'p' for predicate registers, 'lit' for literal (hexadecimal or decimal) values, 'mem' for memory, 'const' for constant memory, 'tex' for texture shapes, 'channel' for texture channels, 'bitfield' for bitfield operands, and 'misc' for operands without a clear type.

The second column is the binary, with zeros and ones for opcode bits, and the character 'x' in place of bits that are not controlled by the opcode, with the least significant bit on the left. Bits which affect the types of the operands are treated as opcode bits.

1.1 Opcodes on Compute Capability 3.x

Table 1. Opcode lookup table: opcodeTable3x

Instruction	Bits
MOV reg reg lit	01xx1100100111
MOV reg reg	01xx1111xxxxxxxx1100100111
MOV reg const lit	01xx1100100110
MOV reg const	01xx1111xxxxxxxx1100100110
MOV32I reg lit lit	01xx0001011110
MOV32I reg lit	01xxxxxxxxxxxxxxxx1111xx0001011110
LD reg mem	00xx1001000111
LDL reg mem	01xx0001011110
LDS reg mem	01xx1001011110
LDC reg const	01xx0100111110
ST mem reg	00xx1001001111
STL mem reg	01xx0101011110
STS mem reg	01xx1101011110
FADD reg reg lit	10xx1101010011
FADD reg reg const	01xx1101000110
FADD reg reg reg	01xx1101000111
FADD32I reg reg lit	00xx000000010
FMUL reg reg const	01xx1011000110
FMUL reg reg lit	10xx1011000011
FMUL reg reg reg	01xx1011000111
FMUL32I reg reg lit	01xx000000100
FFMA reg reg const reg	01xx00110010
FFMA reg reg reg reg	01xx0000110011
FFMA reg reg lit reg	10xx0000111001
FFMA reg reg reg const	01xx000110001
FSETP p p reg const p	01xx110111010
FSETP p p reg reg p	01xx1110111011
FSETP p p reg lit p	10xx1110101101
DSETP p p reg lit p	10xx0000101101
DSETP p p reg const p	01xx000111010
DSETP p p reg reg p	01xx1000111011
FCMP reg reg reg reg	01xx0010111011
FCMP reg reg const reg	01xx010111010
MUFU reg reg	01xx0000100001
DADD reg reg const	01xx0111000110
DADD reg reg lit	10xx0111000011
DADD reg reg reg	01xx0111000111
DMUL reg reg reg	01xx0000100111
DMUL reg reg lit	10xx0000110011

1	DMUL reg reg const	01xxx0000100110	56
2	DFMA reg reg lit reg	10xxx0111001101	57
3	DFMA reg reg reg const	01xxx111011001	58
4	DFMA reg reg const reg	01xxx111011010	59
5	DFMA reg reg reg reg	01xxx0111011011	60
6	IADD reg reg const	01xxx0100000110	61
7	IADD reg reg reg	01xxx0100000111	62
8	IADD reg reg lit	10xxx0100000011	63
9	IADD32I reg reg lit	10xxx000000010	64
10	IMNMX reg reg lit p	10xxx0010000011	65
11	IMNMX reg reg reg p	01xxx0010000111	66
12	IMNMX reg reg const p	01xxx0010000110	67
13	IMUL reg reg const	01xxx1110000110	68
14	IMUL reg reg lit	10xxx1110000011	69
15	IMUL reg reg reg	01xxx1110000111	70
16	IMUL32I reg reg lit	01xxx001110100	71
17	IMAD reg reg lit reg	10xxx0010000101	72
18	IMAD reg reg const reg	01xxx10001010	73
19	IMAD reg reg reg reg	01xxx0010001011	74
20	IMAD reg reg reg const	01xxx010001001	75
21	ISCADD reg reg lit lit	10xxx1100000011	76
22	ISCADD reg reg reg lit	01xxx1100000111	77
23	ISCADD reg reg const lit	01xxx1100000110	78
24	ISSET reg reg const p	01xxx101011010	79
25	ISSETP p p reg lit p	10xxx1011001101	80
26	ISSETP p p reg reg p	01xxx1011011011	81
27	ISSETP p p reg const p	01xxx011011010	82
28	ICMP reg reg lit reg	10xxx1001011101	83
29	ICMP reg reg reg reg	01xxx0001011011	84
30	ICMP reg reg const reg	01xxx001011010	85
31	I2F reg const	01xxx1110100110	86
32	I2F reg reg	01xxx1110100111	87
33	I2I reg const	01xxx0001100110	88
34	I2I reg reg	01xxx0001100111	89
35	I2I reg lit	10xxx0001110011	90
36	F2I reg reg	01xxx0110100111	91
37	F2I reg const	01xxx0110100110	92
38	F2F reg reg	01xxx1010100111	93
39	F2F reg const	01xxx1010100110	94
40	LOP reg reg const	01xxx0001000110	95
41	LOP reg reg lit	10xxx0001000011	96
42	LOP reg reg reg	01xxx0001000111	97
43	LOP32I reg reg lit	00xxx000000100	98
44	SHL reg reg const	01xxx1001000110	99
45	SHR reg reg lit	10xxx1010000011	100
46	SHR reg reg const	01xxx1010000110	101
47	BFE reg reg lit	10xxx0000000011	102
48	BFE reg reg const	01xxx0000000110	103
49	BFI reg reg lit reg	10xxx0111101101	104
50	SEL reg reg reg p	01xxx0010100111	105
51	SEL reg reg lit p	10xxx0010100011	106
52	SEL reg reg const p	01xxx0010100110	107
53	SSY const	00xxxxxx1xxx100101000	108
54	SSY lit	00xxxxxx0xxx0100101000	109
55		2	110

111	BRA const	00111101xxx001001000	166
112	BRA misc const	00xxxxxx1xxx001001000	167
113	BRA lit	00111100xxx0001001000	168
114	BRA misc lit	00xxxxxx0xxx0001001000	169
115	BRX misc reg lit	00xxxxxx0xxx0101001000	170
116	BRX reg lit	00111100xxx0101001000	171
117	BRX const	00111101xxx101001000	172
118	BRX misc const	00xxxxxx1xxx101001000	173
119	PCNT const	00xxxxxx1xxx110101000	174
120	PCNT lit	00xxxxxx0xxx0110101000	175
121	CONT misc	00xxx0101011000	176
122	CONT	0011110xxx0101011000	177
123	PBK lit	00xxxxxx0xxx0010101000	178
124	PBK const	00xxxxxx1xxx010101000	179
125	BRK misc	00xxx0001011000	180
126	BRK	0011110xxx0001011000	181
127	CAL const	00xxxxxx1xxx011001000	182
128	CAL lit	00xxxxxx0xxx0011001000	183
129	RET misc	00xxx0010011000	184
130	RET	0011110xxx0010011000	185
131	EXIT misc	00xxx0000011000	186
132	EXIT	0011110xxx0000011000	187
133	NOP misc lit	01xxx0110100001	188
134	NOP lit	01xxxxxxxxxx11110xxx0110100001	189
135	BPT lit	00xxx0000000000	190
136	S2R reg sreg	01xxx1001100001	191
137	PSETP p p p p p	01xxx0100100001	192
138	PSET reg p p p	01xxx1000100001	193
139	FLO reg reg	01xxx0110000111	194
140	FLO reg const	01xxx0110000110	195
141	P2R reg misc reg lit	10xxx1001100011	196
142	P2R reg misc reg const	01xxx1001100110	197
143	R2P misc reg lit	10xxx000101100011	198
144	R2P misc reg const	01xxx100101100110	199
145	TEX reg reg lit tex lit	10xxxxxxxxxxxxxxxxxxxxxxxxxxx11111111xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx110	200
146	TEX reg reg reg lit tex lit	xxx110	201
147	TEXDEPBAR lit	01xxx0011101110	202
148	RRO reg reg	01xxx0100100111	203
149	RRO reg const	01xxx0100100110	204
150	PRMT reg reg lit reg	10xxx0001101101	205
151	DMNMX reg reg reg p	01xxx0101000111	206
152	DMNMX reg reg const p	01xxx0101000110	207
153	FMNMX reg reg lit p	10xxx0011000011	208
154	FMNMX reg reg reg p	01xxx0011000111	209
155	FMNMX reg reg const p	01xxx0011000110	210
156	VOTE p p	0111111111xxx1101100001	211
157	VOTE reg p p	01xxx1101100001	212
158	POPC reg reg reg	01xxx1000000111	213
159	POPC reg reg const	01xxx1000000110	214
160	MEMBAR	01xxx1100111110	215
161	CSETP p p misc p	01xxx0010100001	216
162	ISCADD32I reg reg lit lit	00xxx0xxxxx101	217
163	TLD reg reg lit tex lit	01xxxxxxxxxxxxxxxxxxxxxxxxxxx11111111xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1110	218
164	TLD reg reg reg lit tex lit	01xxx1110	219
165		3	220

221	SHF reg reg reg reg	01xxx111111011	276
222	SHF reg reg lit reg	10xxx1111101101	277
223	FCHK p reg reg	01xxx1000100111	278
224	FCHK p reg const	01xxx1000100110	279
225	ISUB reg const reg	01xxx01x0100000110	280
226	ISUB reg reg const	01xxx10x0100000110	281
227	ISUB reg reg reg	01xxx10x0100000111	282
228	ISUB reg lit reg	10xxx01x0100000011	283
229	ISUB reg reg lit	10xxx10x0100000011	284
230	LDB reg mem	10xxxxxxxxxxxxxxxxxxxxxxxxxx11111110xx1111xxx000100011xxxxxxxxxxx110	285

1.2 Opcodes on Compute Capabilities 5.x and 6.x

Table 2. Opcode lookup table: opcodeTable5x6x

	Instruction	Bits	
236	MOV reg const	xx1111xxxxxxxxx1100100110010	291
237	MOV reg const lit	xx1100100110010	292
238	MOV reg reg	xx1100100111010	293
239	MOV reg lit	xx1100100111010	294
240	MOV32I reg lit	xxxxxxxxxxx1111xx000010000000	295
241	MOV32I reg lit lit	xx000010000000	296
242	LD reg mem p	xx1001xxxxxxxx1	297
243	LDL reg mem	xx0001011110111	298
244	LDS reg mem	xx1001011110111	299
245	LDC reg const	xx0100111101111	300
246	ST mem reg p	xx101	301
247	STL mem reg	xx0101011110111	302
248	STS mem reg	xx1101011110111	303
249	FADD reg reg reg	xx1101000111010	304
250	FADD reg reg const	xx1101000110010	305
251	FADD reg reg lit	xx1101010011100	306
252	FADD32I reg reg lit	xx000000010000	307
253	FMUL reg reg reg	xx1011000111010	308
254	FMUL reg reg lit	xx1011000011100	309
255	FMUL reg reg const	xx1011000110010	310
256	FMUL32I reg reg lit	xx000001111000	311
257	FFMA reg reg reg const	xx0000110001010	312
258	FFMA reg reg lit reg	xx0000101001100	313
259	FFMA reg reg const reg	xx0000110010010	314
260	FFMA reg reg reg reg	xx0000110011010	315
261	FSET reg reg lit p	xx1001100001100	316
262	FSET reg reg reg p	xx1000100011010	317
263	FSETP p p reg lit p	xx1110101101100	318
264	FSETP p p reg reg p	xx1110111011010	319
265	FSETP p p reg const p	xx0110111010010	320
266	DSETP p p reg reg p	xx1000111011010	321
267	DSETP p p reg lit p	xx00001011011100	322
268	DSETP p p reg const p	xx1000111010010	323
269	FCMP reg reg reg reg	xx0010111011010	324
270	FCMP reg reg const reg	xx1010111010010	325
271	FCMP reg reg lit reg	xx10101011011100	326
272	MUFU reg reg	xx0000100001010	327
273	DADD reg reg reg	xx0111000111010	328
274			329

331	DADD reg reg lit	XX0111000011100	386
332	DADD reg reg const	XX0111000110010	387
333	DMUL reg reg reg	XX0000100111010	388
334	DMUL reg reg lit	XX0000110011100	389
335	DMUL reg reg const	XX0000100110010	390
336	DFMA reg reg reg reg	XX0111011011010	391
337	DFMA reg reg lit reg	XX0111001101100	392
338	DFMA reg reg const reg	XX0111011010010	393
339	DFMA reg reg reg const	XX0111011001010	394
340	IADD reg reg reg	XX0100000111010	395
341	IADD reg reg const	XX0100000110010	396
342	IADD reg reg lit	XX0100000011100	397
343	IADD32I reg reg lit	XX0000000111000	398
344	IMNMX reg reg const p	XX0010000110010	399
345	IMNMX reg reg reg p	XX0010000111010	400
346	IMNMX reg reg lit p	XX0010000011100	401
347	ISCADD reg reg reg lit	XX1100000111010	402
348	ISCADD reg reg lit lit	XX1100000011100	403
349	ISCADD reg reg const lit	XX1100000110010	404
350	ISSET reg reg reg p	XX0101011011010	405
351	ISSET reg reg const p	XX1101011010010	406
352	ISSET reg reg lit p	XX0101001101100	407
353	ISSETP p p reg reg p	XX1011011011010	408
354	ISSETP p p reg lit p	XX1011001101100	409
355	ISSETP p p reg const p	XX1011011010010	410
356	ICMP reg reg reg reg	XX0001011011010	411
357	ICMP reg reg lit reg	XX1001011101100	412
358	ICMP reg reg const reg	XX1001011010010	413
359	I2F reg reg	XX1110100111010	414
360	I2F reg const	XX1110100110010	415
361	I2I reg lit	XX0011110011100	416
362	I2I reg reg	XX00111100111010	417
363	I2I reg const	XX00111100110010	418
364	F2I reg reg	XX0110100111010	419
365	F2F reg reg	XX1010100111010	420
366	F2F reg const	XX1010100110010	421
367	F2F reg lit	XX1010100011100	422
368	LOP reg reg lit	XX1110001000011100	423
369	LOP p reg reg reg	XX100011101010	424
370	LOP reg reg reg	XX1110001000111010	425
371	LOP p reg reg const	XX100011001010	426
372	LOP reg reg const	XX1110001000110010	427
373	LOP p reg reg lit	XX10000111100	428
374	LOP32I reg reg lit	XX000000100000	429
375	SHL reg reg lit	XX1001000011100	430
376	SHL reg reg reg	XX1001000111010	431
377	SHR reg reg lit	XX1010000011100	432
378	SHR reg reg reg	XX1010000111010	433
379	BFE reg reg lit	XX0000000011100	434
380	BFI reg reg lit reg	XX0111101101100	435
381	SEL reg reg reg p	XX0010100111010	436
382	SEL reg reg lit p	XX0010100011100	437
383	SEL reg reg const p	XX0010100110010	438
384	SSY lit	xxxxx0xx0100101000111	439
385			440

441	SSY const	xxxxx1xx0100101000111	496
442	BRA const	111101xx0001001000111	497
443	BRA misc const	xxxxx1xx0001001000111	498
444	BRA lit	111100xx0001001000111	499
445	BRA misc lit	xxxxx0xx0001001000111	500
446	BRX const	111101xx0101001000111	501
447	BRX misc const	xxxxx1xx0101001000111	502
448	BRX reg lit	111100xx0101001000111	503
449	BRX misc reg lit	xxxxx0xx0101001000111	504
450	PCNT lit	xxxxx0xx0110101000111	505
451	PCNT const	xxxxx1xx0110101000111	506
452	CONT	11110xx0101011000111	507
453	CONT misc	xx0101011000111	508
454	PBK lit	xxxxx0xx0010101000111	509
455	PBK const	xxxxx1xx0010101000111	510
456	BRK	11110xx0001011000111	511
457	BRK misc	xx0001011000111	512
458	CAL lit	xxxxx0xx0011001000111	513
459	CAL const	xxxxx1xx0011001000111	514
460	RET	11110xx0010011000111	515
461	RET misc	xx0010011000111	516
462	EXIT	11110xx0000011000111	517
463	EXIT misc	xx0000011000111	518
464	NOP lit	xxxxxxxxx11110xx0110100001010	519
465	NOP misc lit	xx0110100001010	520
466	NOP	xxxxxxxxx11110xxxxxxxx0000000000000000xxxxxxxxxxxxxxxxxx0110100001010	521
467	NOP misc	xxxxxxxxxxxxxxxxxxxxxxxxxx0000000000000000xxxxxxxxxxxxxxxxxx0110100001010	522
468	BAR lit	xxxxxxxxxxxxxxxxxxxxxxxxxx0000000000000000000110110000001010100001111	523
469	BAR lit lit	xx1110110000001010100001111	524
470	S2R reg sreg	xx1001100001111	525
471	PSETP p p p p p	xx0100100001010	526
472	PSET reg p p p	xx1000100001010	527
473	FLO reg reg	xx0110000111010	528
474	TEX reg reg lit tex lit	xxxxxxxxxxxxxxxxxxxxxxxxxx1111111xxxxxxxxxxxxxxxxxxxxxxxxxx1110000000011	529
475	TEX reg reg reg lit tex lit	xx1110000000011	530
476	RRO reg reg	xx0100100111010	531
477	PRMT reg reg lit reg	xx0001101101100	532
478	DMNMX reg reg reg p	xx0101000111010	533
479	DMNMX reg reg lit p	xx0101000011100	534
480	FMNMX reg reg reg p	xx0011000111010	535
481	FMNMX reg reg lit p	xx0011000011100	536
482	RED mem reg	xx1111111010111	537
483	VOTE reg p p	xx1101100001010	538
484	VOTE p p	11111111xx1101100001010	539
485	POPC reg reg	xx1000000111010	540
486	CSETP p p misc p	xx0010100001010	541
487	ISCADD32I reg reg lit lit	xx0xxxxx101000	542
488	SHF reg reg lit reg	xx1111101101100	543
489	SHF reg reg reg reg	xx111111011010	544
490	FCHK p reg reg	xx1000100111010	545
491	JCAL lit	xxxxx0xx010001000111	546
492	JCAL const	xxxxx1xx0010001000111	547
493	LDG reg mem	xx0101101110111	548
494	ATOM reg mem reg reg	xx0111101110111	549
495			550

551	XMAD reg reg reg reg	XX0000011011010	606
552	XMAD reg reg lit reg	XX0010001101100	607
553	XMAD reg reg reg const	XX0110010001010	608
554	XMAD reg reg const reg	XX0000001110010	609
555	SYNC	11110XX1111100001111	610
556	SYNC misc	XX1111100001111	611
557	STG mem reg	XX1101101110111	612
558	IADD3 reg reg reg reg	XX0001100111010	613
559	IADD3 reg reg lit reg	XX00011000111100	614
560	IADD3 reg reg const reg	XX0001100110010	615
561	VABSDIFF reg reg reg reg	XX10010000101010	616
562	VABSDIFF reg reg lit reg	XX00010000101010	617
563	DEPBAR sb lit bitfield	XXXXXXXXXXXXXXXXXXXXXXXXXXXX1XXXXXXXXXXXXXXXXXXXXXXXXXXXX0111100001111	618
564	DEPBAR sb lit	000000XXXXXXXXXXXXXXXXXXXX1XXXXXXXXXXXXXXXXXXXXXXXXXXXX0111100001111	619
565	DEPBAR bitfield	XXXXXXXXXXXXXXXXXXXXXXXXXXXX0XXXXXXXXXXXXXXXXXXXXXXXXXXXX0111100001111	620
566	DEPBAR	000000XXXXXXXXXXXXXXXXXXXX0XXXXXXXXXXXXXXXXXXXXXXXXXXXX0111100001111	621
567	LOP3 reg reg reg reg lit	XX1110011111011010	622
568	LOP3 p reg reg reg reg lit	XX1111101101010	623
569	LOP3 reg reg const reg lit	XX1000000	624
570	LOP3 reg reg lit reg lit	XX111100	625
571	TLDS reg reg reg lit tex channel	XXXXXXXXXXXXXXXXXXXX1111111XXXXXXXXXXXXXXXXXXXXXXXXXXXX1011011	626
572	TLDS reg reg reg reg lit tex channel	XX1011011	627
573	TEXS reg reg reg lit tex channel	XXXXXXXXXXXXXXXXXXXX1111111XXXXXXXXXXXXXXXXXXXXXXXXXXXX0011011	628
574	TEXS reg reg reg reg lit tex channel	XX0011011	629
575	LEA reg reg reg lit	XX1110101111011010	630
576	LEA reg reg reg	XX00000XXXX1110101111011010	631
577	LEA p reg reg reg lit	XX10111101101010	632
578	LEA p reg reg reg	XX00000XXXX10111101101010	633
579	LEA reg reg reg reg lit	XX111110111101101010	634
580	LEA reg reg reg reg	XX111110111101101010	635
581	LEA p reg reg reg reg	XX1101111011011010	636
582	LEA p reg reg reg reg lit	XX1101111011011010	637
583	LEA reg reg lit	XX11101011011011100	638
584	LEA reg reg lit lit	XX11101011011011100	639
585	LEA p reg reg lit	XX1011011011100	640
586	LEA p reg reg lit lit	XX1011011011100	641
587	DSET reg reg reg p	XX1000010011010	642
588	DSET reg reg const p	XX0000010010010	643
589	DSET reg reg lit p	XX0001001001100	644

References

- [1] Yunqing Hou, J Lai, and D Mikushin. 2011. Asfermi: An assembler for the NVIDIA Fermi instruction set. URL: <http://code.google.com/p/asfermi/> (accessed: 03.12. 2012) (2011).