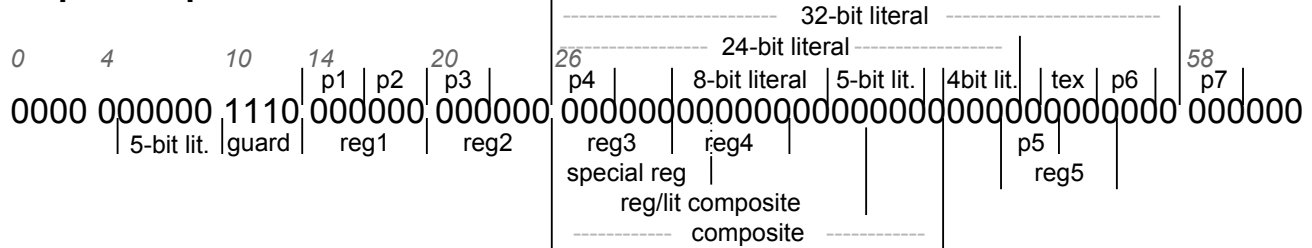


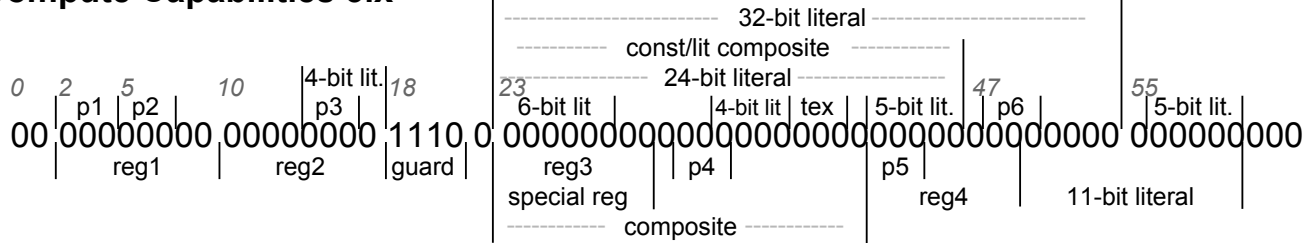
## Appendix - Decoded Instructions

This appendix contains a list of decoded instructions for the distinct ISAs we have explored. We enclose optional operands in parentheses. Operands use the names indicated by Figure 1. A specific operand name in the tables here correspond to a specific range of bits in Figure 1. We include official descriptions of the instructions from NVIDIA's CUDA Toolkit Documentation.

### Compute Capabilities 2.x and 3.0



### Compute Capabilities 3.x



### Compute Capabilities 5.x and 6.x

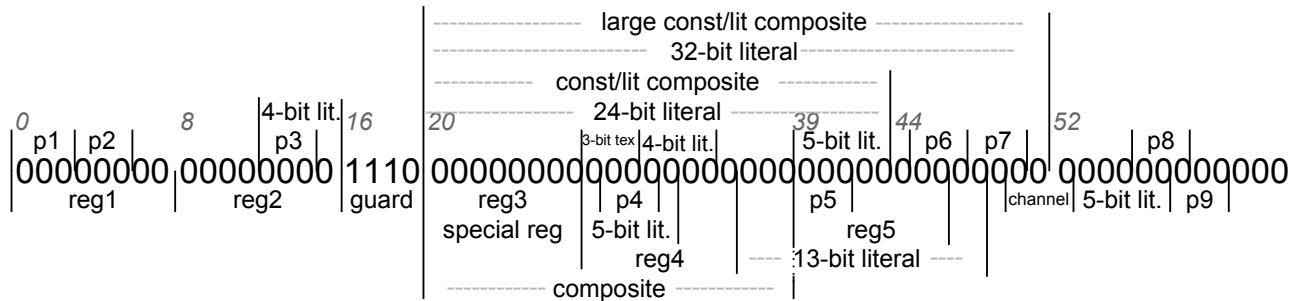


Figure 1. Common operands on different CUDA architectures.

### Instructions for Compute Capabilities 2.x and 3.0

Instruction	Official Description
VOTE (reg1), p6, p3	Query condition across threads
CCTL (reg1), [reg2 + 30-bit lit]	Cache Control
MOV32I, reg1, 32-bit lit	((undocumented))
MOV reg1, composite	Move
LDC reg1, const_mem_with_reg2	Load from Constant
SEL reg1, reg2, composite, p5	Conditional Select/Move
B2R reg1, 6-bit lit, p4	Barrier to Register
S2R reg1, special reg	Special Register to Register
P2R reg1, PR, reg2, composite	Predicate to Register
R2P PR, reg2, composite	Register to Predicate
TEX reg1, reg2, (reg3), 8-bit lit, 5-bit lit, tex, 4-bit lit	Texture Fetch
TLD reg1, reg2, 8-bit lit, tex, 4-bit lit	Texture Load

1	LEPC reg1	Load Effective PC	56
2	I2F reg1, composite	Integer to Float	57
3	I2I reg1, composite	Integer to Integer	58
4	F2I reg1, composite	Float to Integer	59
5	F2F reg1, composite	Float to Float	60
6	MUFU reg1, reg2	FP Multi-Function Operator	61
7	FLO reg1, composite	Integer Find Leading One	62
8	RRO reg1, composite	FP Range Reduction Operator	63
9	ISCADD32I reg1, reg2, 32-bit lit, 5-bit lit	((undocumented))	64
10	FADD32I reg1, reg2, 32-bit lit	((undocumented))	65
11	FMUL32I reg1, reg2, 32-bit lit	((undocumented))	66
12	IADD32I reg1, reg2, 32-bit lit	((undocumented))	67
13	IMUL32I reg1, reg2, 32-bit lit	((undocumented))	68
14	LOP32I reg1, reg2, 32-bit lit	((undocumented))	69
15	FADD reg1, reg2, composite	FP32 Add	70
16	FMUL reg1, reg2, composite	FP32 Multiply	71
17	DADD reg1, reg2, composite	FP64 Add	72
18	DMUL reg1, reg2, composite	FP64 Multiply	73
19	IADD reg1, reg2, composite	Integer Add	74
20	ISUB reg1, reg2 <=> composite	((undocumented))	75
21	IMUL reg1, reg2, composite	Integer Multiply	76
22	LOP reg1, reg2, composite	Integer Logic Op	77
23	SHL reg1, reg2, composite	Integer Shift Left	78
24	SHR reg1, reg2, composite	Integer Shift Right	79
25	BFE reg1, reg2, composite	Integer Bit Field Extract	80
26	POPC reg1, reg2, reg3	Population Count	81
27	FFMA reg1, reg2, composite <=> reg5	FP32 Fused Multiply Add	82
28	DFMA reg1, reg2, composite <=> reg5	FP64 Fused Multiply Add	83
29	IMAD reg1, reg2, composite <=> reg5	Integer Multiply Add	84
30	FCMP reg1, reg2, composite, reg5	FP32 Compare	85
31	ICMP reg1, reg2, composite, reg5	Integer Compare and Select	86
32	BFI reg1, reg2, composite, reg5	Integer Bit Field Insert	87
33	PRMT reg1, reg2, composite, reg5	Permute	88
34	FSET reg1, reg2, composite, p5	FP32 Set	89
35	ISSET reg1, reg2, composite, p5	Integer Set	90
36	PSET reg1, p3/p5, p4, p5/p3	Predicate Set	91
37	FMNMX reg1, reg2, composite, p5	FP32 Minimum/Maximum	92
38	DMNMX reg1, reg2, composite, p5	FP64 Minimum/Maximum	93
39	IMNMX reg1, reg2, composite, p5	Integer Minimum/Maximum	94
40	VMNMX reg1, reg2, reg3, reg5	((undocumented))	95
41	ISCADD reg1, reg2, composite, 5-bit lit	Integer Scaled Add	96
42	VADD reg1, reg2, reg/lit composite, reg5	((undocumented))	97
43	BRX reg2, 24-bit lit	Branch to Relative Indexed Address	98
44	SSY 24-bit lit	Set Sync Relative Address	99
45	BRA 24-bit lit	Branch to Relative Address	100
46	PCNT 24-bit lit	Pre-Continue Relative Address	101
47	PBK 24-bit lit	Pre-Break Relative Address	102
48	CAL 24-bit lit	Call to Relative Address	103
49	JCAL 24-bit lit	Call to Absolute Address	104
50	TEXDEPBAR composite	((undocumented))	105
51	DSETP p2, p1, reg2, composite, p5	FP64 Set Predicate	106
52	ISSETP p2, p1, reg2, composite, p5	Integer Set Predicate	107
53	FSETP p2, p1, reg2, composite, p5	FP32 Set Predicate	108
54	CSETP p2, p1, CC, p5	CC Set Predicate	109
55			110

111	PSETP p2, p1, p3/p5, p4, p5/p3	Predicate Set Predicate	166
112	STSCUL p, [reg2 + ??lit], reg1	Store to Shared Memory Conditionally and Unlock	167
113	LDLK p, reg1, [reg2 + 32-bit lit]	Load and Lock	168
114	LDSLK p7, reg1, [reg2 + 24-bit lit]	Load from Shared Memory and Lock	169
115	LD reg1, [reg2 + 32-bit lit]	Load from Memory	170
116	LDU reg1, [reg2 + 32-bit lit]	Load Uniform	171
117	LDL reg1, [reg2 + 24-bit lit]	Load from Local Memory	172
118	LDS reg1, [reg2 + 24-bit lit]	Load from Shared Memory and Lock	173
119	STL [reg2 + 24-bit lit], reg1	Store to Local Memory	174
120	STS [reg2 + 24-bit lit], reg1	Store to Shared Memory and Unlock	175
121	STSUL [reg2 + 24-bit lit], reg1	Store to Shared Memory and Unlock	176
122	ST [reg2 + 32-bit lit], reg1	Store to Memory	177
123	STUL [reg2 + 32-bit lit], reg1	Store and Unlock	178
124	RED [reg2 + 32-bit lit], reg1	Atomic Memory Reduction Operation	179
125	ATOM too complicated	Atomic Memory Operation	180
126	LD_LDU reg4, reg1, [reg2 + 6-bit lit], [reg3 + 6-bit lit]	A combination of a generic load LD with a load uniform LDU	181
127	NOP (CC)	No Operation	182
128	CONT	Continue in Loop	183
129	BRK	Break from Loop	184
130	RET	Return from Call	185
131	EXIT	Exit Program	186
132	BPT	Breakpoint/Trap	187
133	MEMBAR	Memory Barrier	188
134			189
135			190

### Instructions for Compute Capability 3.x

136			191
137			192
138	Instruction	Official Description	193
139	FCHK p2, reg2, composite	FP32 Division Test	194
140	VOTE (reg1), p6, p5	Query condition across threads	195
141	LDC reg1, const_mem_with_reg2	Load Constant	196
142	MOV reg1, composite, (5-bit lit)	Move	197
143	MOV32I reg1, 32-bit lit, (4-bit lit)	((undocumented))	198
144	S2R reg1, special reg	Move Special Register to Register	199
145	P2R reg1, PR, reg2, composite	Predicate to Register	200
146	R2P PR, reg1, composite	Register to Predicate	201
147	SEL reg1, reg2, composite, p5	Conditional Select/Move	202
148	TEX reg1, reg2, (reg3), 14-bit lit, tex, 4-bit lit	Texture Fetch	203
149	TLD reg1, reg2, (reg3), 15-bit lit tex, 4-bit lit	Texture Load	204
150	F2F reg1, composite	Floating Point To Floating Point Conversion	205
151	F2I reg1, composite	Floating Point To Integer Conversion	206
152	I2F reg1, composite	Integer To Floating Point Conversion	207
153	I2I reg1, composite	Integer To Integer Conversion	208
154	MUFU reg1, reg2	FP32 Multi Function Operation	209
155	FLO reg1, composite	Find Leading One	210
156	RRO reg1, composite	Range Reduction Operator FP	211
157	FADD32I reg1, reg2, 32-bit lit	((undocumented))	212
158	FMUL32I reg1, reg2, 32-bit lit	((undocumented))	213
159	IADD32I reg1, reg2, 32-bit lit	((undocumented))	214
160	IMUL32I reg1, reg2, 32-bit lit	((undocumented))	215
161	LOP32I reg1, reg2, 32-bit lit	((undocumented))	216
162	BFE reg1, reg2, composite	Integer Bit Field Extract	217
163	IADD reg1, reg2, composite	Integer Addition	218
164	IMUL reg1, reg2, composite	Integer Multiply	219
165			220

221	ISUB reg1, composite, reg2	((undocumented))	276
222	ISUB reg1, reg2, composite	((undocumented))	277
223	DADD reg1, reg2, composite	FP64 Add	278
224	DMUL reg1, reg2, composite	FP64 Multiply	279
225	FADD reg1, reg2, composite	FP32 Add	280
226	FMUL reg1, reg2, composite	FP32 Multiply	281
227	LOP reg1, reg2, composite	Integer Logic Op	282
228	POPC reg1, reg2, composite	Population Count	283
229	SHL reg1, reg2, composite	Integer Shift Left	284
230	SHR reg1, reg2, composite	Integer Shift Right	285
231	ISSET reg1, reg2, composite, p5	Integer Set	286
232	PSET reg1, p3, p4, p5	Predicate Set	287
233	DFMA reg1, reg2, composite <-> reg4	FP64 Fused Multiply Add	288
234	FFMA reg1, reg2, composite <-> reg4	FP32 Fused Multiply Add	289
235	IMAD reg1, reg2, composite <-> reg4	Integer Multiply And Add	290
236	DMNMX reg1, reg2, composite, p5	FP64 Minimum/Maximum	291
237	FMNMX reg1, reg2, composite, p5	FP32 Minimum/Maximum	292
238	IMNMX reg1, reg2, composite, p5	Integer Minimum/Maximum	293
239	BFI reg1, reg2, composite, reg4	Integer Bit Field Insert	294
240	PRMT reg1, reg2, composite, reg4	Permute	295
241	SHF reg1, reg2, composite, reg4	Integer Funnel Shift	296
242	FCMP reg1, reg2, composite, reg4	FP32 Compare to Zero and Select Source	297
243	ICMP reg1, reg2, composite, reg4	Integer Compare to Zero and Select Source	298
244	ISCADD reg1, reg2, composite, 5-bit lit	Scaled Integer Addition	299
245	ISCADD32I reg1, reg2, 32-bit lit, 5-bit lit	((undocumented))	300
246	BRA (CC), const/lit composite	Relative Branch	301
247	BRX (CC), const_mem_with_reg2	Relative Branch Indirect	302
248	BRX (CC), reg2, 24-bit lit	Relative Branch Indirect	303
249	CAL const/lit composite	Relative Call	304
250	PBK const/lit composite	Pre-Break	305
251	PCNT const/lit composite	Pre-continue	306
252	SSY const/lit composite	Set Synchronization Point	307
253	TEXDEPBAR 6-bit lit	((undocumented))	308
254	DSETP p2, p1, reg2, composite, p5	FP64 Set Predicate	309
255	FSETP p2, p1, reg2, composite, p5	FP32 Set Predicate	310
256	ISSETP p2, p1, reg2, composite, p5	Integer Set Predicate	311
257	CSETP p2, p1, CC, p5	CC Set Predicate	312
258	PSETP p2, p1, p3, p4, p5	Predicate Set Predicate	313
259	LDG reg1, [reg2 + 11-bit lit]	Non-coherent Global Memory Load	314
260	LD reg1, [reg2 + 32-bit lit]	Load from Memory	315
261	LDL reg1, [reg2 + 24-bit lit]	Load from Local Memory	316
262	LDS reg1, [reg2 + 24-bit lit]	Load from Shared Memory	317
263	ST [reg2 + 32-bit lit], reg1	Store to Memory	318
264	STL [reg2 + 24-bit lit], reg1	Store to Local Memory	319
265	STS [reg2 + 24-bit lit], reg1	Store to Shared Memory	320
266	BPT	Breakpoint/Trap	321
267	BRK (CC)	Break	322
268	CONT (CC)	Continue	323
269	EXIT (CC)	Exit Program	324
270	MEMBAR	Memory Barrier	325
271	NOP (CC)	No Operation	326
272	RET (CC)	Return From Subroutine	327
273			328
274			329
275			330

## Instructions for Compute Capabilities 5.x and 6.x

Instruction	Official Description
FCHK p2, reg2, composite	Single Precision FP Divide Range Check
VOTE (reg1), p6, p5	Vote Across SIMD Thread Group
LDC reg1, const_mem_with_reg2	Load Constant
MOV reg1, composite, (5-bit lit)	Move
MOV32I reg1, 32-bit lit, (4-bit lit)	((undocumented))
S2R reg1, special_reg	Move Special Register to Register
SEL reg1, reg2, composite, p5	Select Source with Predicate
TEX reg1, reg2, (reg3), 13-bit lit, 3-bit tex, 4-bit lit	Texture Fetch
TEXS reg4, reg1, reg2, (reg3), 13-bit lit, 1-bit tex, channel	Texture Fetch with scalar/non-vec4 source/destinations
TLDS reg4, reg1, reg2, (reg3), 13-bit lit, 1-bit tex, channel	Texture Load with scalar/non-vec4 source/destinations
I2I reg1, composite	Integer To Integer Conversion
I2F reg1, composite	Integer To Floating Point Conversion
F2I reg1, composite	Floating Point To Integer Conversion
F2F reg1, composite	Floating Point To Floating Point Conversion
MUFU reg1, reg2	Multi Function Operation
FLO reg1, composite	Find Leading One
POPC reg1, composite	Population count
RRO reg1, composite	Range Reduction Operator FP
FADD32I reg1, reg2, 32-bit lit	((undocumented))
FMUL32I reg1, reg2, 32-bit lit	((undocumented))
IADD32I reg1, reg2, 32-bit lit	((undocumented))
LOP32I reg1, reg2, 32-bit lit	((undocumented))
BFE reg1, reg2, composite	Bit Field Extract
DADD reg1, reg2, composite	FP64 Add
DMUL reg1, reg2, composite	FP64 Multiply
FADD reg1, reg2, composite	FP32 Add
FMUL reg1, reg2, composite	FP32 Multiply
IADD reg1, reg2, composite	Integer Addition
SHL reg1, reg2, composite	Shift Left
SHR reg1, reg2, composite	Shift Right
LOP (p7), reg1, reg2, composite	Logic Operation
BFI reg1, reg2, composite, reg5	Bit Field Insert
PRMT reg1, reg2, composite, reg5	Permute Register Pair
DFMA reg1, reg2, composite <=> reg5	FP64 Fused Multiply Add
FFMA reg1, reg2, composite <=> reg5	FP32 Fused Multiply and Add
FCMP reg1, reg2, composite, reg5	FP32 Compare to Zero and Select Source
IADD3 reg1, reg2, composite, reg5	3-input Integer Addition
ICMP reg1, reg2, composite, reg5	Integer Compare to Zero and Select Source
XMAD reg1, reg2, composite <=> reg5	Integer Short Multiply Add
SHF reg1, reg2, composite, reg5	Funnel Shift
VABSDIFF reg1, reg2, composite, reg5	((undocumented))
IMNMX reg1, reg2, composite, p5	Integer Minimum/Maximum
DMNMX reg1, reg2, composite, p5	FP64 Minimum/Maximum
FMNMX reg1, reg2, composite, p5	FP32 Minimum/Maximum
ISCADD reg1, reg2, composite, 5-bit lit	Scaled Integer Addition
ISCADD32I reg1, reg2, 32-bit lit, 5-bit lit	((undocumented))
DSET reg1, reg2, composite, p5	FP64 Compare And Set
FSET reg1, reg2, composite, p5	FP32 Compare And Set
ISSET reg1, reg2, composite, p5	Integer Compare And Set
PSET reg1, p3, p4, p5	Combine Predicates and Set
LOP3 (p7), reg1, reg2, reg3, reg5, 8-bit lit	3-input Logic Operation

441	LOP3 reg1, reg2, composite, reg5, 9-bit lit	3-input Logic Operation	496
442	LEA (p7), reg1, reg2, 19-bit lit, (5-bit lit)	Compute Effective Address	497
443	LEA (p7), reg1, reg2, reg3, reg5, (5-bit lit)	Compute Effective Address	498
444	LEA (p7), reg1, reg2, reg3, (5-bit lit)	Compute Effective Address	499
445	PSETP p2, p1, p3, p4, p5	Combine Predicates and Set Predicate	500
446	DSETP p2, p1, reg2, composite, p5	FP64 Compare And Set Predicate	501
447	FSETP p2, p1, reg2, composite, p5	FP32 Compare And Set Predicate	502
448	ISSETP p2, p1, reg2, composite, p5	Integer Compare And Set Predicate	503
449	CSETP p2, p1, CC, p5	Test Condition Code and Set Predicate	504
450	BAR 8-bit lit, (19-bit lit)	Barrier Synchronization	505
451	BRA (CC), const/lit composite	Relative Branch	506
452	CAL const/lit composite	Relative Call	507
453	PBK const/lit composite	Pre-Break	508
454	PCNT const/lit composite	Pre-continue	509
455	SSY const/lit composite	Set Synchronization Point	510
456	JCAL large const/lit composite	Absolute Call	511
457	BRX (CC), const_mem_with_reg2	Relative Branch Indirect	512
458	BRX (CC), reg2, 24-bit lit	Relative Branch Indirect	513
459	DEPBAR (sb, 6-bit lit), (bitfield)	((undocumented))	514
460	LD reg1, [reg2 + 32-bit lit], p8	Load from generic Memory	515
461	ST [reg2 + 32-bit lit], reg1, p9	Store to generic Memory	516
462	LDG reg1, [reg2 + 24-bit lit]	Load from Global Memory	517
463	LDL reg1, [reg2 + 24-bit lit]	Load within Local Memory Window	518
464	LDS reg1, [reg2 + 24-bit lit]	Local within Shared Memory Window	519
465	STG [reg2 + 24-bit lit], reg1	Store to global Memory	520
466	STL [reg2 + 24-bit lit], reg1	Store within Local or Shared Window	521
467	STS [reg2 + 24-bit lit], reg1	Store within Local or Shared Window	522
468	RED [reg2 + 20-bit lit], reg1	Reduction Operation on generic Memory	523
469	NOP (CC), 16-bit lit	No Operation	524
470	BRK (CC)	Break	525
471	CONT (CC)	Continue	526
472	EXIT (CC)	Exit Program	527
473	RET (CC)	Return From Subroutine	528
474	SYNC (CC)	Converge threads after conditional branch	529
475			530
476			531
477			532
478			533
479			534
480			535
481			536
482			537
483			538
484			539
485			540
486			541
487			542
488			543
489			544
490			545
491			546
492			547
493			548
494			549
495			550

## Appendix - Opcodes

In this Appendix we list the opcodes for decoded instructions on most of the distinct ISAs we have explored. We omit Compute Capabilities 2.x and 3.0, which have previously had their opcodes detailed in Asfermi [1].

The first column in each table is the opcode's string and the operand types. We use 'reg' for general register operands, 'p' for predicate registers, 'lit' for literal (hexadecimal or decimal) values, 'mem' for memory, 'const' for constant memory, 'tex' for texture shapes, 'channel' for texture channels, 'bitfield' for bitfield operands, and 'misc' for operands without a clear type.

The second column is the binary, with zeros and ones for opcode bits, and the character 'x' in place of bits that are not controlled by the opcode, with the least significant bit on the left. Bits which affect the types of the operands are treated as opcode bits.

### Opcodes on Compute Capability 3.x

**Table 4.** Opcode lookup table: opcodeTable3x

Instruction	Bits
MOV reg reg lit	01xx1100100111
MOV reg reg	01xx1111xxxxxxxx1100100111
MOV reg const lit	01xx1100100110
MOV reg const	01xx1111xxxxxxxx1100100110
MOV32I reg lit lit	01xx0001011110
MOV32I reg lit	01xxxxxxxxxxxx1111xx0001011110
LD reg mem	00xx100100011
LDL reg mem	01xx0001011110
LDS reg mem	01xx1001011110
LDC reg const	01xx0100111110
ST mem reg	00xx100100111
STL mem reg	01xx0101011110
STS mem reg	01xx1101011110
FADD reg reg lit	10xx1101010011
FADD reg reg const	01xx1101000110
FADD reg reg reg	01xx1101000111
FADD32I reg reg lit	00xx000000010
FMUL reg reg const	01xx1011000110
FMUL reg reg lit	10xx1011000011
FMUL reg reg reg	01xx1011000111
FMUL32I reg reg lit	01xx000000100
FFMA reg reg const reg	01xx00110010
FFMA reg reg reg reg	01xx0000110011
FFMA reg reg lit reg	10xx0000111001
FFMA reg reg reg const	01xx000110001
FSETP p p reg const p	01xx110111010
FSETP p p reg reg p	01xx1110111011
FSETP p p reg lit p	10xx1110101101
DSETP p p reg lit p	10xx0000101101
DSETP p p reg const p	01xx000111010
DSETP p p reg reg p	01xx1000111011
FCMP reg reg reg reg	01xx0010111011
FCMP reg reg const reg	01xx010111010
MUFU reg reg	01xx0000100001
DADD reg reg const	01xx0111000110
DADD reg reg lit	10xx0111000011
DADD reg reg reg	01xx0111000111
DMUL reg reg reg	01xx0000100111
DMUL reg reg lit	10xx0000110011



661	DMUL reg reg const	01xxx0000100110	716
662	DFMA reg reg lit reg	10xxx0111001101	717
663	DFMA reg reg reg const	01xxx111011001	718
664	DFMA reg reg const reg	01xxx111011010	719
665	DFMA reg reg reg reg	01xxx0111011011	720
666	IADD reg reg const	01xxx0100000110	721
667	IADD reg reg reg	01xxx0100000111	722
668	IADD reg reg lit	10xxx0100000011	723
669	IADD32I reg reg lit	10xxx0000000010	724
670	IMNMX reg reg lit p	10xxx0010000011	725
671	IMNMX reg reg reg p	01xxx0010000111	726
672	IMNMX reg reg const p	01xxx0010000110	727
673	IMUL reg reg const	01xxx1110000110	728
674	IMUL reg reg lit	10xxx1110000011	729
675	IMUL reg reg reg	01xxx1110000111	730
676	IMUL32I reg reg lit	01xxx001110100	731
677	IMAD reg reg lit reg	10xxx0010000101	732
678	IMAD reg reg const reg	01xxx10001010	733
679	IMAD reg reg reg reg	01xxx0010001011	734
680	IMAD reg reg reg const	01xxx010001001	735
681	ISCADD reg reg lit lit	10xxx1100000011	736
682	ISCADD reg reg reg lit	01xxx1100000111	737
683	ISCADD reg reg const lit	01xxx1100000110	738
684	ISSET reg reg const p	01xxx101011010	739
685	ISETP p p reg lit p	10xxx1011001101	740
686	ISETP p p reg reg p	01xxx1011011011	741
687	ISETP p p reg const p	01xxx011011010	742
688	ICMP reg reg lit reg	10xxx1001011101	743
689	ICMP reg reg reg reg	01xxx0001011011	744
690	ICMP reg reg const reg	01xxx001011010	745
691	I2F reg const	01xxx1110100110	746
692	I2F reg reg	01xxx1110100111	747
693	I2I reg const	01xxx0001100110	748
694	I2I reg reg	01xxx0001100111	749
695	I2I reg lit	10xxx0001110011	750
696	F2I reg reg	01xxx0110100111	751
697	F2I reg const	01xxx0110100110	752
698	F2F reg reg	01xxx1010100111	753
699	F2F reg const	01xxx1010100110	754
700	LOP reg reg const	01xxx0001000110	755
701	LOP reg reg lit	10xxx0001000011	756
702	LOP reg reg reg	01xxx0001000111	757
703	LOP32I reg reg lit	00xxx000000100	758
704	SHL reg reg const	01xxx1001000110	759
705	SHR reg reg lit	10xxx1010000011	760
706	SHR reg reg const	01xxx1010000110	761
707	BFE reg reg lit	10xxx0000000011	762
708	BFE reg reg const	01xxx0000000110	763
709	BFI reg reg lit reg	10xxx0111101101	764
710	SEL reg reg reg p	01xxx0010100111	765
711	SEL reg reg lit p	10xxx0010100011	766
712	SEL reg reg const p	01xxx0010100110	767
713	SSY const	00xxxxx1xx100101000	768
714	SSY lit	00xxxxx0xx0100101000	769
715		8	770



9

881	SHF reg reg reg reg	01xx111111011	936
882	SHF reg reg lit reg	10xx1111101101	937
883	FCHK p reg reg	01xx1000100111	938
884	FCHK p reg const	01xx1000100110	939
885	ISUB reg const reg	01xx01x0100000110	940
886	ISUB reg reg const	01xx10x0100000110	941
887	ISUB reg reg reg	01xx10x0100000111	942
888	ISUB reg lit reg	10xx01x0100000011	943
889	ISUB reg reg lit	10xx10x0100000011	944
890	LDG reg mem	10xxxxxxxxxxxxxxxxxxxxxxxx11111110xx1111xx000100011xxxxxxxxxx110	945

## Opcodes on Compute Capabilities 5.x and 6.x

**Table 5.** Opcode lookup table: opcodeTable5x6x

	Instruction	Bits	
896			950
897	MOV reg const	xx1111xxxxxxxxx1100100110010	951
898	MOV reg const lit	xxx1100100110010	952
899	MOV reg reg	xx1111xxxxxxxxx1100100111010	953
900	MOV reg reg lit	xxx1100100111010	954
901	MOV32I reg lit	xxxxxxxxxxxxxx1111xx000010000000	955
902	MOV32I reg lit lit	xxx000010000000	956
903	LD reg mem p	xxx1001xxxxxxxx1	957
904	LDL reg mem	xxx0001011110111	958
905	LDS reg mem	xxx1001011110111	959
906	LDC reg const	xxx0100111110111	960
907	ST mem reg p	xxx101	961
908	STL mem reg	xxx0101011110111	962
909	STS mem reg	xxx1101011110111	963
910	FADD reg reg reg	xxx1101000111010	964
911	FADD reg reg const	xxx1101000110010	965
912	FADD reg reg lit	xxx1101010011100	966
913	FADD32I reg reg lit	xxx000000010000	967
914	FMUL reg reg reg	xxx1011000111010	968
915	FMUL reg reg lit	xxx1011000011100	969
916	FMUL reg reg const	xxx1011000110010	970
917	FMUL32I reg reg lit	xxx000001111000	971
918	FFMA reg reg reg const	xxx0000110001010	972
919	FFMA reg reg lit reg	xxx0000101001100	973
920	FFMA reg reg const reg	xxx0000110010010	974
921	FFMA reg reg reg reg	xxx0000110011010	975
922	FSET reg reg lit p	xxx1001100001100	976
923	FSET reg reg reg p	xxx1000100011010	977
924	FSETP p p reg lit p	xxx1110101101100	978
925	FSETP p p reg reg p	xxx1110111011010	979
926	FSETP p p reg const p	xxx0110111010010	980
927	DSETP p p reg reg p	xxx1000111011010	981
928	DSETP p p reg lit p	xxx00001011101100	982
929	DSETP p p reg const p	xxx1000111010010	983
930	FCMP reg reg reg reg	xxx0010111011010	984
931	FCMP reg reg const reg	xxx1010111010010	985
932	FCMP reg reg lit reg	xxx1010101101100	986
933	MUFU reg reg	xxx0000100001010	987
934	DADD reg reg reg	xxx0111000111010	988
			989

991	DADD reg reg lit	XX0111000011100	1046
992	DADD reg reg const	XX0111000110010	1047
993	DMUL reg reg reg	XX0000100111010	1048
994	DMUL reg reg lit	XX0000110011100	1049
995	DMUL reg reg const	XX0000100110010	1050
996	DFMA reg reg reg reg	XX0111011011010	1051
997	DFMA reg reg lit reg	XX0111001101100	1052
998	DFMA reg reg const reg	XX0111011010010	1053
999	DFMA reg reg reg const	XX0111011001010	1054
1000	IADD reg reg reg	XX0100000111010	1055
1001	IADD reg reg const	XX0100000110010	1056
1002	IADD reg reg lit	XX0100000011100	1057
1003	IADD32I reg reg lit	XX0000000111000	1058
1004	IMNMX reg reg const p	XX0010000110010	1059
1005	IMNMX reg reg reg p	XX0010000111010	1060
1006	IMNMX reg reg lit p	XX0010000011100	1061
1007	ISCADD reg reg reg lit	XX1100000111010	1062
1008	ISCADD reg reg lit lit	XX1100000011100	1063
1009	ISCADD reg reg const lit	XX1100000110010	1064
1010	ISSET reg reg reg p	XX0101011011010	1065
1011	ISSET reg reg const p	XX1101011010010	1066
1012	ISSET reg reg lit p	XX0101001101100	1067
1013	ISSETP p p reg reg p	XX1011011011010	1068
1014	ISSETP p p reg lit p	XX1011001101100	1069
1015	ISSETP p p reg const p	XX1011011010010	1070
1016	ICMP reg reg reg reg	XX0001011011010	1071
1017	ICMP reg reg lit reg	XX1001011101100	1072
1018	ICMP reg reg const reg	XX1001011010010	1073
1019	I2F reg reg	XX1110100111010	1074
1020	I2F reg const	XX1110100110010	1075
1021	I2I reg lit	XX0011110011100	1076
1022	I2I reg reg	XX0011100111010	1077
1023	I2I reg const	XX0011100110010	1078
1024	F2I reg reg	XX0110100111010	1079
1025	F2F reg reg	XX1010100111010	1080
1026	F2F reg const	XX1010100110010	1081
1027	F2F reg lit	XX1010100011100	1082
1028	LOP reg reg lit	XX1110001000011100	1083
1029	LOP p reg reg reg	XX10001110101	1084
1030	LOP reg reg reg	XX1110001000111010	1085
1031	LOP p reg reg const	XX10001100101	1086
1032	LOP reg reg const	XX1110001000110010	1087
1033	LOP p reg reg lit	XX10000111100	1088
1034	LOP32I reg reg lit	XX000000100000	1089
1035	SHL reg reg lit	XX1001000011100	1090
1036	SHL reg reg reg	XX1001000111010	1091
1037	SHR reg reg lit	XX1010000011100	1092
1038	SHR reg reg reg	XX1010000111010	1093
1039	BFE reg reg lit	XX0000000011100	1094
1040	BFI reg reg lit reg	XX0111101101100	1095
1041	SEL reg reg reg p	XX0010100111010	1096
1042	SEL reg reg lit p	XX0010100011100	1097
1043	SEL reg reg const p	XX0010100110010	1098
1044	SSY lit	xxxxx0xx0100101000111	1099
1045			1100

1101	SSY const	xxxxx1xx0100101000111	1156
1102	BRA const	111101xx0001001000111	1157
1103	BRA misc const	xxxxx1xx0001001000111	1158
1104	BRA lit	111100xx0001001000111	1159
1105	BRA misc lit	xxxxx0xx0001001000111	1160
1106	BRX const	111101xx0101001000111	1161
1107	BRX misc const	xxxxx1xx0101001000111	1162
1108	BRX reg lit	111100xx0101001000111	1163
1109	BRX misc reg lit	xxxxx0xx0101001000111	1164
1110	PCNT lit	xxxxx0xx0110101000111	1165
1111	PCNT const	xxxxx1xx0110101000111	1166
1112	CONT	11110xx0101011000111	1167
1113	CONT misc	xx0101011000111	1168
1114	PBK lit	xxxxx0xx0010101000111	1169
1115	PBK const	xxxxx1xx0010101000111	1170
1116	BRK	11110xx0001011000111	1171
1117	BRK misc	xx0001011000111	1172
1118	CAL lit	xxxxx0xx0011001000111	1173
1119	CAL const	xxxxx1xx0011001000111	1174
1120	RET	11110xx0010011000111	1175
1121	RET misc	xx0010011000111	1176
1122	EXIT	11110xx0000011000111	1177
1123	EXIT misc	xx0000011000111	1178
1124	NOP lit	xxxxxxxxx11110xx0110100001010	1179
1125	NOP misc lit	xx0110100001010	1180
1126	NOP	xxxxxxxxx11110xxxxxxxxx0000000000000000xxxxxxxxxxxxxxxxxx0110100001010	1181
1127	NOP misc	xxxxxxxxxxxxxxxxxxxxxxxxxx0000000000000000xxxxxxxxxxxxxxxxxx0110100001010	1182
1128	BAR lit	xxxxxxxxxxxxxxxxxxxxxxxxxx000000000000000000110110000001010100001111	1183
1129	BAR lit lit	xx110110000001010100001111	1184
1130	S2R reg sreg	xx1001100001111	1185
1131	PSETP p p p p p	xx0100100001010	1186
1132	PSET reg p p p	xx1000100001010	1187
1133	FLO reg reg	xx0110000111010	1188
1134	TEX reg reg lit tex lit	xxxxxxxxxxxxxxxxxxxxxxxxxx1111111xxxxxxxxxxxxxxxxxxxxxxxxxx1110000000011	1189
1135	TEX reg reg reg lit tex lit	xx1110000000011	1190
1136	RRO reg reg	xx0100100111010	1191
1137	PRMT reg reg lit reg	xx0001101101100	1192
1138	DMNMX reg reg reg p	xx0101000111010	1193
1139	DMNMX reg reg lit p	xx0101000011100	1194
1140	FMNMX reg reg reg p	xx0011000111010	1195
1141	FMNMX reg reg lit p	xx0011000011100	1196
1142	RED mem reg	xx1111111010111	1197
1143	VOTE reg p p	xx1101100001010	1198
1144	VOTE p p	11111111xx1101100001010	1199
1145	POPC reg reg	xx1000000111010	1200
1146	CSETP p p misc p	xx0010100001010	1201
1147	ISCADD32I reg reg lit lit	xx0xxxxx101000	1202
1148	SHF reg reg lit reg	xx1111101101100	1203
1149	SHF reg reg reg reg	xx11111101101010	1204
1150	FCHK p reg reg	xx1000100111010	1205
1151	JCAL lit	xxxxx0xx010001000111	1206
1152	JCAL const	xxxxx1xx0010001000111	1207
1153	LDG reg mem	xx0101101110111	1208
1154	ATOM reg mem reg reg	xx0111101110111	1209
1155			1210

1211	XMAD reg reg reg reg	XX0000011011010	1266
1212	XMAD reg reg lit reg	XX0010001101100	1267
1213	XMAD reg reg reg const	XX0110010001010	1268
1214	XMAD reg reg const reg	XX0000001110010	1269
1215	SYNC	11110XX1111100001111	1270
1216	SYNC misc	XX1111100001111	1271
1217	STG mem reg	XX1101101110111	1272
1218	IADD3 reg reg reg reg	XX0001100111010	1273
1219	IADD3 reg reg lit reg	XX00011000111100	1274
1220	IADD3 reg reg const reg	XX0001100110010	1275
1221	VABSDIFF reg reg reg reg	XX10010000101010	1276
1222	VABSDIFF reg reg lit reg	XX00010000101010	1277
1223	DEPBAR sb lit bitfield	XXXXXXXXXXXXXXXXXXXXXXXXXXXX1XXXXXXXXXXXXXXXXXXXXXXXXXXXX0111100001111	1278
1224	DEPBAR sb lit	000000XXXXXXXXXXXXXXXXXXXX1XXXXXXXXXXXXXXXXXXXXXXXXXXXX0111100001111	1279
1225	DEPBAR bitfield	XXXXXXXXXXXXXXXXXXXXXXXXXXXX0XXXXXXXXXXXXXXXXXXXXXXXXXXXX0111100001111	1280
1226	DEPBAR	000000XXXXXXXXXXXXXXXXXXXX0XXXXXXXXXXXXXXXXXXXXXXXXXXXX0111100001111	1281
1227	LOP3 reg reg reg reg lit	XX1110011111011010	1282
1228	LOP3 p reg reg reg reg lit	XX1111101101010	1283
1229	LOP3 reg reg const reg lit	XX1000000	1284
1230	LOP3 reg reg lit reg lit	XX111100	1285
1231	TLDS reg reg reg lit tex channel	XXXXXXXXXXXXXXXXXXXX1111111XXXXXXXXXXXXXXXXXXXXXXXXXXXX1011011	1286
1232	TLDS reg reg reg reg lit tex channel	XX1011011	1287
1233	TEXS reg reg reg lit tex channel	XXXXXXXXXXXXXXXXXXXX1111111XXXXXXXXXXXXXXXXXXXXXXXXXXXX0011011	1288
1234	TEXS reg reg reg reg lit tex channel	XX0011011	1289
1235	LEA reg reg reg lit	XX1110101111011010	1290
1236	LEA reg reg reg	XX00000XXXX1110101111011010	1291
1237	LEA p reg reg reg lit	XX10111101101010	1292
1238	LEA p reg reg reg	XX00000XXXXXX10111101101010	1293
1239	LEA reg reg reg reg lit	XX111110111101101010	1294
1240	LEA reg reg reg reg	XX111110111101101010	1295
1241	LEA p reg reg reg reg	XX110111101101101010	1296
1242	LEA p reg reg reg reg lit	XX110111101101101010	1297
1243	LEA reg reg lit	XX11101011011011100	1298
1244	LEA reg reg lit lit	XX11101011011011100	1299
1245	LEA p reg reg lit	XX1011011011100	1300
1246	LEA p reg reg lit lit	XX1011011011100	1301
1247	DSET reg reg reg p	XX100001001101010	1302
1248	DSET reg reg const p	XX000001001001010	1303
1249	DSET reg reg lit p	XX0001001001100	1304
1250			1305
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1265			1320

## Special Registers

In this appendix we list all special registers we have observed. The first column is the encoded value. The second column contains the name of the special register, which nearly always begins with the text "SR\_". In cases where different architectures disagree regarding the name associated with an encoding, we list the older name in the third column.

Not all special registers are available on every GPU architecture. Additionally, the names produced by the disassembler will vary in formatting depending on its version. In particular, capitalization of the letters may differ, and dots may be replaced by underscores.

Encoding	Special Register	Alternate SR
0	SR_LANEID	
1	SR_CLOCK	
2	SR_VIRTCFG	
3	SR_VIRTID	
4	SR_PM0	
5	SR_PM1	
6	SR_PM2	
7	SR_PM3	
8	SR_PM4	
9	SR_PM5	
10	SR_PM6	
11	SR_PM7	
16	SR_PRIM_TYPE	
17	SR_INVOCATION_ID	
18	SR_Y_DIRECTION	
19	SR_THREAD_KILL	
20	SM_SHADER_TYPE	
21	SR_DIRECTCBEWRITEADDRESSLOW	
22	SR_DIRECTCBEWRITEADDRESSHIGH	
23	SR_DIRECTCBEWRITEENABLED	
24	SR_MACHINE_ID_0	
25	SR_MACHINE_ID_1	
26	SR_MACHINE_ID_2	
27	SR_MACHINE_ID_3	
28	SR_AFFINITY	
29	SR_INVOCATION_INFO	
30	SR_WSCALEFACTOR_XY	
31	SR_WSCALEFACTOR_Z	
32	SR_TID	
33	SR_TID.X	
34	SR_TID.Y	
35	SR_TID.Z	
36	SR_CTA_PARAM	
37	SR_CTAID.X	
38	SR_CTAID.Y	
39	SR_CTAID.Z	
40	SR_NTID	
41	SR_CIRQUEUEINCRMINUSONE	SR_NTID.X
42	SR_NLATC	SR_NTID.Y
43	SR_NTID.Z	
44	SR_GRIDPARAM	
45	SR_NCTAID.X	
46	SR_NCTAID.Y	
47	SR_NCTAID.Z	
48	SR_SWINLO	

1431	49	SR_SWINSZ	1486
1432	50	SR_SMEMSZ	1487
1433	51	SR_SMEMBANKS	1488
1434	52	SR_LWINLO	1489
1435	53	SR_LWINSZ	1490
1436	54	SR_LMEMLOSZ	1491
1437	55	SR_LMEMHIOFF	1492
1438	56	SR_EQMASK	1493
1439	57	SR_LTMASK	1494
1440	58	SR_LEMASK	1495
1441	59	SR_GTMASK	1496
1442	60	SR_GEMASK	1497
1443	61	SR_REGALLOC	1498
1444	62	SR_CTXADDR	1499
1445	64	SR_GLOBALERRORSTATUS	1500
1446	66	SR_WARPERRORSTATUS	1501
1447	67	SR_WARPERRORSTATUSCLEAR	1502
1448	72	SR_PM_HI0	1503
1449	73	SR_PM_HI1	1504
1450	74	SR_PM_HI2	1505
1451	75	SR_PM_HI3	1506
1452	76	SR_PM_HI4	1507
1453	77	SR_PM_HI5	1508
1454	78	SR_PM_HI6	1509
1455	79	SR_PM_HI7	1510
1456	80	SR_CLOCKLO	1511
1457	81	SR_CLOCKHI	1512
1458	82	SR_GLOBALTIMERLO	1513
1459	83	SR_GLOBALTIMERHI	1514
1460	96	SR_HWTASKID	1515
1461	97	SR_CIRCULARQUEUEENTRYINDEX	1516
1462	98	SR_CIRCULARQUEUEENTRYADDRESSLOW	1517
1463	99	SR_CIRCULARQUEUEENTRYADDRESSHIGH	1518
1464			1519
1465			1520
1466			1521

## References

- [1] Hou, Y., Lai, J., AND MIKUSHIN, D. Asfermi: An assembler for the nvidia fermi instruction set. URL: <http://code.google.com/p/asfermi/> (accessed: 03.12. 2012) (2011).