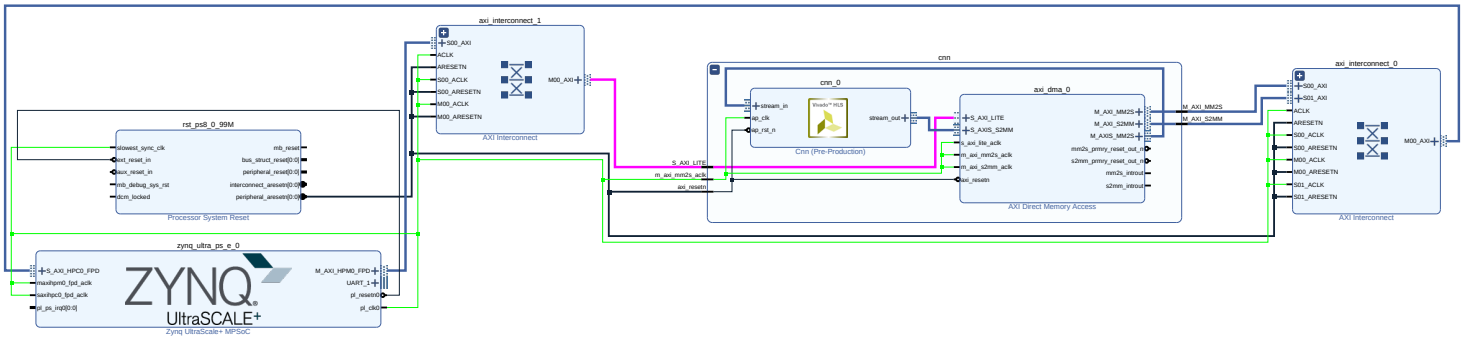
axi_interconnect_1
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
rst_psll_0_99M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
zynq_ultra_ps_e_0
S_AXI_HPC0_FPD
maxihpm0_fpd_aclk
saxihpc0_fpd_aclk
pl_ps_irq[0:0]
M_AXI_HPM0_FPD
UART_1
pl_resetn0
pl_clk0
ZYNQ
UltraSCALE+
Zynq UltraScale+ MPSoC
S_AXI_LITE
m_axi_mm2s_aclk
axi_resetn
cnn
cnn_0
stream_in
ap_clk
ap_rst_n
stream_out
Cnn (Pre-Production)
axi_dma_0
S_AXI_LITE
S_AXIS_S2MM
s_axi_lite_aclk
m_axi_mm2s_aclk
m_axi_s2mm_aclk
axi_resetn
M_AXI_MM2S
M_AXI_S2MM
M_AXIS_MM2S
mm2s_prmry_reset_out_n
s2mm_prmry_reset_out_n
mm2s_introut
s2mm_introut
AXI Direct Memory Access
M_AXI_MM2S
M_AXI_S2MM
axi_interconnect_0
S00_AXI
S01_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
S01_ACLK
S01_ARESETN
M00_AXI
AXI Interconnect