Interconnection of Two Very Weak AC Systems by VSC-HVDC Links Using Power-Synchronization Control

Lidong Zhang, *Member, IEEE*, Lennart Harnefors, *Senior Member, IEEE*, and Hans-Peter Nee, *Senior Member, IEEE*

***Abstract*—In this paper, voltage-source converter (VSC) based high-voltage dc (HVDC) transmission is investigated for interconnection of two very weak ac systems. By using the recently proposed power-synchronization control, the short-circuit capacities of the ac systems are no longer the limiting factors, but rather the load angles. For the analysis of the stability, the Jacobian transfer matrix concept has been introduced. The right-half plane (RHP) transmission zero of the ac Jacobian transfer matrix moves closer to the origin with larger load angles. The paper shows that, due to the bandwidth limitation imposed by the RHP zero on the direct-voltage control of the VSC, high dc-capacitance values are needed for such applications. In addition, the paper proposes a control structure particularly designed for weak-ac-system interconnections. As an example, it is shown that the proposed control structure enables a power transmission of 0.86 p.u. from a system with the short-circuit ratio (SCR) of 1.2 to a system with an SCR of 1.0. This should be compared to previous results for VSC based HVDC using vector current control. In this case, only 0.4 p.u. power transmission can be achieved for dc link where only one of the ac systems has an SCR of 1.0.**

***Index Terms*—Control, converters, HVDC, power systems, stability.**

I. Introduction

LARGE interconnected ac systems have many well-known advantages [1], [2]. However, larger interconnected ac systems also increase the system complexity from the operation point of view, and might adversely decrease the system reliability. Large blackouts in America and Europe confirmed clearly that the close coupling of the neighboring systems might also include the risk of uncontrolled cascading effects in large and heavily loaded systems [3], [4]. High-voltage dc (HVDC) transmission has been introduced since the 1950s [5]. In addition to its unique role in submarine-cable transmission, asynchronous-system connection, etc., HVDC also has the "firewall" function in preventing cascaded ac-system outages spreading from one system to another [6]. By utilizing HVDC links as system interconnector, one can gain the benefits of larger systems, yet keep the operation of each subsystem relatively independent. Therefore, HVDC transmission is generally considered as a promising solution for future large ac-system interconnections [7].

However, there is an inherent weakness with the conventional line-commutated HVDC system, i.e., the commutation of the converter valve is dependent on the stiffness of the alternating voltage supplied by the ac system. The converter cannot work properly if the connected ac system is weak. Substantial research has been performed in this field [8]–[12]. The most outstanding contribution on this subject is [8], which recommends to use short-circuit ratio (SCR) as a description of the strength of the ac system relative to the power rating of the HVDC link. Both [11] and [12] conclude that, for ac systems with an SCR lower than 1.5, synchronous condensers have to be installed to increase the short-circuit capacity of the ac system. However, synchronous condensers can substantially increase the investment and maintenance costs of an HVDC project.

The pulse-width modulation (PWM) based voltage-source converter (VSC) is an emerging technology for HVDC transmission [13], [14]. Thanks to the gradually increased ratings and reduced losses, the technology has reached maturity in recent years. In contrast to the conventional thyristor-based HVDC system, a VSC-HVDC system has the potential to be connected to very weak ac systems, as well as the capability to generate or consume reactive power depending on the operating conditions. With the traditional vector current control, however, the potential of the VSC is not fully utilized [15]–[17], e.g., [16] shows that the maximum power that a VSC-HVDC link using vector current control can transmit to the ac system with $\mathrm{SCR} = 1.0$ is 0.4 p.u. On the other hand, the recently proposed power-synchronization control for grid-connected VSCs has been shown to be a superior solution for VSC-HVDC links connected to very weak ac systems [18], [19]. One of the major features of the power-synchronization control is that the VSC synchronizes with the ac system through an active-power control loop, similar to the operation of a synchronous machine. By using power-synchronization control, the VSC emulates a synchronous machine. Therefore, it basically has no requirement on the short-circuit capacity of the ac system. Moreover, a VSC terminal can give the weak ac system strong voltage support, just like a normal synchronous machine does.

In this paper, VSC-HVDC technology using the recently proposed power-synchronization control is investigated for interconnection of two very weak ac systems. The major focuses of the paper are dynamic modeling and controller design. The paper is organized as follows. In Section II, the definition and characteristics of weak ac systems are discussed and followed

Manuscript received November 19, 2009; revised November 23, 2009. First published May 24, 2010; current version published January 21, 2011. This work was supported by ELFORSK under the Electra program. Paper no. TPWRS-00897-2009.

L. Zhang and L. Harnefors are with ABB Power Systems, SE-771 80 Ludvika, Sweden (e-mail: lidong.zhang@se.abb.com; lennart.harnefors@se.abb.com).

H.-P. Nee is with the School of Electrical Engineering, Royal Institute of Technology, SE-100 44 Stockholm, Sweden (e-mail: hansi@ee.kth.se).

Digital Object Identifier 10.1109/TPWRS.2010.2047875

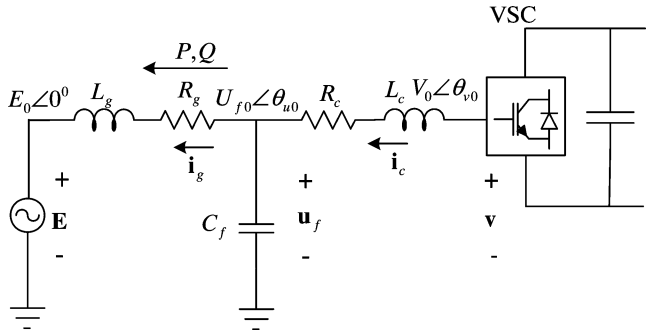

Fig. 1. Main-circuit diagram of a VSC converter connected to ac systems.

by a brief review of the fundamental principle of power-synchronization control for grid-connected VSCs. In Section III, the design of direct-voltage controllers is described and the requirement on dc capacitance for weak-system connections is discussed. Finally, in Section IV, a control structure is proposed for weak-ac-system interconnection. The proposed design and linear model are verified by a VSC-HVDC model in the electromagnetic transient simulation software PSCAD/EMTDC. The simulation software PSCAD/EMTDC is often considered as adequate for controller design in industry. Experiments on converters with power ratings of several MW are very costly and time consuming. Such tests are likely to be performed in the future; however, they are beyond the scope of the present paper.

II. Control of VSC-HVDC Links Connected to Weak AC Systems

Fig. 1 shows the main-circuit diagram of a VSC-HVDC converter connected to an ac system. L_c and R_c are the inductance and resistance of the phase reactor of the VSC, and L_g and R_g are the inductance and resistance of the ac system. C_f is the ac capacitor connected at the point-of-common-coupling (PCC). The bold letter symbols $\mathbf{E}$, $\mathbf{u}_f$, and $\mathbf{v}$ represent the voltage vectors of the ac source, the PCC, and the VSC. E_0, U_{f0}, and V_0 are their corresponding voltage magnitudes. The ac source, which is a stiff constant-frequency voltage source, is used as the voltage reference, and the phase angles of $\mathbf{u}_f$ and $\mathbf{v}$ are θ_{u0} and θ_{v0}, respectively. P and Q are the active power and reactive power from the VSC to the ac system. The quantity $\mathbf{i}_c$ is the current vector of the phase reactor, and $\mathbf{i}_g$ is the current vector to the ac source.

A. Characteristics of Weak AC Systems

A weak ac system is typically characterized by its high impedance [8]. As the ac-system impedance increases, the voltage magnitude of the ac system will become ever more sensitive to power variations of the HVDC system. This difficulty is usually measured by the short-circuit ratio (SCR), which is a ratio of the ac-system short-circuit capacity versus the rated power of the HVDC system. SCR is directly related to the ac-system inductance L_g. According to [8], SCR is defined as

$$\mathrm{SCR} = \frac{S_{\mathrm{ac}}}{P_{dN}} \tag{1}$$

where S_{ac} is the short-circuit capacity of the ac system at the filter bus, while P_{dN} is the rated dc power of the HVDC link. The short-circuit capacity of the ac system S_{ac} can be expressed as

$$S_{\mathrm{ac}} = \frac{U_{f0}^2}{Z} \approx \frac{U_{f0}^2}{\omega_1 L_g} \tag{2}$$

where ω_1 is the angular frequency of the ac system and Z is the equivalent impedance of the ac system. To further simplify the expression of SCR, the filter-bus voltage is assumed to be identical to the base value, i.e., $U_{f0} \approx U_{aN}$, and the rated power of the HVDC link P_{dN} is used as the base power of the ac system, i.e., $S_{aN} = P_{dN}$. If $\omega_1 L_g$ is expressed in per unit (p.u.), it follows from (1) and (2) that SCR can be expressed as $\mathrm{SCR} = 1/(\omega_1 L_g)$.

Besides the voltage-control difficulty, SCR also imposes a theoretical limitation on the maximum power that the HVDC system is able to transmit to or from the ac system. This can be shown by the following well-known power-angle equation:

$$P = \frac{E_0 U_{f0}}{\omega_1 L_g} \sin\theta_{u0} \approx \mathrm{SCR}\, \sin\theta_{u0} \tag{3}$$

where θ_{u0} is defined as the load angle of the VSC-HVDC converter in this paper, and E_0 and U_{f0} are approximately equal to 1 p.u. in normal operating conditions. Equation (3) shows that the maximum load angle cannot be beyond 90° in steady state, e.g., for VSC-HVDC links connected to a system with $\mathrm{SCR} = 1.0$, the maximum theoretical power transmission is $P \approx 1.0$ p.u.

B. Modeling of AC Systems

In a synchronous grid dq reference frame with the d axis chosen aligned with the ac source E, the dynamic equations of the main circuit in Fig. 1 can be written as

$$L_c \frac{d\mathbf{i}_c}{dt} = \mathbf{v} - \mathbf{u}_f - R_c\mathbf{i}_c - j\omega_1 L_c \mathbf{i}_c \tag{4}$$

$$C_f \frac{d\mathbf{u}_f}{dt} = \mathbf{i}_c - \mathbf{i}_g - j\omega_1 C_f \mathbf{u}_f \tag{5}$$

$$L_g \frac{d\mathbf{i}_g}{dt} = \mathbf{u}_f - \mathbf{E} - R_g\mathbf{i}_g - j\omega_1 L_g \mathbf{i}_g \tag{6}$$

and in dq-component form

$$\begin{aligned}
L_c \frac{di_{cd}}{dt} &= v_d - u_{fd} - R_c i_{cd} + \omega_1 L_c i_{cq} \\
L_c \frac{di_{cq}}{dt} &= v_q - u_{fq} - R_c i_{cq} - \omega_1 L_c i_{cd} \\
C_f \frac{du_{fd}}{dt} &= i_{cd} - i_{gd} + \omega_1 C_f u_{fq} \\
C_f \frac{du_{fq}}{dt} &= i_{cq} - i_{gq} - \omega_1 C_f u_{fd} \\
L_g \frac{di_{gd}}{dt} &= u_{fd} - E_0 - R_g i_{gd} + \omega_1 L_g i_{gq} \\
L_g \frac{di_{gq}}{dt} &= u_{fq} - R_g i_{gq} - \omega_1 L_g i_{gd}.
\end{aligned} \tag{7}$$

For power-synchronization control, the active power and alternating voltage are controlled by the phase angle θ_v and voltage magnitude V of the VSC output. Thus, the real and imaginary parts of the VSC vector v_d and v_q can be expressed as

$$v_d = V\cos\theta_v, \quad v_q = V\sin\theta_v. \tag{8}$$

The output variables are the active power P and the voltage magnitude U_f at the PCC, which are expressed as

$$P = \mathrm{Re}\left\{\mathbf{u}_f \mathbf{i}_g^*\right\}, \quad U_f = \sqrt{U_{fd}^2 + U_{fq}^2}. \tag{9}$$

The state-space model can be obtained by linearizing (6), (8), and (9), which yields the following form:

$$\frac{d}{dt}\mathbf{x} = A\mathbf{x} + B\mathbf{u}, \quad \mathbf{y} = C\mathbf{x} + D\mathbf{u} \tag{10}$$

where

$$\begin{aligned} \mathbf{u} &= \left[\Delta\theta_v \quad \tfrac{\Delta V}{V_0}\right]^T, \quad \mathbf{y} = \left[\Delta P \quad \Delta U_f\right]^T \\ \mathbf{x} &= \left[\Delta i_{cd} \quad \Delta i_{cq} \quad \Delta u_{fd} \quad \Delta u_{fq} \quad \Delta i_{gd} \quad \Delta i_{gq}\right]^T. \end{aligned} \tag{11}$$

The state-space representation (10) can also be written in input-output transfer matrix form

$$\mathbf{y} = \left[C\left(sI - A\right)^{-1} B + D\right]\mathbf{u} \tag{12}$$

which yields

$$\begin{bmatrix} \Delta P \\ \Delta U_f \end{bmatrix} = \underbrace{\begin{bmatrix} J_{\mathrm{P}\theta}(s) & J_{\mathrm{PV}}(s) \\ J_{\mathrm{U}_f\theta}(s) & J_{\mathrm{U}_f V}(s) \end{bmatrix}}_{\mathbf{J}} \begin{bmatrix} \Delta\theta_v \\ \frac{\Delta V}{V_0} \end{bmatrix}. \tag{13}$$

If the resistance R_g and R_c are neglected, the poles of $\mathbf{J}(s)$, i.e., the eigenvalues of the A matrix, can be solved analytically with the expressions

$$\begin{aligned} p_{1,2} &= \pm j\omega_1, \quad p_{3,4} = \pm j\left(\sqrt{\frac{1}{L_g C_f} + \frac{1}{L_c C_f}} - \omega_1\right) \\ p_{5,6} &= \pm j\left(\sqrt{\frac{1}{L_g C_f} + \frac{1}{L_c C_f}} + \omega_1\right). \end{aligned} \tag{14}$$

The poles of $\mathbf{J}(s)$ are independent of the operating points, but are usually very poorly damped due to the low resistance in transmission systems. $\mathbf{J}(s)$ contains a pair of transmission zeros. If the resistances R_g and R_c are neglected, the zeros are given by

$$z_{1,2} = \pm\omega_1\sqrt{\frac{E_0\cos\theta_{u0}}{U_{f0} - E_0\cos\theta_{u0}}} \approx \pm\omega_1\sqrt{\frac{\cos\theta_{u0}}{1 - \cos\theta_{u0}}}. \tag{15}$$

In contrast to the poles, the transmission zeros of $\mathbf{J}(s)$ are very much dependent on the operating points, mainly on the load angle θ_{u0} [18]. The higher the load angle, the closer the zeros are to the origin. In control theory, a zero on the right-half plane (RHP) of the process imposes a fundamental limitation on the achievable bandwidth of the closed-loop system [20], i.e., the closed-loop system cannot achieve higher bandwidth than the location of the RHP zero. It is interesting to note that (15) is consistent with the conclusion drawn from the steady-state relationship in (3) but with more dynamic insight. With a load angle $\theta_{u0} = 90°$, the zeros of $\mathbf{J}(s)$ move to the origin. From feedback-control point of view, such a process cannot be tightly controlled at low frequencies.

Due to the similarity with the Jacobian matrix in load-flow studies in terms of inputs and outputs [21], $\mathbf{J}(s)$ is named Jacobian transfer matrix in this paper. The concept of Jacobian transfer matrix can be used to represent larger ac systems with more input devices to study the interactions, especially if the electromagnetic transients are considered.

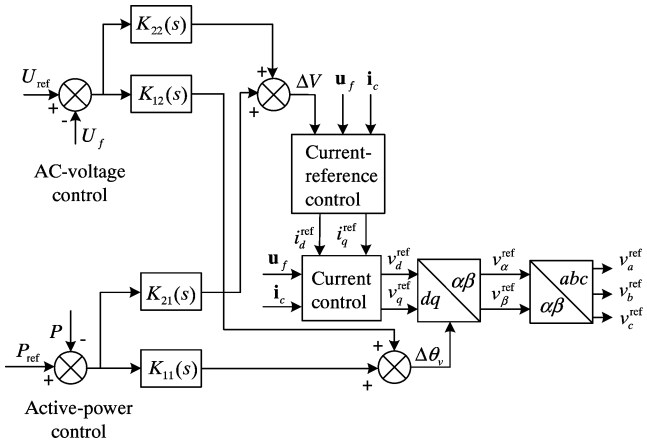

Fig. 2. Power-synchronization control of grid-connected VSCs.

C. Power-Synchronization Control of Grid-Connected VSCs

The fundamental idea of power-synchronization control of grid-connected VSCs is that VSCs synchronize with the ac systems through the active-power control instead of using a phase-locked loop (PLL), similar to the operation of a synchronous machine [18]. Fig. 2 shows the control overview of power-synchronization control. The active power and the alternating voltage are controlled by the phase angle and the magnitude of the VSC through a multivariable controller [19]

$$K(s) = \begin{bmatrix} K_{11}(s) & K_{12}(s) \\ K_{21}(s) & K_{22}(s) \end{bmatrix}. \tag{16}$$

In Fig. 2, the "Current control" block is a standard proportional-type vector current controller with the expression

$$\mathbf{v}_{\mathrm{ref}}^c = \alpha_c L_c\left(\mathbf{i}_{\mathrm{ref}} - \mathbf{i}_c^c\right) + j\omega_1 L_c \mathbf{i}_c^c + \mathbf{u}_f^c \tag{17}$$

where α_c is the desired closed-loop bandwidth of the inner-current controller, $\mathbf{i}_{\mathrm{ref}}$ is the converter current reference, and $\mathbf{v}_{\mathrm{ref}}^c$ is the voltage reference of the VSC. The superscript c denotes the converter dq frame, which leads the grid dq frame with the phase angle θ_v. With power-synchronization control, instead of giving a constant current reference to (17), the value of $\mathbf{i}_{\mathrm{ref}}$ in (17) is given by

$$\mathbf{i}_{\mathrm{ref}} = \frac{1}{\alpha_c L_c}\left[\left(V_0 + \Delta V\right) - H_{\mathrm{HP}}(s)\,\mathbf{i}_c^c - \mathbf{u}_f^c - j\omega_1 L_c \mathbf{i}_c^c\right] + \mathbf{i}_c^c \tag{18}$$

where V_0 is a nominal value, e.g., $V_0 = 1.0$ p.u. Equation (18) corresponds to the "Current reference control" in Fig. 2. The current reference in (18) is designed in such a way that the control law in (17) becomes

$$\mathbf{v}_{\mathrm{ref}}^c = \left(V_0 + \Delta V\right) - H_{\mathrm{HP}}(s)\,\mathbf{i}_c^c \tag{19}$$

in normal operation. This can be easily verified by substituting (18) into (17). However, the current reference $\mathbf{i}_{\mathrm{ref}}$ in (18) gives an indication of the actual converter current. During ac system faults, current limitation is automatically achieved by limiting

the modulus of $\mathbf{i}_{\rm ref}$ to the maximum current limit $I_{\max}$. A detailed analysis of this has been given in [18]. The output variables $v_a^{\rm ref}$, $v_b^{\rm ref}$, and $v_c^{\rm ref}$ are the three-phase reference voltages of the VSC for pulsewidth modulation. An important part of the power-synchronization control structure is the high-pass current controller $H_{\rm HP}(s)$ in (19). As mentioned in Section II-B, the resonant (complex) poles of $\mathbf{J}(s)$ are usually poorly damped, which requires the control system of the VSC to provide additional damping. This is especially important for VSC-HVDC links connected to weak ac systems, where the resonance frequency tends to be lower. Therefore, a high-pass current control was proposed in [18] to add "active damping" to the resonant poles. The high-pass current controller has the transfer function

$$H_{\rm HP}(s) = \frac{k_v s}{\alpha_v + s} \tag{20}$$

where α_v should be chosen to cover the frequency range of all the possible resonances in ac systems, typically $\alpha_v < 30 - 50$ rad/s to also cover the subsynchronous resonance in ac systems. The gain k_v determines the level of damping as shown below. With the $H_{\rm HP}(s)$ control function applied, if the switching-time delay of the converter is neglected and it is assumed that $|\mathbf{v}_{\rm ref}^c|$ does not exceed the maximum voltage modulus, then $\mathbf{v} = \mathbf{v}_{\rm ref}^c e^{j\theta_v}$. The dynamic equation in (4) should be expressed as

$$L_c\frac{d\mathbf{i_c}}{dt} = (V_0 + \Delta V)e^{j\theta_v} - H_{\rm HP}(s)\mathbf{i}_c - \mathbf{u}_f - R_c\mathbf{i}_c - j\omega_1 L_c\mathbf{i}_c. \tag{21}$$

To fit (21) in state-space form, a new state variable ρ_c is introduced. Consequently, (21) is expressed as

$$\begin{aligned} L_c\frac{d\mathbf{i_c}}{dt} &= L_c\rho_c + (V_0 + \Delta V)e^{j\theta_v} \\ &\quad - (R_c + k_v + \alpha_v L_c)\,\mathbf{i}_c - \mathbf{u}_f - j\omega_1 L_c\mathbf{i}_c \\ L_c\frac{d\rho_c}{dt} &= \alpha_v\Big((V_0 + \Delta V)e^{j\theta_v} - R_c\mathbf{i}_c \\ &\quad - \mathbf{u}_f - j\omega_1 L_c\mathbf{i}_c\Big). \end{aligned} \tag{22}$$

Replacing the phase-reactor dynamic equations in (4) by (22) and following the same procedure as in Section II-B, the transfer matrix $\mathbf{J}(s)$ including $H_{\rm HP}(s)$ can be obtained. By varying k_v, Fig. 3 shows the effect of $H_{\rm HP}(s)$ which shifts the resonant poles of $\mathbf{J}(s)$ towards the left-half plane (LHP) without affecting the locations of the two transmission zeros.

Power-synchronization control is fundamentally of multi-input multi-output nature, i.e., both the active power and the alternating voltage are controlled by the phase angle and voltage magnitude of the VSC. In this paper, the multivariable internal model controller (IMC) designed in [19] is applied.

VSCs using power-synchronization control basically emulate the operation of a synchronous machine. Therefore, it contributes short-circuit capacity to the ac system at the PCC. In order to obtain a simple estimate of the impact of the VSC on the short-circuit capacity of ac system, the effects of the alternating-voltage control and the ac filter can be disregarded.

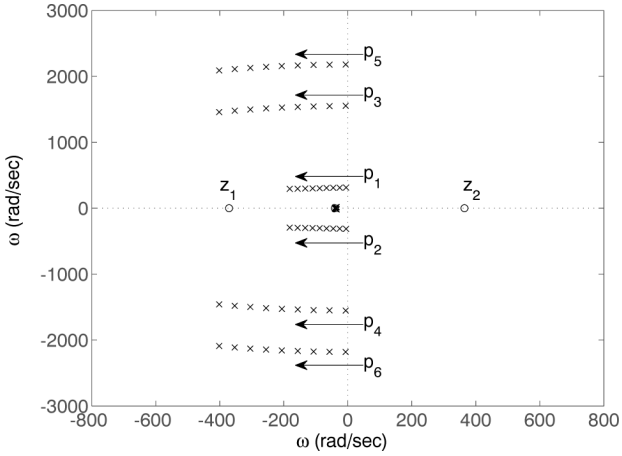

Fig. 3. Damping effect of $H_{\rm HP}(s)$ on the resonant poles of the ac system represented by $\mathbf{J}(s)$ ("x": pole, "o": zero). Main circuit parameters: $\omega_1 L_g = 1.0$ p.u., $R_g = 0.01$ p.u., $\omega_1 L_c = 0.2$ p.u., $R_c = 0.01$ p.u., $\omega_1 C_f = 0.17$ p.u.. Initial conditions: $V_0 = 1.05$ p.u., $E_0 = 1.0$ p.u., $\theta_{u0} = 60°$. $H_{\rm HP}(s)$: $\alpha_v = 40$ rad/s, k_v from 0.0 to 0.6.

Doing so, the short-circuit capacity of the ac system including the VSC at the PCC can be expressed as

$$S_{\rm ac} = \frac{U_{f0}^2(L_g + L_c)}{\omega_1 L_g L_c} \tag{23}$$

where the resistances R_g and R_c have also been neglected. However, VSCs do not necessarily increase short-circuit currents to the ac system during ac system faults thanks to the current limitation function [18].

III. Direct-Voltage Control

For a VSC-HVDC link, at least one of the converter stations has to control the direct voltage, while the other converter station controls the active power. The active power is thus automatically balanced between the two converter stations. In this section, the various aspects of the direct-voltage control are discussed.

A. Modeling of DC Systems

Fig. 4(a) shows a dc-link circuit that is simplified as one dc capacitor. Such a representation is applicable for dc cable transmission or back-to-back HVDC links. The capacitor bank at the dc link is an energy storage. The time derivative of the stored energy must equal the sum of the instantaneous power infeed from the two converters (neglecting the losses). The direct-voltage dynamics can thus be written as

$$\frac{1}{2}C_d\frac{d\left(u_d^2\right)}{dt} = P_{d1} + P_{d2} \tag{24}$$

where C_d is dc-link capacitance and u_d is the direct voltage. P_{d1} and P_{d2} are the instantaneous power from Converter 1 and Converter 2. If the direct-voltage controller were to operate directly on the error $u_d^{\rm ref} - u_d$, the closed-loop dynamics would be dependent on the operating point U_{d0}. This inconvenience is avoided by selecting the direct-voltage controller operating

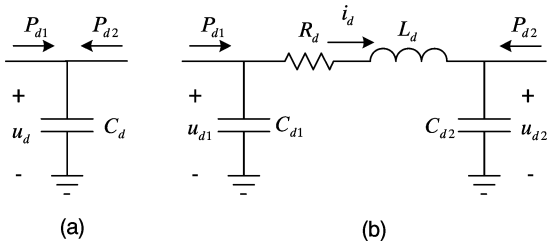

Fig. 4. DC-link representation of the VSC-HVDC system. (a) dc capacitor (b)π-link.

instead on the error $\left(u_d^{\text{ref}}\right)^2 - u_d^2$ as suggested in [22]. Consequently, the dc-link dynamics can be written in the linearized form

$$\Delta u_d^2 = \frac{2}{sC_d}\left(\Delta P_{d1} + \Delta P_{d2}\right). \tag{25}$$

If the dc transmission line is a long overhead line, then the resistance and inductance of the line have to be taken into account. Fig. 4(b) shows a π-link model of the dc circuit. Based on Kirchhoff's voltage and current laws, the dynamic equations of the dc circuit can be written as

$$\begin{aligned} C_{d1}\frac{du_{d1}}{dt} &= \frac{P_{d1}}{u_{d1}} - i_d \\ L_d\frac{di_d}{dt} &= u_{d1} - u_{d2} - R_d i_d \\ C_{d2}\frac{du_{d2}}{dt} &= i_d + \frac{P_{d2}}{u_{d2}} \end{aligned} \tag{26}$$

where C_{d1} and C_{d2} are the lumped capacitances representing the capacitance and the dc capacitors at the two converter stations, and u_{d1} and u_{d2} represent the direct voltages at two converter stations. R_d and L_d are the resistance and inductance of the dc line. If the linearized deviation variables ΔP_{d1} and ΔP_{d2} of P_{d1} and P_{d2} are chosen as the inputs, and Δu_{d1}^2 and Δu_{d2}^2 of u_{d1} and u_{d2} are chosen as the outputs, a state-space model can be obtained by linearization of (26)

$$\frac{d}{dt}\mathbf{x} = A\mathbf{x} + B\mathbf{u}, \quad \mathbf{y} = C\mathbf{x} + D\mathbf{u} \tag{27}$$

where

$$\begin{aligned} A &= \begin{bmatrix} -\frac{P_{d10}}{u_{d10}^2 C_{d1}} & -\frac{1}{C_{d1}} & 0 \\ \frac{1}{L_d} & -\frac{R_d}{L_d} & -\frac{1}{L_d} \\ 0 & \frac{1}{C_{d2}} & -\frac{P_{d20}}{u_{d20}^2 C_{d2}} \end{bmatrix} \\ B &= \begin{bmatrix} \frac{1}{u_{d10}C_{d1}} & 0 & 0 \\ 0 & 0 & \frac{1}{u_{d20}C_{d2}} \end{bmatrix}^T \\ C &= \begin{bmatrix} 2u_{d10} & 0 & 0 \\ 0 & 0 & 2u_{d20} \end{bmatrix}, \quad D = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \\ \mathbf{x} &= \begin{bmatrix} \Delta u_{d1} & \Delta i_d & \Delta u_{d2} \end{bmatrix}^T \\ \mathbf{u} &= \begin{bmatrix} \Delta P_{d1} & \Delta P_{d2} \end{bmatrix}^T, \quad \mathbf{y} = \begin{bmatrix} \Delta u_{d1}^2 & \Delta u_{d2}^2 \end{bmatrix}^T. \end{aligned} \tag{28}$$

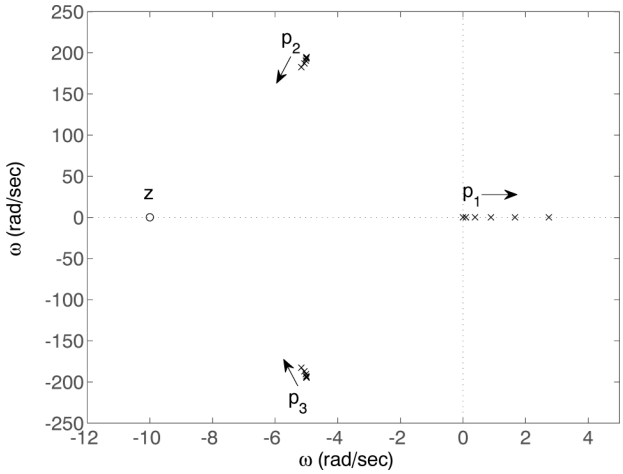

Fig. 5. Root-loci of $\mathbf{G}_d(s)$ regarding operating-point variations ("x": pole, "o": zero). DC-link parameters: $L_d = 0.0035$ p.u., $R_d = 0.035$ p.u., $C_{d1} = 0.015$ p.u., $C_{d2} = 0.015$ p.u.. Initial conditions: $u_{d10} = 1.0$ p.u., variation of P_{d10} from 0.0 p.u. to 1.0 p.u.

The subscript 0 in (28) denotes the operating-point value. The state-space representation (27) can also be written in input-output transfer matrix form by applying (12), yielding

$$\begin{bmatrix} \Delta u_{d1}^2 \\ \Delta u_{d2}^2 \end{bmatrix} = \underbrace{\begin{bmatrix} G_{d11}(s) & G_{d12}(s) \\ G_{d21}(s) & G_{d22}(s) \end{bmatrix}}_{\mathbf{G}_d(s)} \begin{bmatrix} \Delta P_{d1} \\ \Delta P_{d2} \end{bmatrix}. \tag{29}$$

The poles of $\mathbf{G}_d(s)$ are the eigenvalues of the A matrix, which can be solved analytically for the operating point where $P_{d10} = P_{d20} = 0$ with the expression

$$p_1 = 0, \quad p_{2,3} = -\frac{R_d}{2L_d} \pm j\sqrt{\frac{R_d^2}{4L_d^2} - \frac{C_{d1} + C_{d2}}{L_d C_{d1} C_{d2}}}. \tag{30}$$

As shown in Fig. 5, the poles of $\mathbf{G}_d(s)$ are dependent on the operating point. With the increase of the loading, the frequencies of the two complex poles $p_{2,3}$ are reduced, and the real pole p_1 at the origin moves into the right-half plane. In control theory, the RHP pole of the process imposes a fundamental lower limit on the bandwidth of the controller, i.e., the closed-loop system of the direct-voltage control has to achieve a bandwidth that is higher than the location of the RHP pole of $\mathbf{G}_d(s)$ to stabilize the process. Recalling the upper limit imposed by the RHP zero of $\mathbf{J}(s)$ on the bandwidth of the power-synchronization controller in Section II-B, it is generally more complicated to operate VSC-HVDC links at high load angles.

The instability of $\mathbf{G}_d(s)$ has to do with the resistance of the dc link. With dc powers as the inputs, as the way how VSCs work to a dc link, the dc resistance gives a destabilizing effect. Of course, such destabilizing effects only become apparent if the dc resistance is large enough, e.g., long-distance HVDC transmissions. The analytical solutions of the poles of $\mathbf{G}_d(s)$ with other operating point than $P_{d10} = P_{d20} = 0$ are difficult to obtain. However, Appendix B gives a rigorous mathematical proof of the instability of $\mathbf{G}_d(s)$ for other operating points than $P_{d10} = 0$

or $P_{d20} = 0$. The mathematical proof also shows the role of the dc resistance to the instability of $\mathbf{G}_d(s)$.

The expression for the transmission zero of $\mathbf{G}_d(s)$ is surprisingly simple, i.e., $z = -R_d/L_d$. The location of the zero is independent of the operating points. This implies that the dc system is always a minimum-phase system. Due to the similarity with the ac Jacobian transfer matrix $\mathbf{J}(s)$ in Section II-B, the transfer matrix $\mathbf{G}_d(s)$ may be conveniently named dc Jacobian transfer matrix. Similar to the concept of ac Jacobian transfer matrix for ac systems, the concept of dc Jacobian transfer matrix can also be used to represent larger dc systems with several or many VSC terminals.

B. Direct-Voltage Controller Design

The connection between the ac Jacobian transfer matrix $\mathbf{J}(s)$ and dc Jacobian transfer matrix $\mathbf{G}_d(s)$ is the equivalence between the instantaneous power P_a at the ac side and that at the dc side P_d of the VSC

$$\Delta P_a = -\Delta P_d \tag{31}$$

i.e., the output of the ac Jacobian transfer matrix becomes the input of the dc Jacobian transfer matrix, and the minus sign in (31) is due to the definition of the power direction. However, a direct connection of the two matrices may introduce an error, since the active power derived in (9) is the power from the PCC to the ac system, which is somewhat different from the active power flowing through the VSC due to the energy stored in the phase reactor. Therefore, the ac power ΔP_a should be obtained from the linearization of $P_a = P_{\rm VSC} = \mathrm{Re}\{\mathbf{vi}_c^*\}$. In Section IV, the active power from the VSC is named $P_{\rm VSC}$ to distinguish from the active power from the PCC into the grid.

Another possible error is that (31) does not consider the losses in the VSC. Experiment tests show that this error might have an impact if dc resonance is a concern. The losses of the VSC are of nonlinear nature and shall not be simply represented by a constant resistor. This issue certainly needs to be addressed in future research.

For the direct-voltage controller, a proportional-integral (PI) controller is proposed with the control law

$$P_{\rm ref} = \underbrace{-\left(K_{pd} + \frac{K_{id}}{s}\right)}_{F_{\rm dc}(s)} \left[\left(u_d^{\rm ref}\right)^2 - u_d^2\right]. \tag{32}$$

If the power-synchronization controller is assumed to be sufficiently fast, i.e., $P_{\rm ref} = P_{\rm VSC}$, and the dc link is assumed to be a pure capacitor, i.e., $\mathbf{G}_d(s) = 2/sC_d$, then the closed-loop system is expressed as

$$u_d^2 = \frac{2(K_{pd}s + K_{id})}{s^2 C_d + 2K_{pd}s + 2K_{id}} (u_d^{\rm ref})^2. \tag{33}$$

The control parameters are selected as

$$K_{pd} = \alpha_d C_d \text{ and } K_{id} = \frac{\alpha_d^2 C_d}{2} \tag{34}$$

which place two real poles of the closed-loop system at $s = -\alpha_d$. For long overhead lines, the dc-line inductance and the dc capacitance may create resonance peak in the low-frequency range. If the resonance peak appears in the bandwidth where the direct-voltage controller is active, an effective way to mitigate the dc resonance is to apply a notch filter in the direct-voltage control loop. A notch filter commonly has the expression

$$F_n(s) = \frac{s^2 + 2\xi_1\omega_n s + \omega_n^2}{s^2 + 2\xi_2\omega_n s + \omega_n^2} \tag{35}$$

where the three adjustable parameters are ξ_1, ξ_2, and ω_n. The ratio of ξ_2/ξ_1 sets the depth of the notch, and ω_n is the resonance frequency. Fig. 6 shows the effect of the notch filter by time step response with 0.1 p.u. change of the direct-voltage reference. It should be noted that the notch filter may adversely affect the phase margin of direct-voltage control.

The block diagram of the direct-voltage controller is shown in Fig. 7. A prefilter $K_r(s)$ is added on the reference to remove the overshooting with reference tracking [20]. The multivariable power-synchronization controller is used as an inner loop.

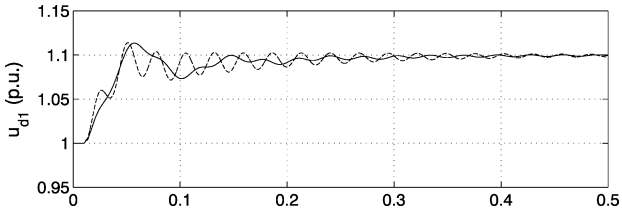

Fig. 6. Notch filter to reduce the dc resonance peak (dashed: without notch filter, solid: with notch filter). DC-link parameters: the same as Fig. 5. Initial conditions: $u_{d10} = 1.0$ p.u., $P_{d10} = 1.0$ p.u. Direct-voltage controller: $\alpha_d = 40$ rad/s. Notch filter: $\omega_n = 194$ rad/s, $\xi_1 = 0.2$, $\xi_2 = 0.8$.

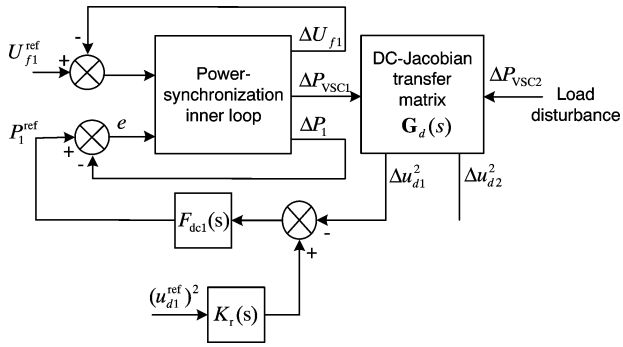

Fig. 7. Control block diagram of direct-voltage controller.

C. DC-Capacitance Requirements

In Section III-B, it has been shown that, by explicitly including the dc capacitance in the direct-voltage control parameters, one can freely place the poles of the closed-loop system. This implies that, as long as its size is known, the dc-capacitance does not affect the linear (small signal) stability of the direct-voltage control. However, for disturbance reduction, the dc capacitance has an important role. In this section, the dc-capacitance requirement for weak-system connections is discussed. To simplify the analysis, the dc-link representation shown in Fig. 4(a) is assumed, i.e., $\mathbf{G}_d(s) = 2/sC_d$ [cf. (25)]. If the power-synchronization loop has the bandwidth which is considerable higher than that of the direct-voltage controller, the

transfer function from the load disturbance to the error signal e as shown in Fig. 7 becomes

$$G_{pe}(s) = \frac{\frac{2}{sC_{dc}}}{1+\alpha_d C_{dc}\left(\frac{\frac{s+\alpha_d}{2}}{s}\right)\frac{2}{sC_{dc}}} = \frac{2s}{C_{dc}(s+\alpha_d)^2}. \quad (36)$$

If the worst scenario is considered, i.e., the active power output to the other converter station is changed stepwise from the maximum active power P_m to 0, e.g., the converter is suddenly blocked. The step response of the error signal $e_d(t)$ in the time domain becomes

$$\begin{aligned} e_d(t) &= \mathcal{L}^{-1}\left\{G_{pe}(s)\frac{P_m}{s}\right\} \\ &= \mathcal{L}^{-1}\left\{\frac{2P_m}{C_d(s+\alpha_d)^2}\right\} = \frac{2P_m}{C_d}te^{-(\alpha_d/t)}. \end{aligned} \quad (37)$$

The time derivative of $e_d(t)$ is

$$\frac{de_d}{dt} = \frac{2P_m}{C_d}(1-\alpha_d t)e^{-\alpha_d t}. \quad (38)$$

The time derivative of $e_d(t)$ becomes zero at $t = 1/\alpha_d$, which corresponds to the peak of the voltage error. By substituting this into (37), the maximum error is found to be $e_{d,\max} = 2P_m e^{-1}/(\alpha_d C_d)$. By considering $u_{d,\max}$ the maximum direct-voltage allowed, then $e_{d,\max} = u_{d,\max}^2 - \left(u_d^{\text{ref}}\right)^2$, the required dc capacitance is

$$C_d > \frac{2P_m e^{-1}}{\left(u_{d,\max}^2 - \left(u_d^{\text{ref}}\right)^2\right)\alpha_d}. \quad (39)$$

A common expression for dc capacitance is using its time constant T_d, which is defined as

$$T_d = \frac{C_{d0}U_{dN}^2}{2P_{dN}} = \frac{C_d}{2} \quad (40)$$

where U_{dN} is the direct-voltage base value (kV) and P_{dN} is the rated (base) power (MW) of the VSC, and C_{d0} is the dc capacitance (μF). Substituting (40) into (39) yields

$$T_d > \frac{P_m e^{-1}}{\left(u_{d,\max}^2 - \left(u_d^{\text{ref}}\right)^2\right)\alpha_d}. \quad (41)$$

It should be noted that, for the dc-capacitance requirement, only per unit values of the direct voltage and the dc power are applicable for (41), while either per unit values or real values can be applied in (39). As mentioned in Section II-A, for weak-system connections, the VSC-HVDC link needs to operate with large load angles, where the RHP transmission zero of the ac Jacobian transfer matrix $\mathbf{J}(s)$ moves closer to the origin. The RHP zero limits the bandwidth of the power-synchronization controller, and eventually limits the bandwidth of the direct-voltage controller. A rule of thumb is that the bandwidth of the power-synchronization controller should be lower than half of the location of the RHP zero [20]. If it is further assumed that the direct-voltage controller is four times slower than the power-synchronization loop, then α_d can be solved by (15) and (3). Accordingly

$$\alpha_d < \frac{1}{8}\omega_1\sqrt{\frac{\cos\theta_{u0}}{1-\cos\theta_{u0}}} = \frac{1}{8}\omega_1\sqrt{\frac{\sqrt{1-\left(\frac{P_m}{\text{SCR}}\right)^2}}{1-\sqrt{1-\left(\frac{P_m}{\text{SCR}}\right)^2}}}. \quad (42)$$

Another issue that needs to be taken into account is that, if the bandwidth of the direct-voltage controller is chosen four times slower than the power-synchronization loop, the inner loop will affect the maximum voltage variation. Fig. 8 shows the ratio of bandwidth reduction by the inner loop, which is approximated by a first-order filter with bandwidth α_p. Considering this effect, (41) is adjusted as

$$T_d > \frac{1.3P_m e^{-1}}{\left(u_{d,\max}^2 - \left(u_d^{\text{ref}}\right)^2\right)\alpha_d}. \quad (43)$$

Given the maximum loading P_m and maximum allowed direct voltage $u_{d,\max}$, the relationship between dc-capacitance requirement and SCR of the ac system can be established by (42) and (43). If the worst scenario is considered, the maximum loading should be chosen as $P_m = 1.0$ p.u. However, with very weak-ac-system connection, it is recommended that the load angle shall not be above 60° to maintain a reasonable stability margin. For instance, if the SCR of the ac system is 1.0, then the maximum loading is $P_m = \text{SCR}\,\sin\theta = 0.86$ p.u.. Fig. 9 shows the plots of dc-capacitance requirement for ac systems having $\text{SCR} \le 2.0$ with different allowed $u_{d,\max}$.

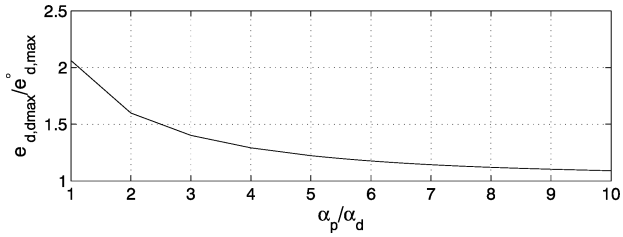

Fig. 8. Direct-voltage control bandwidth reduced by the inner loop.

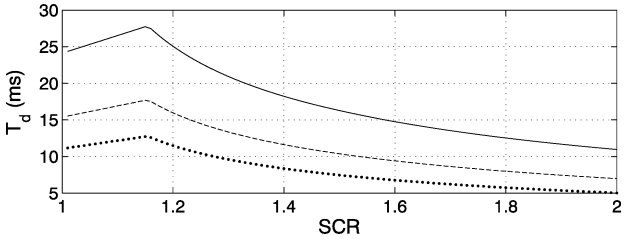

Fig. 9. DC-capacitance requirement in weak-ac-system connection with $u_d^{\text{ref}} = 1.0$ p.u. (solid: $u_{d,\max} = 1.2$ p.u., dashed: $u_{d,\max} = 1.3$ p.u., dotted: $u_{d,\max} = 1.4$ p.u.).

IV. Interconnection of Two Very Weak AC Systems

This section shows a design example. A 350-MW VSC-HVDC link is applied to interconnect two very weak ac systems, where the inverter station (station 1, power receiving end) connected to an ac system having $\text{SCR}_1 = 1.0$, while the rectifier station (station 2, power sending end) connected to an ac system having $\text{SCR}_2 = 1.2$. Since the VSC-HVDC systems have mostly been applied with cable transmissions, the dc link

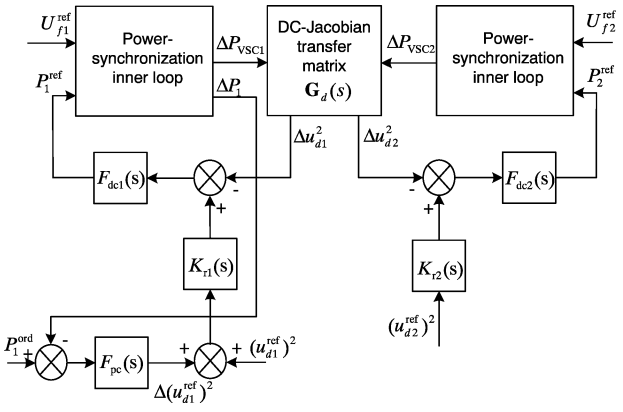

Fig. 10. Control block diagram of a VSC-HVDC link interconnecting two weak ac systems.

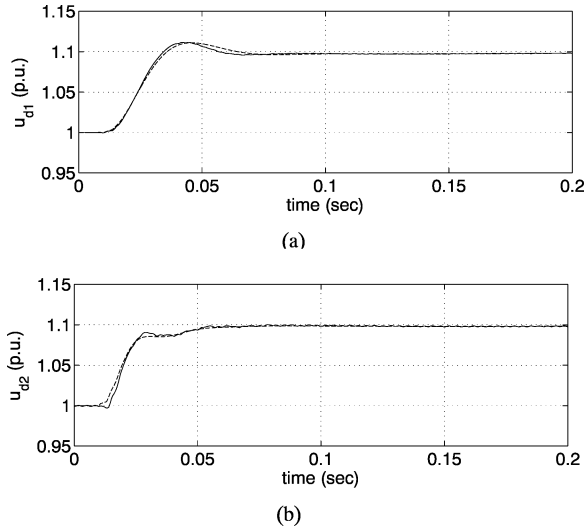

Fig. 11. Step response of the direct-voltage controllers. (a) Direct-voltage step at station 1. (b) Direct-voltage step at station 2 (solid: nonlinear simulation, dashed: linear model).

is supposed to be represented by the single dc-capacitor model shown in Fig. 4(a). The detailed parameters of the converter stations are listed in Appendix A.

From Fig. 7, it can be easily observed that, if one converter station controls the direct voltage, while the other converter station controls the active power, the two converter stations are, in fact, linearly independent. This implies that the stability of one converter station does not affect the stability of the other converter station. One might consequently conclude that there is nothing more special for a VSC-HVDC link connected to two weak systems than it is only connected to one weak system. This might be true if only linear effects are considered. However, the real system is nonlinear. For VSC-HVDC operation, the direct voltage has to be carefully maintained around its nominal value. For instance, a big direct-voltage drop might temporarily limit the capability of the alternating-voltage controller and negatively affect the linear stability of the control systems.

The proposed control structure for weak-system interconnection is shown in Fig. 10. The basic idea of the design is that both of the two converter stations have direct-voltage controllers, while the active-power controlling station controls the active power by adding an additional contribution to the reference of the direct-voltage controller, and its output shall be limited. This may seem unnecessarily complicated since two cascaded control layers have been applied. However, the proposed scheme has shown to be superior to other solutions since it gives the highest priority to direct-voltage control, which is very important for weak ac system interconnection. Once the direct voltage comes out of bounds, the nonlinear phenomena will create substantial difficulties for the control system. With the proposed control structure, the linear independence between the two converter stations is lost. However, the bandwidth of the direct-voltage controllers is much higher than the bandwidth of the ac system dynamics. This implies that the "firewall" effect of the HVDC link is still in force.

A. Power-Synchronization Inner Loop

Due to the very low SCR of the ac system connected to the converter station 1, the maximum allowed power is $P_{m1} = 0.86$ p.u., which corresponds to approximately $\theta_{u10} = 60^\circ$ load angle. The ac system connected to the converter station 2 has slightly higher SCR, but considering the losses of the converter station and of the dc cable, it has maximum loading $P_{m2} = -0.91$ p.u., which corresponds approximately to load angle of $\theta_{u20} = -50^\circ$.

The power-synchronization controller is used as the inner loop for the direct-voltage controller as shown in Fig. 7. In this application, the multivariable internal model control (IMC) investigated in [19] is applied to parameterize the power-synchronization controller. According to the discussion in Section II-B, the bandwidth of the power-synchronization controller should be lower than half of the RHP-zero location of $\mathbf{J}(s)$. By using (15), the bandwidth of the active-power controller of power-synchronization control at the two converter stations can be calculated as $\alpha_{p1} = 160$ rad/s and $\alpha_{p2} = 210$ rad/s. The bandwidths of the alternating-voltage controllers, however, do not need to be very high. Thus, they have been chosen as $\alpha_{u1} = \alpha_{u2} = 50$ rad/s.

B. Direct-Voltage Controller

As mentioned in Section III-C, the bandwidth of the direct-voltage controllers should be chosen at least four times slower than the active-power controller of the power-synchronization control. Alternatively, the bandwidth of the direct-voltage controllers can be calculated directly by substituting the SCR and maximum loading into (42), which yields $\alpha_{d1} = 39$ rad/s and $\alpha_{d2} = 53$ rad/s. However, the linear analysis shows that the direct-voltage controller at the rectifier side (station 2) tends to have less phase margin than the inverter side (station 1). Therefore, the bandwidth of both of the direct-voltage controllers have been chosen as $\alpha_{d1} = \alpha_{d2} = 40$ rad/s. Fig. 11 shows the step response of the direct-voltage controllers at the two converter stations with the comparison between the linear model and the nonlinear model in PSCAD/EMTDC.

Fig. 12 shows the plots of disturbance reduction of the direct-voltage controller with the comparison between the linear model and the nonlinear model in PSCAD/EMTDC. The maximum direct-voltage peak in Fig. 12(b) is below the specification

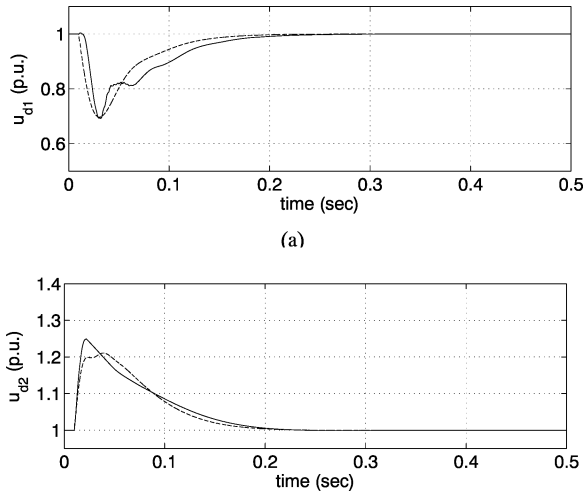

Fig. 12. Disturbance reductions of the direct-voltage controllers with maximum load changes. (a) Converter block at station 2. (b) Converter block at station 1 (solid: nonlinear simulation, dashed: linear model).

$u_{d,\max} = 1.3$ p.u. The discrepancies between the linear result and nonlinear simulation result are due to that the linear result is obtained at one operating point, while the disturbance reduction in PSCAD/EMTDC involves operating point changes. The tests in PSCAD/EMTDC are performed by blocking the converter at the other station with maximum loading.

C. Active-Power Controller

In principle, either of the VSC-HVDC converter stations can be the power-controlling station. In this example, the converter station 1 controls the active power by a PI controller with the control law

$$\Delta\left(u_{d1}^{\text{ref}}\right)^2 = \underbrace{-K_{pp}\left(1+\frac{K_{ip}}{s}\right)}_{F_{\text{pc}}(s)}\left[P_1^{\text{ord}} - P_1\right]. \qquad (44)$$

The parameters of the active-power controller are tuned by the root-locus technique. The proposed PI controller has two parameters. Thus, the first step is to determine the value of the K_{ip}. A higher integral gain of a PI controller is necessary for eliminating error in steady state, as well as reducing the power-recovery time after ac-system faults. However, a large integral gain may also reduce the phase margin of the closed-loop system. Thus, the initial integral gain is chosen as $K_{ip} = 30$. It should be noted that K_{ip} might need to be re-adjusted based on the time simulation result.

Fig. 13 shows the root-loci of the closed-loop system by varying K_{pp} from 0.0 to 1.0; three dominant pole pairs are affected. The pole pair $p_{5,6}$ are shifted from the origin towards the left-half plane, which can be viewed as the stabilizing effect of the feedback control. However, both the pole pairs $p_{1,2}$ $(-64 \pm j233)$ and $p_{3,4}$ ($p_3 = -37.2$, $p_4 = -50.0$) are shifted towards the right-half plane. Frequency domain analysis show that $p_{1,2}$ are related to the gain margin, while $p_{3,4}$ are related to the phase margin of the active-power control. $K_{pp} = 0.6$ is chosen to get a balance of stability and

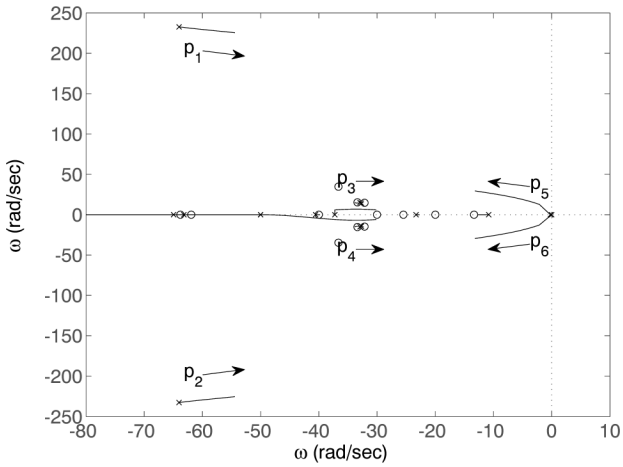

Fig. 13. Root-loci of the dominant poles of the closed-loop system by applying PI-type active-power control. $K_{ip} = 30$, K_{pp} from 0 to 1.0.

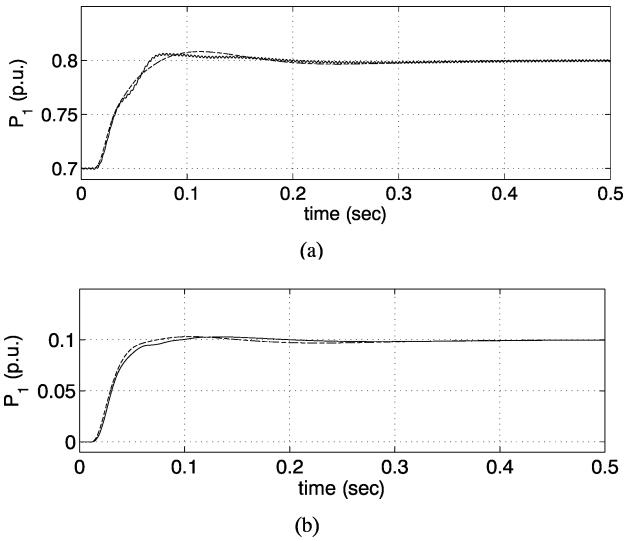

Fig. 14. Step response of the active-power controller at low and high power levels at the converter station 1. (a) Step from $P_1 = 0.7$ p.u. to $P_1 = 0.8$ p.u. (b) Step from $P_1 = 0.0$ p.u. to $P_1 = 0.1$ p.u. (solid: nonlinear simulation, dashed: linear model). Active-power controller: $K_{pp} = 0.6$, $K_{ip} = 30$.

response time, which places the three dominant pole pairs at $p_{1,2} = -54.6 \pm j225$ rad/s, $p_{3,4} = -30.2 \pm j5.86$ rad/s, and $p_{5,6} = -12.3 \pm j28.5$ rad/s.

Fig. 14 shows the step response of the active-power control at low and high power levels, respectively. The step response at the high power level corresponds to the operating point applied for the root-locus tuning. The output of the active-power controller should be limited to avoid too large direct-voltage variations. In this example, the limitation of the output of the active-power controller is chosen as ± 0.25, which corresponds to approximately $+12\%$ and -13% direct-voltage variations.

D. AC-System Faults

The fault ride-through capability of the VSC-HVDC link is tested in PSCAD/EMTDC by applying three-phase ac-system faults at both of the converter stations. The VSC-HVDC link initially operates with maximum loading, i.e., $P_1 = 0.86$ p.u. The VSC-HVDC link is supposed to ride through ac-system faults

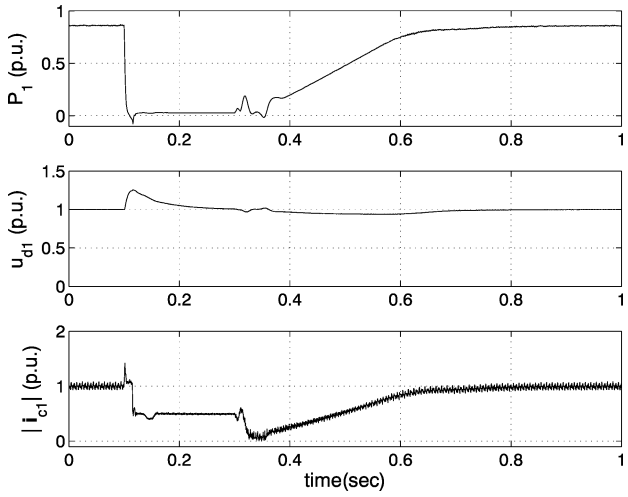

Fig. 15. Fault ride-through capability of the VSC-HVDC link with a three-phase ac-system fault at the inverter station (station 1).

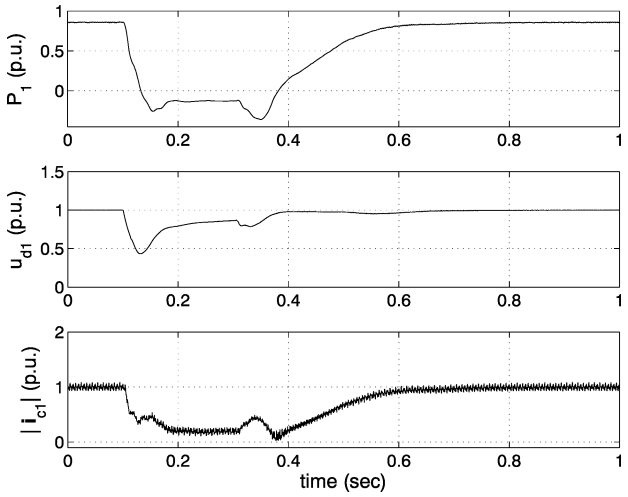

Fig. 16. Fault ride-through capability of the VSC-HVDC link with a three-phase ac-system fault at the rectifier station (station 2).

without relying on telecommunications between the two converter stations.

In Fig. 15, a three-phase ac fault with 0.2 s duration is applied at the converter station 1, i.e., the power-controlling station in this example, at 0.1 s. One consequence of the ac fault is that the direct voltage increases to approximately 1.3 p.u. due to the loss of power output. The converter station 2 brings down the direct voltage to its nominal value after an initial overshooting. Another consequence of the ac fault is the increase of the modulus of the valve current $|\mathbf{i}_{c1}|$. A current limitation controller proposed in [18] has been applied during the ac-system fault. After detecting the fault, the current limiter reduces the valve current to half of the maximum load current $I_{\max}$ except a very short current spike at the fault inception. For VSC applications, regardless of the control principle, the converter always tries to protect itself from excessive over currents. This fast protection is often implemented as a low-level hardware system, and its objective is to protect the converter in cases where the higher levels of control fail. Since the current spike in Fig. 15 is so short (< 1.4 p.u. in magnitude and < 5 ms) in duration, it neither does any harm to the converter valve, nor contributes much to the short-circuit current to the ac system.

Fig. 16 shows a three-phase ac fault with 0.2 s duration applied at the converter station 2, i.e., the direct-voltage controlling station in this example, at 0.1 s. During the ac-system fault, the power-controlling station controls the direct voltage to a lower voltage level which is 13% less than the nominal value. The 13% is a result of the limitation of the power controller. Since the ac fault is applied at the converter station 2, there is no over-current problem at the converter station 1. A specific amount of active power flows in the reverse direction during the fault period. However, the current limitation controller at the rectifier (station 2) limits the fault current to half of the maximum load current, or any other desired value.

A benchmark with vector current control is performed in [18]. It was found that vector current control could not operate in the conditions corresponding to Figs. 15 and 16.

V. Conclusions

In this paper, VSC-HVDC system using power-synchronization control is investigated for interconnection of two very weak ac systems. By using power-synchronization control, the VSC-HVDC link is possible to be applied in more challenging conditions. In addition, the VSC-HVDC link contributes short-circuit capacity to the ac system at the PCC without increasing the short-circuit current thanks to its current limiting capability during ac-system faults. The major consideration for VSC-HVDC links connected to weak ac systems is that the RHP transmission zero of the ac Jacobian transfer matrix, which moves closer to the origin with larger load angles. The RHP zero imposes a fundamental limitation on the achievable bandwidth of the VSC, which implies the following for VSC-HVDC links interconnecting two very weak ac systems.

- At either of the converter stations, the VSC-HVDC converter shall not operate with too large load angles in the steady state to maintain a reasonable stability margin.
- A higher dc capacitance is necessary to keep the variation of the direct voltage within the allowed range.
- The active-power controller at the power-controlling station should use the direct-voltage controller as the inner loop and limit its output in order not to affect the direct-voltage level too much from its nominal value.

Appendix A

AC system base value: power $S_{aN} = 350$ MVA, line-to-line voltage $U_{aN} = 195$ kV, nominal frequency $f = 50$ Hz.

DC system base value: power $P_{dN} = 350$ MW, pole-to-ground voltage $U_{dN} = 150$ kV.

VSC-HVDC link: rated power $P = 350$ MW, rated alternating voltage $U = 195$ kV, maximum valve current $I_{\max} = 1.12$ kA, maximum allowed direct voltage $u_{d,\max} = 1.3$ p.u., $L_c = 0.069$ H, $R_c = 1.089\ \Omega$, dc capacitance per pole 233.3 μF (15 ms in total), switching frequency $f_{\text{sw}} = 1650$ Hz.

APPENDIX B

In the following, a mathematical proof of the instability of the dc Jacobian transfer matrix $\mathbf{G}_d(s)$ for operating points that $P_{d10} \neq 0$ and $P_{d20} \neq 0$ is given. $\mathbf{G}_d(s)$ is a linear model of the dc π-link in Fig. 4.

The poles of $\mathbf{G}_d(s)$ are the eigenvalues of the A matrix in (28) which has the characteristic equation

$$\det(\lambda I - A) = \lambda^3 + a_1\lambda^2 + a_2\lambda^2 + a_3 = 0 \tag{45}$$

with the coefficients

$$\begin{aligned} a_1 &= \frac{P_{d10}}{u_{d10}^2 C_{d1}} + \frac{P_{d20}}{u_{d20}^2 C_{d2}} + \frac{R_d}{L_d} \\ a_2 &= \frac{P_{d10}P_{d20}}{U_{d10}^2 u_{d20}^2 C_{d1}C_{d2}} + \frac{P_{d10}R_d}{u_{d10}^2 L_d C_{d1}} + \frac{P_{d20}R_d}{u_{d20}^2 L_d C_{d2}} \\ &\quad + \frac{1}{L_d C_{d1}} + \frac{1}{L_d C_{d2}} \\ a_3 &= \frac{P_{d10}u_{d20}^2 + P_{d20}u_{d10}^2 + P_{d10}P_{d20}R_d}{U_{d10}^2 u_{d20}^2 L_d C_{d1} C_{d2}}. \end{aligned} \tag{46}$$

To prove the *instability* of $\mathbf{G}_d(s)$, it is *sufficient* that any one of the three coefficients in (46) is negative. The following is a proof of

$$a_3 < 0. \tag{47}$$

It is obvious that the denominator of a_3 in (46) is positive. Thus, (47) is identical to

$$P_{d10}u_{d20}^2 + P_{d20}u_{d10}^2 + P_{d10}P_{d20}R_d < 0. \tag{48}$$

From the main circuit of the π-link model in Fig. 4, the following equality is established:

$$\frac{P_{d10}}{u_{d10}} = i_{d0} = -\frac{P_{d20}}{u_{d20}}. \tag{49}$$

For VSC-HVDC applications, it is apparent that u_{d10} and u_{d20} have the same polarity. Consequently, it follows from (49) that

$$\frac{P_{d10}}{P_{d20}} < 0 \tag{50}$$

or

$$P_{d10}P_{d20} < 0. \tag{51}$$

Based on the inequality in (51), by dividing $P_{d10}P_{d20}$ at both sides, (48) can be rewritten as

$$\frac{u_{d20}^2}{P_{d20}} + \frac{u_{d10}^2}{P_{d10}} + R_d > 0. \tag{52}$$

Substituting

$$\begin{aligned} P_{d10} &= u_{d10}i_{d0}, \quad P_{d20} = -u_{d20}i_{d0} \\ u_{d20} &= u_{d10} - R_d i_{d0} \end{aligned} \tag{53}$$

into (52) yields

$$2R_d > 0 \tag{54}$$

which apparently holds. In other words, for other operating points when $P_{d10} \neq 0$ and $P_{d20} \neq 0$, $\mathbf{G}_d(s)$ is unstable as long as the dc-transmission line is not lossless.

REFERENCES

[1] B. Weedy and B. Cory, *Electric Power Systems*, 4th ed. West Sussex, U.K.: Wiley, 1998.

[2] W. Breuer, M. Lemes, and D. Retzmann, "Perspectives of HVDC and FACTS for system interconnection and grid enhancement," in *Proc. Cigre Workshop: Brazil-China-India Summit Meeting on HVDC and Hybrid Systems*, Rio de Janeiro, Brazil, 2006.

[3] G. Andersson, P. Donalek, R. Farmer, and N. Hatziargyriou, "Causes of the 2003 major grid blackouts in North America and Europe, and recommended means to improve system dynamic performance," *IEEE Trans. Power Syst.*, vol. 20, no. 4, pp. 1922–1928, Nov. 2005.

[4] B. Yang, G. Vittal, and G. Heydt, "Slow-coherency-based controlled islanding-a demonstration of the approach on the August 14, 2003 blackout scenario," *IEEE Trans. Power Syst.*, vol. 21, no. 4, pp. 1840–1847, Nov. 2006.

[5] J. Arrillaga, *High Voltage Direct Current Transmission*, 2nd ed. London, U.K.: Inst. Elect. Eng., 1998.

[6] M. Bahrman and B. Johnson, "The ABCs of HVDC transmission technologies," *IEEE Power Energy Mag.*, vol. 5, no. 2, pp. 32–44, Mar./Apr. 2007.

[7] V. Ramaswami, D. Retzmann, and K. Uecker, "Prospects of bulk power EHV and UHV transmission," in *Proc. GRIDTECH 2007 Int. Conf.*, New Delhi, India, 2007.

[8] IEEE Guide for Planning DC Links Terminating at AC Locations Having Low Short-Circuit Capacities, 1997, IEEE Std. 1204–1997, Tech. Rep.

[9] B. Franken and G. Andersson, "Analysis of HVDC converters connected to weak systems," *IEEE Trans. Power Syst.*, vol. 5, no. 1, pp. 235–242, Feb. 1990.

[10] A. Gavrilovic, "AC/DC system strength as indicated by short circuit ratios," in *Proc. AC/DC Power Transmission Int. Conf.*, London, U.K., 1991.

[11] O. B. Nayak, A. M. Gole, D. G. Chapman, and J. B. Davies, "Dynamic performance of static and synchronous compensators at an HVDC inverter bus in a very weak ac system," *IEEE Trans. Power Syst.*, vol. 9, no. 3, pp. 1350–1358, Aug. 1994.

[12] D. Jovcic, N. Pahalawaththa, and M. Zavahir, "Investigation of the use of inverter control strategy instead of synchronous condensers at inverter terminal of an HVDC system," *IEEE Trans. Power Del.*, vol. 15, no. 2, pp. 704–709, Apr. 2000.

[13] G. Asplund, K. Eriksson, and H. Jiang, "DC transmission based on voltage source converters," in *Proc. Cigre Conf. 14–302*, Paris, France, 1998.

[14] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[15] D. Jovcic, L. Lamont, and L. Xu, "VSC transmission model for analytical studies," in *Proc. IEEE Power Eng. Soc. General Meeting*, Toronto, ON, Canada, 2003.

[16] M. Durrant, H. Werner, and K. Abbott, "Model of a VSC HVDC terminal attached to a weak ac system," in *Proc. IEEE Conf. Control Applications*, Istanbul, Turkey, 2003.

[17] P. Fischer, "Modelling and control of a line-commutated HVDC transmission system interacting with a VSC STATCOM," Ph.D. dissertation, Royal Inst. Technol., Stockholm, Sweden, 2007.

[18] L. Zhang, L. Harnefors, and H.-P. Nee, "Power-synchronization control of grid-connected voltage-source converters," *IEEE Trans. Power Syst.*, vol. 25, no. 2, pp. 809–820, May 2010.

[19] L. Zhang and H.-P. Nee, "Multivariable feedback design of VSC-HVDC connected to weak AC systems," in *Proc. PowerTech 2009*, Bucharest, Romania, 2009.

[20] S. Skogestad and I. Postlethwaite, *Multivariable Feedback Control*, 2nd ed. New York: Wiley, 2005.

[21] P. Kundur, *Power System Stability and Control*. New York: McGraw-Hill, 1993.

[22] R. Ottersten, "On control of back-to-back converters and sensorless induction machine drives," Ph.D. dissertation, Chalmers Univ. Technol., Gothenburg, Sweden, 2003.

Lidong Zhang (M'07) received the B.Sc. degree from the North China Electric Power University, Baoding, China, in 1991 and the Tech.Lic degree from Chalmers University of Technology, Gothenburg, Sweden, in 1999. Since 2007, he has been pursuing the Ph.D. degree in industrial engineering part time at the Royal Institute of Technology, Stockholm, Sweden.

From 1991 to 1996, he worked as an engineer with the Leda Electric Co., Beijing, China. Since 1999, he has been with ABB Power Systems, Ludvika, Sweden. His research interests are HVDC, power system stability and control, and power quality.

Lennart Harnefors (S'93–M'97–SM'07) was born in 1968 in Eskilstuna, Sweden. He received the M.Sc., Licentiate, and Ph.D. degrees in electrical engineering from the Royal Institute of Technology, Stockholm, Sweden, and the Docent (D.Sc.) degree in industrial automation from Lund University, Lund, Sweden, in 1993, 1995, 1997, and 2000, respectively.

From 1994 to 2005, he was with Mälardalen University, Västerås, Sweden, where he, in 2001, was appointed as a Professor of electrical engineering. He is currently with ABB Power Systems, Ludvika, Sweden. From 2001 to 2006, he was also a part-time Visiting Professor of electrical drives at Chalmers University of Technology, Gothenborg, Sweden. His research interests include applied signal processing and control, in particular, control of power electronic systems and ac drives.

Prof. Harnefors was the recipient of the 2000 ABB Gunnar Engström Energy Award and the 2002 IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS Best Paper Award. He is an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.

Hans-Peter Nee (S'91–M'96–SM'04) was born in 1963 in Västerås, Sweden. He received the M.Sc., Licentiate, and Ph.D degrees in electrical engineering from the Royal Institute of Technology, Stockholm, Sweden, in 1987, 1992, and 1996, respectively.

In 1999, he was appointed Professor of Power Electronics in the Department of Electrical Engineering at the Royal Institute of Technology. His interests are power electronic converters, semiconductor components and control aspects of utility applications, like FACTS and HVDC, and variable-speed drives.

Prof. Nee was awarded the Energy Prize by the Swedish State Power Board in 1991, the ICEM'94 (Paris) Verbal Prize in 1994, the Torsten Lindström Electric Power Scholarship in 1996, and the Elforsk Scholarship in 1997. He has served in the board of the IEEE Sweden Section for many years and was the chairman of the board during 2002 and 2003. He is also a member of EPE and serves in the Executive Council and in the International Steering Committee. Additionally, he is active in IEC and the corresponding Swedish organization SEK in the committees TC 25 and TK 25, respectively.