# Impact of Short-Circuit Ratio and Phase-Locked-Loop Parameters on the Small-Signal Behavior of a VSC-HVDC Converter

Jenny Z. Zhou, *Member, IEEE*, Hui Ding, *Member, IEEE*, Shengtao Fan, *Member, IEEE*, Yi Zhang, *Senior Member, IEEE*, and Aniruddha M. Gole, *Fellow, IEEE* 

Abstract—The impact of phase-locked loop (PLL) parameters on the dynamic and steady-state behavior of a voltage-source converter (VSC) in an HVDC transmission system is determined as a function of the system strength [parameterized by the short-circuit ratio (SCR)]. This is achieved by using a linearized small-signal model of the converter system and its controls. The model is validated via electromagnetic transients simulation of the fully detailed large signal model. An interesting result from this study is that the maximum power transfer capability of the VSC-HVDC converter is affected by the PLL gains, and that the theoretical limit (obtained from static voltage stability analysis) is approachable as the PLL gains become very small. This paper shows that gains of the PLL, particularly at low SCRs, greatly affect the operation of the VSC-HVDC converter and that operation at low SCRs approaching 1.3 is very difficult.

Index Terms—HVDC transmission, maximum power transfer, phase-locked loop (PLL), short-circuit ratio (SCR), small-signal analysis, voltage-source converter (VSC).

## I. INTRODUCTION

RALIER work [1] presented an investigation into the power transmission limitations imposed on a VSC-HVDC converter by ac system strength quantified by the short-circuit ratio (SCR) [2]. With an ac network fundamental frequency impedance of  $Z_s = R_s + jX_s$ , the rated ac voltage and power of the VSC as  $V_t$  and  $P_{\rm rated}$ , respectively, this is given by SCR =  $[V_t^2/|Z_s|]/P_{\rm rated}$ . An important observation was that the maximum power transfer of the converter is affected by the SCR and the angle of the ac system impedance ( $\phi = \tan^{-1}(X_s/R_s)$ ) at the fundamental frequency. Research in [3] and [4] also indicated that for stable operation of the VSC-HVDC system, the short-circuit megavolt amperes (MVA) of the ac network had to be somewhat larger than the transmitted dc power. Reference [5] showed that the

Manuscript received August 19, 2013; revised December 09, 2013, February 02, 2014, and May 12, 2014; accepted June 06, 2014. Date of publication July 08, 2014; date of current version September 19, 2014. This work was supported by the Natural Sciences and Engineering Council (NSERC) of Canada.

J. Z. Zhou, H. Ding, S. Fan, and A. M. Gole are with the Department of Electrical and Computer Engineering, University of Manitoba, Winnipeg, MB R3T 5V6 Canada (e-mail: jzhou@teshmont.com; umhvdc@gmail.com; shengtaofan@gmail.com; gole@ee.umanitoba.ca).

Y. Zhang is with RTDS Technologies Inc., Winnipeg, MB R3T 2E1 Canada (e-mail: yzhang@rtds.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPWRD.2014.2330518

converter's active-reactive power characteristic is constrained by the converter's MVA rating and the configuration of the converter. However, the control system plays a large role in how closely these theoretical maximum power transfer limits are achievable, an aspect which has not been widely studied in earlier work.

The phase-locked loop (PLL) is typically used for angle reference generation for the traditional line-commutated converter (LCC)-based HVDC and the newer voltage-sourced converter (VSC)-based HVDC transmission applications [6], [7]. This angle reference is used for generating the firing pulses for the insulated-gate bipolar transistor (IGBT) switches of the VSC. It has been recognized that operation at low SCRs is challenging for VSCs [1], [3], [4], [8]. Some authors have recommended an alternate firing methodology to the PLL [4], [8] as a solution to this challenge. Also, some earlier literature discusses the tracking capability of the PLL when connected to various distorted or changing ac waveforms [9] but does not consider the ac network impedance.

There is a wide range of PLL types currently in use in HVDC schemes [10]–[13]. These follow the same operating principle, and differ mainly in the area of phase-angle measurement. The dq-type PLL presented in [10] is widely used in actual applications [14] and is used in this paper. For other topologies, a similar analysis could be carried out using the approach presented in this paper, and may yield different numerical values for limits to operation. This additional analysis is left for future research.

Indications of possible challenges of high grid impedance (although considering a different control strategy and without any discussion of PLL or synchronization issues) are given in [15]; whereas [16] uses simulation to show that the stability of a VSC with high grid impedance is affected by the PLL gains. Examples of poor performance that can occur with the application of nonlinear current controllers in high grid impedance systems (again without considering the influence of PLL parameters) are also given in [17] [18]. Several studies [9], [19]-[21] of VSC converters operating as pulsewidth-modulated (PWM) rectifiers present the stability limits of the converter, and show how this stability limit can be influenced by converter controls. These studies do not explicitly address the issue of PLL parameters and their influences on the stability limits, but rather indicate how reactive power control might influence the stability limits with various system configurations.

0885-8977 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

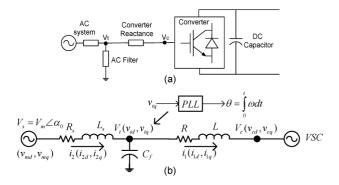


Fig. 1. (a) VSC-HVDC system and (b) equivalent circuit for linearized analysis.

Earlier work [1], [16] showed using numerical simulation only that the VSC's performance, particularly at low SCRs, is significantly affected by the gains of the PLL. Although the influence of PLL parameters on control system dynamics and stability limits for the VSC can be easily found by trial-and-error simulations, and has also been implicitly identified in some previous publications, a quantitative study has been lacking in the available literature on VSC control. This paper aims to study this behavior in detail by using an analytical framework. In order to investigate the impact of PLL on system performance at different SCRs, a small-signal model of the VSC, including its PLL, is developed in this paper. Small-signal stability analysis is applied to investigate how the power system impedance and the parameters of the PLL influence the dynamic behavior and the stability limits of the VSC in HVDC applications. Unlike previous simulation-based work, the analytical frequency-domain approach provides a fundamental, mathematical understanding of how the stability limit changes with parameter values, how the damping is affected, and so on. Earlier research has used static power voltage stability analysis (i.e., without consideration of controller dynamics) to determine the theoretical maximum power limit as a function of the SCR [1]. Using smallsignal analysis, this paper shows that at low SCRs, these theoretical limits can only be approached when the gains of the PLL are reduced.

#### II. LINEARIZED STATE-SPACE VSC MODEL

Linear system theory methods [22] are used to analyze the impact of the PLL on the behavior of the VSC HVDC system. In this paper, a state-space equation of the VSC-HVDC system is derived, which considers the PLL dynamics, the dq-decoupled control system, and the dynamics of the ac network.

## A. Description of the Test System

Fig. 1(a) shows the VSC converter considered in this paper and Fig. 1(b) shows its equivalent circuit used for developing the small-signal model. The ac source is modeled as a Thévenin impedance consisting of  $R_s$  and  $L_s$ ; and the capacitor  $C_f$  represents the shunt filter. The VSC side is modeled by a phase reactor L, a loss resistance R, and a source  $V_c$  representing the VSC's internal voltage.

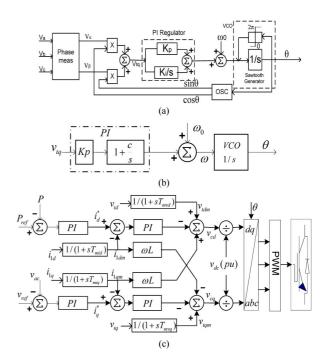


Fig. 2. Control block diagram of the VSC system. (a) PLL topology [10]. (b) PLL transfer function. (c) dq decoupled control [24], [25].

The control block diagram of the system can be represented as in Fig. 2, which includes the PLL control, the voltage and the current measurement delay, the inner current  $(i_d, i_q)$  control loop, and the outer power (P), ac voltage  $(v_{ac})$  control loop.

The PLL shown in Fig. 2(a) is modeled as in [10], and is similar to the PLL used in Hydro Quebec's Chateauguay [14] station. Its linearized model [7] is shown in Fig. 2(b), where the P-I loop filter acts on the phase error signal and feeds the voltage controlled oscillator (VCO). The VCO also has a free-running frequency input  $\omega_0$ . The phase error is actually  $v_{tq}$ , the q-axis voltage at the PLL control point. The proportional and integral gains of the PLL are  $Kp_{\text{PLL}} = K_p$  and  $Ki_{\text{PLL}} = c \cdot K_p$ . This form makes it convenient for the root locus plots later in this paper. Any transducer delays in phase voltage measurement for the PLL are considered to be negligible [23]. The power, ac voltage, and decoupled dq axis control system is shown in Fig. 2(c). It has a decoupled inner control loop which generates the d and q axis voltage orders  $v_{cd}$  and  $v_{cq}$  from the current orders  $i_d^*$  and  $i_q^*$ . The voltage orders from the inner loop are divided by the dc voltage  $v_{\rm dc}$  (per unit) (normally 1.0). The outer control loops are responsible for real power and ac voltage regulation, respectively. They generate the direct and quadrature reference signals for the inner loop.

## B. System and Control Equations

The state-space model derived in this paper includes the ac system shown in Fig. 1 and the VSC controls shown in Fig. 2.

1) AC System Network Equations: Using Park transformation, with the d axis aligned with the PLL control voltage  $v_t$ , the dynamic equations of the ac network in Fig. 1(b) can be written as (1), where the subscripts "d" and "q" represent the corresponding d and q coordinate quantities. The angle used in

| TABLE I |            |           |              |  |  |  |
|---------|------------|-----------|--------------|--|--|--|
| System  | PARAMETERS | FOR MODEL | VERIFICATION |  |  |  |

| Equivalent ac system V <sub>m</sub> (base) | 1.0 pu, 60 Hz |
|--------------------------------------------|---------------|
| Equivalent ac system SCR                   | 1.6 or 4.0    |
| Ac system impedance angle                  | 80°           |
| Rated dc power rating (base)               | 1.0 pu        |
| PLL controlled voltage V <sub>t</sub>      | 1.0 pu, 60 Hz |
| Converter reactance L                      | 0.15 pu       |
| Passive filter C <sub>f</sub>              | 0.15 pu       |
| 2-level PWM switching frequency            | 1980 Hz       |

TABLE II
OPTIMIZED GAINS FOR A POWER CONTROLLING CONVERTER

| PLL $(Kp_{PLL} = K_p, Ki_{PLL} = 5K_p)$                                    | $K_p$ varies from low to high values |
|----------------------------------------------------------------------------|--------------------------------------|
| Measurement time constants (T <sub>mvd</sub> , T <sub>mvq</sub> ) (s)      | (0.02, 0.02)                         |
| Measurement time constants $(T_{mid}, T_{miq})$ (s)                        | (0.0012, 0.0012)                     |
| Power controller gains (Kp <sub>P</sub> , Ki <sub>P</sub> )                | (0.5, 50)                            |
| Ac voltage controller gains (Kp <sub>v</sub> , Ki <sub>v</sub> )           | (0.5, 50)                            |
| Inner i <sub>d</sub> controller gains (Kp <sub>1</sub> , Ki <sub>1</sub> ) | (2, 100)                             |
| Inner i <sub>q</sub> controller gains (Kp <sub>2</sub> , Ki <sub>2</sub> ) | (2, 100)                             |

the Park transformation is the angle  $\theta$  as measured by the PLL, and  $\omega$  is its derivative [also see(5)]

$$\begin{cases}
L\frac{d}{dt} \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} = \begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} - \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} - \omega L \begin{bmatrix} -i_{1q} \\ i_{1d} \end{bmatrix} - R \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} \\
L_s\frac{d}{dt} \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} = \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} - \begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} - \omega L_s \begin{bmatrix} -i_{2q} \\ i_{2d} \end{bmatrix} - R_s \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} \\
C_f\frac{d}{dt} \begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} = \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} - \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} - \omega C_f \begin{bmatrix} -v_{tq} \\ v_{td} \end{bmatrix}
\end{cases}$$
(1

Note that although a specific topology is assumed in Fig. 1(b), any ac network can readily be included by writing its differential equations in a form similar to (1).

2) Power, AC Voltage and dq Axis Controller Equations: The d- and q-axis measured quantities  $v_{td}, v_{tq}$  and  $i_{1d}, i_{1q}$  are passed through filters (modeled as first-order lags) that provide high-frequency noise filtering as shown in Fig. 2(c). The resulting filtered quantities are  $v_{tdm}, v_{tqm}$  and  $i_{1dm}, i_{1qm}$ , respectively. The mathematical relationship between these variables is given by (2), where  $T_{mvd}, T_{mvq}$ , and  $T_{mid}, T_{miq}$  are the time constants of these filters

$$\begin{cases} v_{tdm} + T_{mvd} \frac{dv_{tdm}}{dt} = v_{td}, & v_{tqm} + T_{mvq} \frac{dv_{tqm}}{dt} = v_{tq} \\ i_{1dm} + T_{mid} \frac{di_{1dm}}{dt} = i_{1d}, & i_{1qm} + T_{miq} \frac{di_{1qm}}{dt} = i_{1q} \end{cases}$$
(2)

The outer loop controllers and inner loop controllers in Fig. 2(c) can be written as (3) and (4), respectively. Here, the converter is considered to be in the power and ac voltage-control mode, and the remote converter is responsible for maintaining the dc voltage.  $P_{\rm ref}$  and  $v_{\rm ref}$  are reference values for real power control and ac voltage control, respectively.  $Kp_p, Ki_P$ , and  $Kp_v, Ki_v$  are the proportional-integral (PI) control parameters for the real power controller and ac voltage controller respectively.  $Kp_1, Ki_1$  and  $Kp_2, Ki_2$  are the PI control parameters for direct and quadrature current controllers, respectively. Note that  $v_{\rm dc}$  does not explicitly appear in the equations, because when the PWM-generated firing pulses are applied to the

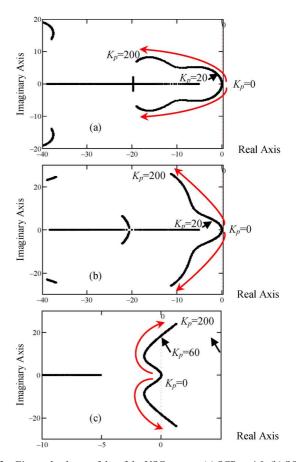


Fig. 3. Eigenvalue locus of the of the VSC system: (a) SCR = 4.0, (b) SCR = 1.6, and (c) SCR = 1.3.

converter switches, the output ac voltage is proportional to the product of the modulation index and dc voltage. Predividing by  $v_{\rm dc}$  as in Fig. 2(c) cancels out the dependence on dc voltage. Thus, the model is built for slow change in dc voltage

$$\begin{cases}
e_{P} = P_{\text{ref}} - (v_{tdm}i_{1dm} + v_{tqm}i_{1qm}) \\
e_{V} = v_{\text{ref}} - \sqrt{v_{tdm}^{2} + v_{tqm}^{2}} \\
i_{d}^{*} = Kp_{P} \cdot e_{P} + Ki_{P} \int e_{P}dt \\
i_{q}^{*} = Kp_{V} \cdot e_{V} + Ki_{V} \int e_{V}dt \\
\begin{cases}
v_{cd} = v_{tdm} + i_{1qm} \cdot \omega L \\
- [Kp_{1}(i_{d}^{*} - i_{1dm}) + Ki_{1} \int (i_{d}^{*} - i_{1dm}) dt] \\
v_{cq} = v_{tqm} - i_{1dm} \cdot \omega L \\
- [Kp_{2}(i_{q}^{*} - i_{1qm}) + Ki_{2} \int (i_{q}^{*} - i_{1qm}) dt]
\end{cases}$$
(4)

3) PLL Control Equations: The dynamics of the PLL controller can be represented by (5), where  $\omega$  is the angular frequency and  $\theta$  is the phase angle from the PLL which is synchronized to the ac voltage waveform at the point of common coupling (PCC). Here,  $K_P$  and  $cK_P$  are the proportional and integral gains of the PLL controller.

The phase "a" reference waveform for the VSC source can thus be obtained as  $v_{ca}(t) = \sqrt{v_{cq}^2 + v_{cd}^2} \cdot \sin(\theta + \alpha)$ , where  $\alpha = \arctan(v_{cq}/v_{cd})$ . Phase "b" and "c" reference waveforms can similarly be generated with additional 120° phase shifts. The

| SCR=1.6            |                      | SCR=4.0              |                     |
|--------------------|----------------------|----------------------|---------------------|
| PLL $K_p=10$       | PLL $K_p$ =100       | PLL $K_p=10$         | PLL $K_p$ =100      |
| -184.006±j3811     | -185.909±j3817       | -150.274±j4038       | -154.585±j4045      |
| -141.311±j3160     | -158.606±j3175       | -116.427±j3367       | -130.011±j3381      |
| -242.678±j1010     | -232.062±j1019       | -283.813±j1392       | -278.211±j1396      |
| -270.975±j452.829  | -267.107±j480.304    | -281.369±j883.164    | -269.188±j893.937   |
| -56.46±j47.701     | -80.579±j45.437      | -61.753±j21.296      | -78.762±j22.572     |
| -35.627±j23.768    | -36.508±j23.484      | -36.965±j13.694      | -41.909±j18.817     |
| -25.976            | -34.708              | -20.883              | -34.756             |
| -12.606            | -5.263               | -16.361              | -5.334              |
| $-3.817 \pm i6.49$ | $-10.149\pm j21.516$ | $-4.043 \pm j 5.075$ | $-17.295\pm j7.289$ |

 $\label{eq:table III} \text{Eigenvalues of the Test System for } P = 1.0 \text{ p.u.}$ 

insulated-gate bipolar transistor (IGBT) firing control system issues firing pulses to the IGBT valves to produce these waveforms for the VSC internal voltage. In this paper, a PWM two-level converter topology is assumed.

$$\begin{cases} \theta = \int \omega dt \\ \omega = \omega_0 + K_P v_{tq} + c \cdot K_p \int v_{tq} dt \end{cases}$$
 (5)

## C. State-Space VSC Model

The derivation of the state-variable equations is given in the Appendix. In order to develop the small-signal state-space equations for the system, the equations must first be linearized around the operating point. In this paper, the VSC's operating point is  $V_{\rm ac0}=1.0~\rm p.u.$  ac voltage and  $P_0=1.0~\rm p.u.$  dc power. This will yield the state-space model of the complete VSC system in the form of

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, \mathbf{u}). \tag{6}$$

Here, the state vector is 16-D (with 10 control state variables and 6 ac network variables), and the input variable is  $\mathbf{u} = [P_{\text{ref}} \ v_{\text{ref}}]$ . Equation (6) can be linearized to provide the small-signal state-variable form of

$$\Delta \dot{X} = A\Delta X + B\Delta U. \tag{7}$$

The derivation of (7) is given in the Appendix in sections A and B, with the final form in section C. The eigenvalues of A in section C provide useful information on the stability of the system as will be shown in the next section.

#### III. MODEL ANALYSIS AND VALIDATION

The system shown in Fig. 1 was used for analysis and validation. For validation, the small-signal model results were compared with those obtained from an electromagnetic transient (EMT) model where the VSC was represented in detail as a two-level pulsewidth-modulated converter.

The system parameters used for model validation are shown in Table I, and the control parameters are shown in Table II. All parameters are in per unit, with rated voltage and dc power as base. The PLL gains vary from low values to high values in order to evaluate the effect of PLL gains on the behavior of the VSC converter, while other controller gains are kept constant.

An earlier study [1] showed that the gains of the VSC inner and outer PI controllers have a limited effect on system transient performance compared to the gains of the PLL.

## A. Eigenvalue Analysis of the VSC Model

The eigenvalue locus of the P = 1.0 p.u. operating point for the PLL gain  $K_p$  that changes from 0 to 200 is plotted (with  $K_i$ set to  $5K_p$  as in Table II). The expanded root locus, showing poles closest to the imaginary axis, is shown in Fig. 3 for SCR = 4.0, SCR = 1.6, and SCR = 1.3, respectively. For SCRs of 4.0 and 1.6, the system is stable for all  $K_p$  values. Indeed, by looking at the root locus, the poles for both of these ac network strengths move more into the left half plane (LHP) as the gain increases. However, when the SCR is reduced to 1.3, the system becomes unstable for  $K_p > 60$ . This is opposite to the situation for higher SCRs, where the system poles move away from the imaginary axis as  $K_p$  increases. A more detailed analysis shows that the SCR value below which unstable poles are possible is 1.32. This suggests that the PLL gain will have to be reduced for weak ac networks. A similar observation was reported in [1] and [16], where numerical EMT simulation was used to obtain results.

The eigenvalues of the P=1.0 p.u. operating point for ac system SCRs of 1.6 and 4.0 for low  $(K_p=10)$  and high  $(K_p=100)$  PLL gains are shown in Table III. The dominant oscillatory eigenvalues for each case are shadowed in gray in Table III.

#### B. Damping Ratio of the VSC System Eigenvalues

The damping ratio [26] of an underdamped oscillation mode is defined as  $\zeta = -\sigma/\sqrt{\sigma^2 + \omega^2}$  (where  $\lambda = \sigma \pm j\omega$  is the eigenvalue of the mode). If the damping ratio  $\zeta$  is considered, the results shown in Fig. 4(a) and (b) indicate that  $K_p$  should be larger than approximately 20 for the stronger systems (SCR = 4 or 1.6) as then the damping ratio is uniformly high. When the ac system is weaker, for example, SCR = 1.3, as shown in Fig. 4(c), the damping ratio becomes negative with the PLL gain  $K_P >$  60, indicating instability. This is also seen in the root locus plot of Fig. 3(c).

In VSC-HVDC installations, additional reactive power support is often provided, in order to reduce the reactive power loading on the VSC valves [1]. This can be in the form of a reactive shunt capacitor. For a larger shunt capacitor, for example, one that provides 30% compensation (with rated dc power as base), Fig. 4(d) indicates that  $K_p$  must be below 55. However,

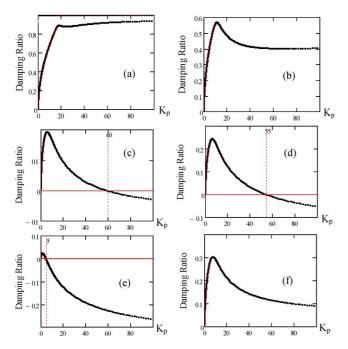


Fig. 4. K<sub>p</sub> versus damping ratio  $\zeta$ : (a) SCR = 4,  $C_f$  = 15%,  $\phi$  = 80°; (b) SCR = 1.6,  $C_f$  =15%,  $\phi$  = 80°; (c) SCR =1.3,  $C_f$  =15%,  $\phi$  = 80°; (d) SCR =1.3,  $C_f$  =30%,  $\phi$  = 80°; (e) SCR = 1.3,  $C_f$  = 15%,  $\phi$  = 78°; (f) SCR = 1.3,  $C_f$  = 15%,  $\phi$  = 82°.

Fig. 4(c) and (d) show that for the weaker system, the dominant poles of the system (i.e., the complex conjugate pair of eigenvalues closest to the  $j\omega$  axis) are far more poorly damped compared with the stronger systems of Fig. 4(a) and (b). Hence, it is expected that operation at very low SCRs approaching 1.3, will prove to be difficult.

Another observation is that when the ac system impedance angle is smaller, for example,  $78^{\circ}$  instead of  $80^{\circ}$  as in Fig. 4(e), the damping is poorer and instability is reached much sooner at  $\mathrm{Kp}=5$ . For a larger impedance angle, that is,  $82^{\circ}$ , Fig. 4(f) shows that the damping is much improved and there is no instability.

## C. Validation of the VSC Model

In order to validate the small-signal model, the time-domain response of the small-signal model was calculated using MATLAB and compared with the time-domain response of the nonlinear model simulated on the electromagnetic transient simulation program PSCAD/EMTDC. A few sample results of the transients in transmitted power (P) and ac voltage  $(V_{ac})$ following setpoint changes are shown in Figs. 5-7. In these figures, the subscript "SS" (e.g., P\_SS and Vac\_SS) refers to the results from the small-signal model and subscript "EMT" (e.g., P EMT and Vac EMT) refers to results from the detailed EMT simulation. Fig. 5 shows a comparison of the power responses obtained from the detailed nonlinear model and the small-signal model for a power order step change from 1.0 to 0.95 p.u. The simulations are for SCR = 1.6 and the low PLL gain of  $K_p = 10$  (i.e.,  $Kp_{\rm PLL} = 10$  and  $Ki_{\rm PLL} = 50$ ). Fig. 6 shows the EMT and small-signal time responses for the high PLL gain of  $K_p = 100$  (i.e.,  $K_{PLL} = 100$  and  $K_{iPLL} = 500$ ).

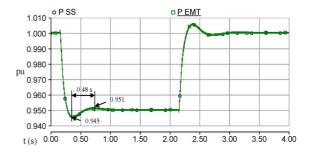


Fig. 5. Power step change from 1.0 to 0.95 p.u. for SCR = 1.6,  $K_p = 10$ .

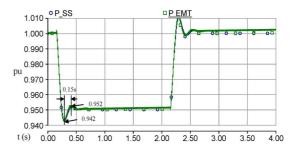


Fig. 6. Power step change from 1.0 to 0.95 p.u. for SCR = 1.6,  $K_p = 100$ .

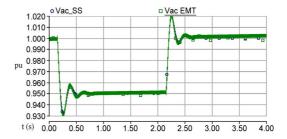


Fig. 7. Voltage step change from 1.0 to 0.95 p.u. for SCR = 1.6,  $K_p = 100$ .

Both figures show that the small-signal model is highly accurate as the two traces are nearly identical. They also show stable operation with low and high PLL gain. At higher gain (Fig. 6), the settling time is smaller than that at the lower gain (Fig. 5), but the transient overshoot is higher.

The calculated eigenvalues in Section III-A are also consistent with the results from EMT simulations. For example, for SCR = 1.6, the dominant eigenevalue for the low gain is  $(-3.817 \pm j6.49)$ . The simulated plot in Fig. 5 shows a half period of oscillation of 0.48 s. This is in complete agreement with the half period derived from the natural frequency of the dominant mode of  $(-3.817 \pm j6.49)$ , for which the half period is also  $0.5 \cdot (2\pi/(6.49)) = 0.48$  s. Likewise, the decay rate of the amplitude in a half cycle is also consistent with the real part of the dominant eigenvalue. Similarly, the small-signal model response was validated using the EMT response for a voltage step change from 1.0 to 0.95 p.u. when the power order is 1.0 p.u. The results are shown in Fig. 7 for the PLL gain of  $K_p = 100$ .

As seen from the root locus in Fig. 3(c), for a small SCR = 1.3, the VSC system becomes unstable for a PLL gain  $K_p > 60$ . Fig. 8 shows EMT simulation for SCR = 1.3, where the gain  $K_p$  is stepped from 10 (stable) to 100 (unstable) at t = 9 s.

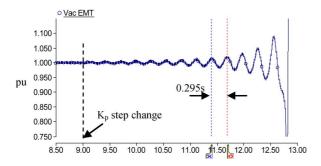


Fig. 8. PLL gain  $K_p$  step change from 10 to 100 for SCR = 1.3.

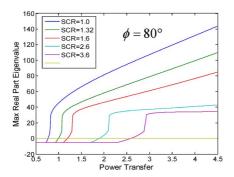


Fig. 9. Real part of the eigenvalue of the system versus power transfer ( $K_p = 100$ ).

The instability at the larger gain is clearly evident from the growing oscillations. The unstable mode eigenvalue for  $K_p = 100$  is  $(0.619 \pm j21.225)$ , which gives an oscillation period of  $2\pi/21.225 = 0.296\,$  s. The observed period (between dotted lines) in Fig. 8 is 0.295 s, showing good agreement.

## D. Possible Physical Reasoning for the Results

When the ac system is very weak, the phase of the ac busbar voltage  $V_t$  is highly sensitive to the converter's d and q current injections. The PLL-generated reference angle  $\theta$  is used for the calculation of the measured dq quantities via the dq transformation. The PLL tries to adjust  $\theta$  to follow and lock onto the phase angle of  $V_t$ . However, while this process is taking place, the injected currents, which also use the PLL's output angle as their reference, now disturb the phase of  $V_t$ . If the ac busbar's phase angle changes too quickly in the wrong direction, the PLL may not be able to catch up to it. Such a destabilizing effect of the ac network has been reported in [27]. By slowing down the PLL,  $\theta$  changes more slowly and will result in slower changes in current injections, thereby reducing the possibility of instability.

## IV. MAXIMUM POWER TRANSFER CAPABILITY AND PLL GAIN LIMITATION ON THE SCR REQUIREMENT

Power voltage instability in dc converters limits the maximum power transfer capability  $(P_{\rm max})$  of the converter for both LCC- [2] and VSC-type converters [1]. These references show that  $P_{\rm max}$  increases with higher SCR. However, their analysis does not take into account any control system dynamics, and essentially is an absolute limit.

Using the small-signal model developed before, the impact of PLL gains on the maximum power transfer is discussed in

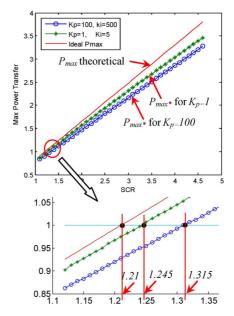


Fig. 10. Maximum power transfer capability versus SCR.

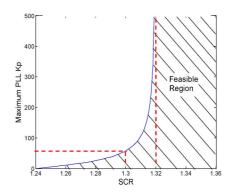


Fig. 11. SCRs versus maximum PLL gain  $K_p$  when transferring rated power.

this section. An interesting result from such a study is the determination of how close one can come to theoretical limit  $P_{max}$  when control system parameters are considered.

For a VSC rectifier, it can be shown that when the Thévenin equivalent of the ac system has a resistive component (i.e., the impedance angle is smaller than 90°),  $P_{\rm max}$  is reduced, whereas the inverter has the opposite trend [1]. The relationship between  $P_{\rm max}$  and SCR can be given as (8). Thus, the more onerous case of a VSC rectifier connected to an ac system with impedance angle of 80° is considered in this paper.

$$P_{\text{max}}(\text{p.u.}) \approx \text{SCR} \cdot \left(1 \pm \frac{R_s}{|Z_s|}\right).$$
 (8)

In (8),  $Z_s=R_s+j\omega L_s$  is the ac system's Thévenin impedance at the fundamental frequency. The "+" sign is used for inverter operation and the "–" is sign for rectifier operation.

Curves in Fig. 9, drawn for a PLL gain of  $K_p=100$ , show the relationship between the transferred power and the largest real part  $\sigma_{\max}$  of the eigenvalues, that is,  $\sigma_{\max}=\max(\mathrm{Re}(\lambda_i))$ ,  $i\in\{1,2\dots16\}$ ; for different SCRs. The curves indicate that for each SCR, there is a critical value of power  $P_{\max}$ , beyond which  $\sigma_{\max}$  goes positive indicating the onset of instability.

This value is the maximum achievable power  $P_{max^*}$  considering the system eigenvalues. Note that the curve for SCR = 1.32, crosses zero at P = 1.0 p.u., indicating that operation at rated power will not be possible for this gain with SCRs less than 1.32. More detailed plotting shows the limit is actually 1.315.

Fig. 10 shows the relationship between the SCR and maximum achievable power  $P_{\max^*}$  for PLL gains of  $K_p=1$  and  $K_p=100$ , respectively. The theoretical maximum power transfer  $P_{\max}$  as derived in [1] and given by (8) is also shown in the figure. The results show  $P_{\max^*} < P_{\max}$ , as is to be expected. The enlarged curves at lower SCR clearly show that the theoretical limit is more closely approached as the PLL gain goes to very small values. The figure shows that at the larger gain  $(K_p=100)$ , rated power can be transmitted only when the SCR is greater than 1.315. For the lower gain  $(K_p=1)$ , rated power can be transmitted even with a weaker system SCR of 1.245; which more closely approaches the theoretical minimum SCR of 1.21.

Another useful way to quantify this phenomenon is to plot the allowed range of  $K_p$  versus the SCR with the aim of transmitting rated power as shown in Fig. 11. The figure shows that a system with an SCR greater than 1.32 is always stable for any  $K_p$ , (large). However for a weaker system, that is, SCR = 1.3, the VSC system becomes unstable for PLL gain  $K_p > 60$ . It must be noted, however, that using too small of a PLL gain gives poor damping, particularly at higher SCRs [see Fig. 4(a) and (b)], and will result in poor dynamic performance. Hence, operation at such low gains is not recommended. At higher SCRs, the lower gains may also result in a slower dynamic response to setpoint changes [1], [16].

#### V. SUMMARY AND CONCLUSIONS

A linearized state-space VSC model was developed and validated using detailed electromagnetic transients simulation. The small-signal model can be used to analyze the system stability for different network impedance and control parameter values.

Results show that the gains of the PLL, particularly at low SCRs, greatly affect the operation of the VSC-HVDC converter. Operation at low SCRs approaching 1.3 (assuming an impedance angle of 80°) is very difficult. For stronger ac networks (e.g., for the case of SCR = 1.6 as shown in the paper), the VSC system works well as long as the PLL gain is kept sufficiently large to provide an adequate damping coefficient. It is also seen that the provision of local capacitive reactive power via a shunt capacitor and the decreased ac system impedance angle will further lower the stability limit.

In conventional LCC-HVDC systems, a SCR of 2.5 or higher indicates a strong system. It was not known what the situation would be for a VSC-HVDC system. This paper has attempted to answer this question and suggests that the boundary between "weak" and "strong" systems for VSC-HVDC transmission is in the range 1.3 to 1.6.

The maximum power transfer limit predicted by a power voltage stability calculation is a theoretical upper limit. Eigenvalue analysis conducted in this paper shows that this

theoretical limit can only be approached closely when the PLL gains go to very small values.

#### **APPENDIX**

The mathematical steps in the derivation of the state-variable equations are given in this section. In the derived equations, the controller gains are represented by  $\alpha$ ,  $\beta$ , and  $\lambda$  as follows:

$$\begin{cases} \beta_{01} = Ki_{P} & \begin{cases} \beta_{02} = Ki_{V} \\ \lambda_{1} = Kp_{P} \end{cases} & \begin{cases} \lambda_{2} = Kp_{V} \\ \lambda_{2} = Kp_{V} \end{cases} & \begin{cases} \alpha_{001} = \beta_{001} = \frac{1}{T_{mvd}} \\ \alpha_{002} = \beta_{001} = \frac{1}{1} \\ \alpha_{003} = \beta_{003} = \frac{1}{T_{mid}} \end{cases} \\ \lambda_{3} = Kp_{1} & \lambda_{4} = Kp_{2} \end{cases}$$

## A. Controller Equations

## 1) Measurement Equations:

$$v_{tdm} + T_{mvd} \frac{dv_{tdm}}{dt} = v_{td}, \text{ gives } \begin{cases} \frac{dx_{01}}{dt} = -\alpha_{001}x_{01} + v_{td} \\ v_{tdm} = \beta_{001}x_{01} \end{cases}$$
(A1)

$$v_{tqm} + T_{mvq} \frac{dv_{tqm}}{dt} = v_{tq}, \text{ gives } \begin{cases} \frac{dx_{02}}{dt} = -\alpha_{002}x_{02} + v_{tq} \\ v_{tqm} = \beta_{002}x_{02} \end{cases}$$
(A2)

$$i_{1dm} + T_{mid} \frac{di_{1dm}}{dt} = i_{1d}, \text{ gives } \begin{cases} \frac{dx_{03}}{dt} = -\alpha_{003}x_{03} + i_{1d} \\ i_{1dm} = \beta_{003}x_{03} \end{cases}$$
 (A3)

$$i_{1qm} + T_{miq} \frac{di_{1qm}}{dt} = i_{1q}, \text{ gives } \begin{cases} \frac{dx_{04}}{dt} = -\alpha_{004}x_{04} + i_{1q} \\ i_{1qm} = \beta_{004}x_{04} \end{cases}$$
 (A4)

#### 2) Outer Controller Equations:

$$\begin{cases} e_{P} = P_{\text{ref}} - (v_{tdm}i_{1dm} + v_{tqm}i_{1qm}) \\ i_{d}^{*} = Kp_{P} \cdot e_{P} + Ki_{P} \int e_{P}dt \end{cases}$$

$$\text{gives } \begin{cases} \frac{dx_{1}}{dt} = e_{P} \\ i_{d}^{*} = \beta_{01}x_{1} + \lambda_{1} \cdot e_{P} \end{cases}$$

$$\begin{cases} e_{V} = V_{\text{ref}} - \sqrt{v_{tdm}^{2} + v_{tqm}^{2}} \\ i_{q}^{*} = Kp_{V} \cdot e_{V} + Ki_{V} \int e_{V}dt \end{cases} \text{gives } \begin{cases} \frac{dx_{2}}{dt} = e_{V} \\ i_{q}^{*} = \beta_{02}x_{2} + \lambda_{2} \cdot e_{V} \end{cases}$$

$$(A6)$$

#### 3) Inner Controller Equations:

$$\begin{cases} e_{id} = i_d^* - i_{1dm} \\ y = v_{tdm} + i_{1qm} \cdot \omega L - v_{cd} \\ Kp_1 \cdot e_{id} + Ki_1 \int e_{id} dt = y \end{cases} \text{ gives } \begin{cases} \frac{dx_3}{dt} = e_{id} \\ y = \beta_{03} x_3 + \lambda_3 \cdot e_{id} \end{cases}$$
(A7)

$$\begin{cases} e_{iq} = i_q^* - i_{1qm} \\ y = v_{tqm} - i_{1dm} \cdot \omega L - v_{cq} \\ Kp_2 \cdot e_{iq} + Ki_2 \int e_{iq} dt = y \end{cases} \text{ gives } \begin{cases} \frac{dx_4}{dt} = e_{iq} \\ y = \beta_{04} x_4 + \lambda_4 \cdot e_{iq} \end{cases}$$
(A8)

### 4) PLL Equations:

$$\begin{cases} \frac{d\theta}{dt} = \omega \\ \frac{d\omega}{dt} = c \cdot K_P v_{tq} + K_P \frac{dv_{tq}}{dt} \end{cases}$$
 gives 
$$\frac{d}{dt} \begin{bmatrix} \theta \\ \omega \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \theta \\ \omega \end{bmatrix} + \begin{bmatrix} 0 \\ c \cdot K_P v_{tq} + K_P \frac{dv_{tq}}{dt} \end{bmatrix}. \quad (A9)$$

Equations (A1)–(A9) thus give the 10 state variables  $x_{01}, x_{02}, x_{03}, x_{04}, x_1, x_2, x_3, x_4, \theta, \omega$  associated with the VSC controller including the PLL.

## B. AC Network State-Space Equations:

Dynamic (1) for the ac network must also be linearized around the operating point. Since  $v_{sd}, v_{sq}$ , and  $v_{cd}, v_{cq}$  in (1) are not state variables, they need to be replaced by state variables. Assume that  $\alpha_0$  is the angle of the Thévenin source  $V_m$  relative to  $V_t$  (the angle reference bus, that is,  $V_t \angle 0$ ) and  $\theta$  is the angle from the PLL. The Thévenin source  $v_{sd}$  and  $v_{sq}$  can be written as (B1), where  $\delta = \theta - (\omega 0t + \alpha_0)$ 

$$v_s = \sqrt{\frac{2}{3}} v_m \cos(\omega 0t + \alpha_0) \to \begin{cases} v_{sd} = v_m \cos(\delta) \\ v_{sq} = v_m \sin(-\delta) \end{cases} .$$
 (B1)

By substituting (A1)–(A9) and (B1) into (1), we can rewrite the six dynamic equations of the ac network in (1) in the form below

$$L\frac{d}{dt}\begin{bmatrix}i_{1d}\\i_{1q}\end{bmatrix} = \begin{bmatrix}v_{td}\\v_{tq}\end{bmatrix} - \omega L\begin{bmatrix}-i_{1q}\\i_{1d}\end{bmatrix} - R\begin{bmatrix}i_{1d}\\i_{1q}\end{bmatrix} - \begin{bmatrix}\beta_{001}x_{01}\\\beta_{002}x_{02}\end{bmatrix}$$

$$-\begin{bmatrix}\lambda_{3}\beta_{003} & \omega L\beta_{004}\\-\omega L\beta_{003} & \lambda_{4}\beta_{004}\end{bmatrix}\begin{bmatrix}x_{03}\\x_{04}\end{bmatrix} + \begin{bmatrix}\beta_{03}x_{3}\\\beta_{04}x_{4}\end{bmatrix}$$

$$+\begin{bmatrix}\lambda_{3}\beta_{01}x_{1}\\\lambda_{4}\beta_{02}x_{2}\end{bmatrix} + \begin{bmatrix}\lambda_{3}\lambda_{1}P_{\text{ref}}\\\lambda_{4}\lambda_{2}v_{\text{ref}}\end{bmatrix}$$

$$-\begin{bmatrix}\lambda_{3}\lambda_{1}(\beta_{001}x_{01}\beta_{003}x_{03} + \beta_{002}x_{02}\beta_{004}x_{04})\\\lambda_{4}\lambda_{2}\sqrt{\beta_{001}^{2}}x_{01}^{2} + \beta_{002}^{2}x_{02}^{2}\end{bmatrix}$$

$$-\begin{bmatrix}\lambda_{3}\lambda_{1}(\beta_{001}x_{01}\beta_{003}x_{03} + \beta_{002}x_{02}\beta_{004}x_{04})\\\lambda_{4}\lambda_{2}\sqrt{\beta_{001}^{2}}x_{01}^{2} + \beta_{002}^{2}x_{02}^{2}\end{bmatrix}$$

$$+\begin{bmatrix}v_{m}\cos(\delta)\\v_{m}\sin(-\delta)\end{bmatrix}$$
(B3)

$$C_f \frac{d}{dt} \begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} = -\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} + \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} - \omega C_f \begin{bmatrix} -v_{tq} \\ v_{td} \end{bmatrix}.$$
 (B4)

Here,  $i_{1d}$ ,  $i_{1q}$ ,  $i_{12}$ ,  $i_{2q}$ ,  $v_{td}$ ,  $v_{tq}$  are the state variables.

## C. Full State-Space Formulation

$$\Delta \dot{X} = A\Delta X + B\Delta U \tag{C1}$$

where  $A = M^{-1}A''$  and  $B = M^{-1}B''$ . M, A'', and B'' are as follows. Any state variables, such as  $v_d$ ,  $v_q$ ,  $i_{1d}$ ,  $i_{1q}$ ,  $i_{2d}$ ,  $i_{2q}$ , are in their constant values at the operating point at which the system is linearized, as shown in equation A.

## ACKNOWLEDGMENT

The authors would like to thank Dr. D. Jacobson of Manitoba Hydro who provided many useful suggestions.

## REFERENCES

- [1] J. Z. Zhou and A. M. Gole, "VSC transmission limitations imposed by ac system strength and ac impedance characteristics," presented at the 10th Int. Conf. AC DC Power Transm. AC DC Power Transm., Birmingham, U.K., Dec. 2012.
- [2] IEEE Guide for Planning DC Links Terminating at AC Locations Having Low Short-Circuit Capacities, IEEE Standard 1204-1997,
- [3] H. Konishi, C. Takahashi, H. Kishibe, and H. Sato, "A consideration of stable operating power limits in VSC-HVDC systems," presented at the 7th Int. Conf. AC-DC Power Transm., London, U.K., 2001.
- [4] L. Zhang, L. Harnefors, and H.-P. Nee, "Interconnection of two very weak AC systems by VSC-HVDC links using power-synchronization control," *IEEE Trans. Power Syst.*, vol. 26, no. 1, pp. 344–355, Feb. 2011

- [5] C. D. Barker and N. M. Kirby, "Reactive power loading of components within a modular multi-level HVDC VSC converter," in *Proc. IEEE Elect. Power Energy Conf.*, 2011, pp. 86–90.
- [6] CIGRE Working Group B4.37, "VSC transmission," Rep. no. 269, Apr. 2005.
- [7] D. Jovcic, "Phase locked loop system for FACTS," IEEE Trans. Power Syst., vol. 18, no. 3, pp. 1116–1124, Aug. 2003.
- [8] L. Zhang, "Modeling and control of VSC-HVDC links connected to weak ac systems," Ph.D. dissertation, School Elect. Eng., Elect. Mach. Power Electron., Royal Institute of Technology, Stockholm, Sweden, 2009.
- [9] S.-K. Chung, "Phase-locked loop for grid-connected three-phase power conversion systems," in *Proc. Inst. Elect. Eng., Elect. Power Appl.*, May 2000, vol. 147, no. 3, pp. 213–219.
- [10] A. Gole, V. K. Sood, and L. Mootoosamy, "Validation and analysis of a grid control system using D-Q-Z transformation for static compensator systems," in *Proc. Can. Conf. Elect. Comput. Eng.*, Montreal, QC, Canada, Sep. 1989, pp. 745–748.
- [11] V. K. Sood, V. Khatri, and H. Jin, "Performance assessment using EMTP of two gate firing units for HVDC converters operating with weak AC systems," in *Proc. Int. Conf. Power Syst. Transients*, Lisbon, Portugal, Sep. 3–7, 1995, pp. 517–522.
- [12] G.-C. Hsich and J. C. Hung, "Phase-locked loop techniques-a survey," *IEEE Trans. Ind. Electron.*, vol. 43, no. 6, pp. 609–615, Dec. 1996.
  [13] A. Ekstrom, "High power electronics HVDC and. SVC," Elect. Power
- [13] A. Ekstrom, "High power electronics HVDC and. SVC," Elect. Power Res. Ctr., Royal Inst. Technol., Stockholm, Sweden, 1990.
- [14] A. M. Gole and V. K. Sood, "A static compensator model for use with electromagnetic transients simulation programs," *IEEE Trans. Power Del.*, vol. 5, no. 3, pp. 1398–1407, Jul. 1990.
- [15] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 263–272, Jan. 2006.
- [16] T. Midtsund, J. A. Suul, and T. Undeland, "Evaluation of current controller performance and stability for voltage source converters connected to a weak grid," in *Proc. 2nd IEEE Int. Symp. Power Electron. Distrib. Gen. Syst.*, 2010, pp. 382–388.
- [17] S. Cobreces, E. Bueno, F. J. Rodriguez, F. Huerta, and P. Rodriguez, "Influence analysis of the effects of an inductive-resistive weak grid over L and LCL filter current hysteresis controllers," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.
- [18] L. Xu and L. Fan, "Impedance-based resonance analysis in a VSC-HVDC system," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2209–2216, Oct. 2013.
- [19] K. Jin and T. H. Ortmeyer, "Application of static compensators in small AC systems with constant power loads," in *Proc. IEEE Power Eng. Soc. Summer Meeting*, Chicago, IL, USA, Jul. 21–25, 2002, vol. 1, pp. 592–596.
- [20] M. Molinas, D. Moltoni, G. Fascendini, J. A. Suul, R. Faranda, and T. M. Undeland, "Investigation on the role of power electronics controlled constant power loads for voltage support in distributed AC systems," presented at the IEEE Power Electron. Specialists Conf., Rhodes, Greece, Jun. 2008.
- [21] G. Kalcon, G. Adam, O. Anaya-Lara, S. Lo, and K. Uhlen, "Small signal stability analysis of multi-terminal VSC-based DC transmission systems," *IEEE Trans. Power Syst.*, vol. 27, no. 4, pp. 1818–1830, Nov. 2012.
- [22] K. Ogata, Modern Control Engineering, ser. Prentice-Hall Instrumentation and Controls Series. Englewood Cliffs, NJ, USA: Prentice-Hall, 1970.
- [23] A. Yazdani and R. Iravani, Voltage-Sourced Converters in Power Systems. Hoboken, NJ, USA: Wiley, 2010.
- [24] C. Schauder and H. Mehta, "Vector analysis and control of advanced static VAR compensators," *Proc. Inst. Elect. Eng., Gen. Transm. Dist.*, vol. 140, no. 4, pp. 299–306, Jul. 1993.
- [25] I. Papic, P. Zunko, D. Povh, and M. Weinhold, "Basic control of unified power flow controller," *IEEE Trans. Power Syst.*, vol. 12, no. 4, pp. 1734–1739, Nov. 1997.
- [26] P. Kundur, Power System Stability and Control. New York, USA: McGraw-Hill, 1993.
- [27] D. Dong, J. Li, D. Boroyevich, P. Mattavelli, I. Cvetkovic, and Y. Xue, "Frequency behavior and its stability of grid-interface converter in distributed generation systems," in *Proc. 27th IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 1887–1893.



**Jenny Z. Zhou** (S'01–M'03) received the B.Sc. degree in electrical engineering from the Southeast University, Nanjing, China, in 1988, and the M.Sc. (EE) and the Ph.D. degrees in electrical engineering from the University of Manitoba, Winninpeg, MB, Canada, in 2003 and 2013, respectively.

Currently, she is a Senior Supervising Engineer with Teshmont Consultants LP, Winnipeg. Her interests are system transients in interconnected ac-dc systems, HVDC transmission, and flexible ac transmission systems. She is a Registered Profes-

sional Engineer in the Province of Manitoba, Alberta, and Newfoundland and Labrador, Canada.



**Hui Ding** (S'09–M'11) was born in Shaanxi, China. He received the B.S. degree in power systems and its automation and the Ph.D. degree in power electronics and drives from North China Electric Power University, Beijing, China, in 2003 and 2010, respectively.

From 2010 to 2012, he worked on TS-EMT hybrid simulation in Power System Department of CEPRI. Currently, he is a Postdoctoral Fellow at the University of Manitoba, Winnipeg, MB, Canada, working on parallel electromagnetic transients simulation, as well as HVDC system simulation and analysis.



Shengtao Fan (M'11) was born in Shandong, China, in 1981. He received his B.Sc. degree in electronic information science and technology from Shandong University, Weihai, China, in 2002 and the Ph.D. degree in mechatronics engineering from Beihang University, Beijing, China, in 2009.

From 2009 to 2012, he worked in the Power System Department of CEPRI with an emphasis on the development of TS-EMT hybrid simulation. Currently, he is a Postdoctoral Fellow at the University of Manitoba, Winnipeg, MB, Canada, working

on the computation of electromagnetic transients in power systems.



Yi Zhang (M'05–SM'11) received the Ph.D. degree in electrical engineering from the University of Manitoba, Winnipeg, MB, Canada.

He joined RTDS Technologies, Inc., Winnipeg, in 2000 and is currently Chief Engineer/R&D Manager. His research interests are in power system analysis and real-time digital simulation. He is a registered professional engineer in the province of Manitoba, Canada.



Aniruddha M. Gole (S'77–M'82–SM'04–F'10) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 1978 and the Ph.D. degree in electrical engineering from the University of Manitoba, Winnipeg, MB, Canada, in 1982, where he is currently a Distinguished Professor.

Dr. Gole is a member of the original development team for the PSCAD/EMTDC program. He is the 2007 recipient of the IEEE PES Nari Hingorani FACTS Award. He is a Registered Professional

Engineer in the Province of Manitoba, Canada.