Stability of DC-Link Voltage as Affected by Phase Locked Loop in VSC when Attached to Weak Grid

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***Abstract*—This paper analyzes DC-link voltage stability as affected by phase locked loop (PLL) in voltage source converters (VSC) when connected to weak grid. PLL has an impact on power transferred to the grid from VSC due to active/reactive power current regulation aligned to PLL reference frame. DC-link voltage, directly related to power flows, is then affected by PLL dynamics. Interactions between PLL and DC-link voltage control are more serious in weak grid where terminal voltage, as input of PLL, becomes susceptible to power flow variations in VSC. In this paper, a system with VSC connected to infinite bus via grid impedance is studied for operating in inverter mode. Deteriorated DC-link voltage small signal stability is presented with quick PLL response as short circuit ratio (SCR) becomes significantly low. It may be possible for PLL to improve the DC-link voltage large signal stability due to its effect on power transfer.**

***Index Terms*-- DC-link voltage control, phase locked loop (PLL), small signal stability, voltage source converter (VSC), weak grid.**

I. INTRODUCTION

Voltage source converters (VSC) are widely used in power system, e.g., renewable generations, high voltage dc transmissions (HVDC), flexible ac transmission devices and inverter drive systems. With the increasing penetration of renewable generations and the great potential of VSC-HVDC transmissions, VSC performance becomes important in power system operation. Challenges are confronted with VSC operating in low short circuit ratio (SCR) AC grid [1] [2]. Causes behind have not been fully recognized. One crucial aspect for VSC performance is the stability of DC-link voltage. The VSC inner current control and external power control are realized through the regulation of VSC internal voltage produced by modulation of DC-link voltage with pulse width modulation (PWM) technique.

In researches on VSC, DC-link voltage stability has not gained much attention as that of current vector control issue. In [3], controller tuning was conducted for optimum operation and stability of DC-link voltage as outer loop of the cascaded VSC control. Oscillations of DC-link voltage were exhibited in inverter drives in [4] due to the negative resistance effect and stabilizing control was then proposed. In [5], the DC-link solution via storage devices or dumped load during the grid voltage dips was presented to satisfy the grid code for HVDC transferred offshore wind parks connected to high impedance grid. In [6], a VSC model with accurate DC-link voltage dynamics was derived and non-minimum phase property was revealed in case of rectifying mode. A DC-link voltage controller was presented based on the model derived. Beyond that, DC-link voltage stability of VSC is rarely considered in previous researches.

A significant aspect related to DC-link voltage performance is the effect of phase locked loop (PLL). PLL is used for grid synchronization. It detects VSC terminal voltage phase and produces the reference frame for VSC inner current control. It was recognized that PLL had an impact on VSC stability when connected to weak AC system [7] [8]. The conclusion was drawn from small signal modeling and time-domain simulation of VSC. Further explanations were missing. PLL was considered to have an effect on VSC power regulation when attached to high impedance AC grid [5] [9]. Ref. [5] discussed the effect of PLL dynamics on power transfer caused by distorted terminal voltage. While in [9], PLL effect on small signal stability of active power control was analyzed with voltage and power angle control strategy, which is not popular in VSC applications nowadays. Ref. [10] studied PLL effect on the overall VSC system stability including inner current loop and external power control loop from a perspective of PLL impact on system input admittance.

This paper analyzes the effect of PLL dynamics on stability of DC-link voltage in VSC integrated to weak grid. The basic considerations are as follows. For one thing, VSC terminal voltage is susceptible to power flow variations in the grid as well as in VSC. PLL will respond to terminal voltage variations. For another, DC-link voltage is controlled via the regulation of *d*-axis current aligned to the PLL reference frame. Active power transferred to the grid from VSC relies on the phase of PLL. Moreover, the bandwidth of DC-link voltage control and PLL are about in the same time scale. Dynamic interactions may be anticipated. To start with, a simple system with VSC connected to infinite bus via grid impedance is studied.

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The rest of this paper is arranged as follows. Section II briefly describes the study system. A model is derived in section III with introduction of some basics for DC-link voltage performance. Section IV analyzes the effect of PLL on DC-link voltage small signal stability. In section V, the concept of PLL impact on large disturbance stability is explored. In section VI, simulations are conducted to validate the analysis. Section VII summarizes the conclusions.

II. GRID CONNECTED VSC

In the study system, VSC is attached to infinite bus via grid impedance for operating in inverter mode, which means power is transferred from VSC to the grid. VSC control system is illustrated in Fig. 1. It includes (a) two internal current loops to control *d* and *q*-axis current components, (b) two external power control loops, which generate reference values for the inner current loops based on active and reactive power commands and (c) phase locked loop, which detects phase of terminal voltage and produces *dq*0 rotating reference frame for VSC current and power control. VSC active power control is realized by maintaining DC-link voltage to be constant, which can also be referred to as DC-link voltage control. Terminal voltage regulation is employed for reactive power control in this paper. The conventional synchronous reference frame PLL (SRF-PLL) is used for grid synchronization. The instantaneous phase is detected by projecting terminal voltage vector to PLL rotating reference frame and phase lock is realized by regulating quadrature reference voltage to be zero with a PI controller.

To focus on the problems concerned, assumptions are made as follows. (a) Only the fundamental frequency behavior of the system is considered. (b) The inner current loop dynamics are ignored for its relatively quick response compared to DC-link voltage control and PLL. (c) The filter capacitor is neglected for its mainly influencing the high frequency performance. (d) Active power input of VSC DC-link maintains constant. Under these assumptions, current injected to the grid is supposed to be equal to the reference value. VSC is modeled as controlled current source.

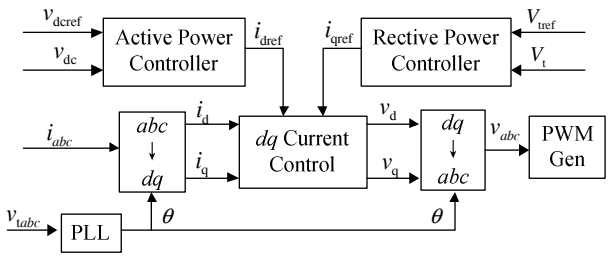

Fig. 1. VSC control system.

III. FUNDAMENTLAS FOR DC-LINK VOLTAGE CONTROL

The control block diagram of VSC system is presented Fig. 2. P_{in} and P_e stand for power injected into VSC and power transmitted to grid from VSC, regarded as VSC input power and output power, respectively. V_t and θ_t are the magnitude and phase of terminal voltage. v_{dc} is DC-link voltage. i_d and i_q are *d* and *q*-axis components of grid current in the PLL reference frame, while i_d^s and i_q^s are the components in infinite bus reference frame. The current produced in PLL reference frame is transformed to infinite bus reference frame, as expressed in (1). This is because voltages and currents have to be expressed in a common reference frame to solve the network equations. θ_{pll} is the phase that PLL leads the infinite bus, as shown in Fig. 3. ω_{pll} and ω_s are the rotating speed of PLL and the infinite bus, respectively. It can be figured out that P_e, V_t and θ_t are the functions of i_d, i_q and θ_{pll}, according to the theory of circuit. PI controllers are employed for DC-link voltage and reactive power regulation.

$$\begin{bmatrix} i_d^s \\ i_d^s \end{bmatrix} = \begin{bmatrix} \cos\theta_{pll} & -\sin\theta_{pll} \\ \sin\theta_{pll} & \cos\theta_{pll} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (1)$$

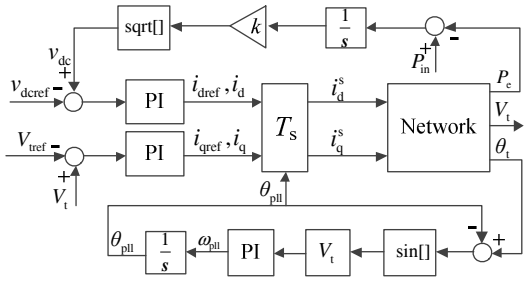

Fig. 2. Block diagram of VSC system.

The performance of DC-link voltage is similar to rotor motion of synchronous generator. DC-link capacitor is to be charged or discharge when there is unbalance between input power and output power of VSC. DC-link voltage is maintained through the regulation of power output via the control of *d*-axis current aligned to PLL reference frame with a PI controller.

A significant difference between DC-link performance and rotor motion of synchronous generator is that an extra PLL is introduced in VSC to provide reference frame for active and reactive current regulation. Current commands produced by power control loop are realized in PLL reference frame. Power transferred to the grid relies on PLL phase.

Key factors that effect DC-link performance include (a) effect of *d*-axis current i_d regulation on power output, (b) terminal voltage phase variations caused by i_d regulation, which affects PLL input, (c) phase angle between PLL and the infinite bus, which impacts i_d contribution to power output and (d) reactive power control, which influences the terminal voltage magnitude and thus influences power output. Fig. 4 shows crucial relationships for DC-link performance based on the steady state solutions of the network equations. Effect of reactive power control is not included and is not going to be discussed in this paper.

Fig. 4 (a) illustrates the plot of P_e-i_d curve with the assumption that θ_{pll} equals to θ_t by neglecting PLL dynamics and that V_t maintains constant. The value of i_d has a major impact on VSC power output. With the increase of i_d, power increases first, and then decreases. Maximum power is transmitted when the phase angle between terminal voltage and the infinite bus reaches 90 degrees. When this angle gets larger than 90 degrees, increase in i_d leads to decrease in power due to negative product of i_d current vector and infinite

bus voltage vector, as illustrated in Fig. 4 (b). $\boldsymbol{V}_s$ represents the infinite bus voltage vector.

Fig. 4 (c) shows the plot of θ_t-i_d curve with different grid impedance. i_d has an impact on terminal voltage phase. θ_t increases with the increase of i_d. With larger grid impedance, terminal voltage phase is more susceptible to i_d variations.

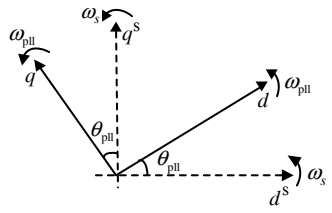

Fig. 3. Relationships between PLL and infinite bus reference frames.

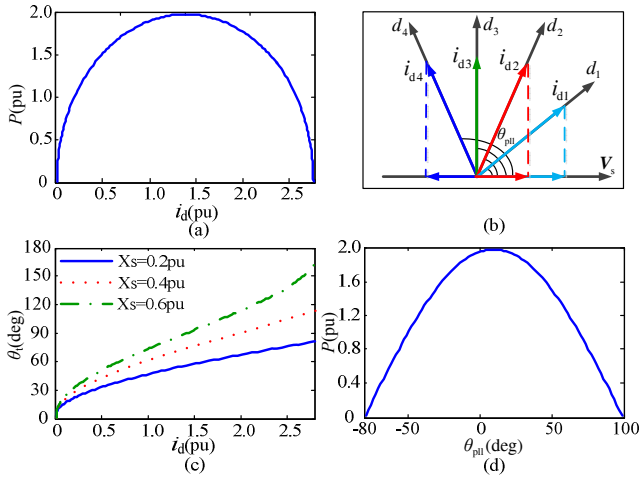

Fig. 4. (a) P_e- i_d curve. (b) i_d effect on P_e at different θ_t. (c) θ_t - i_d curve. (d) P_e-θ_{pll} curve.

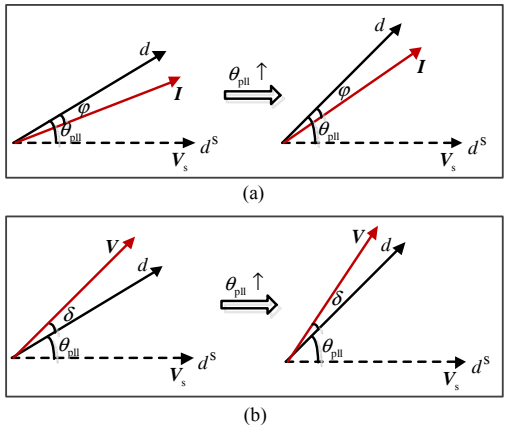

Fig. 5. Effect of PLL on power transfer with inner loop behaving as (a) controlled current source (b) controlled voltage source.

Fig. 4 (d) shows the plot of P_e-θ_{pll} curve with a given value of i_d and i_q. P_e changes with the variation of PLL phase. The given current vector lags behind PLL reference frame by about 10 degrees with a virtual power factor of 0.98. Power below the maximum can be transmitted at two different values of θ_{pll}. The normal operation is at the right value, with θ_{pll} varying from about 10 to 100 degrees in this case. Power is reduced with the increase of PLL phase in the operation range. Fig. 5 (a) explains the reason behind. With θ_{pll} getting larger, the phase angle between the regulated current vector and the infinite bus increases. Power transferred to the grid is reduced as a result.

IV. PLL Effect on Small Signal Stability of DC-Link Voltage Control

The model developed in Section III is nonlinear due to the nonlinear properties of the network and PLL. In this section, a linear model is derived for a basic understanding of PLL effect. By linearizing around the operating conditions, the system block diagram is obtained, as shown in Fig. 6. The influence of reactive power control is represented by ΔP_{e3}, which is not discussed in this paper. $\Delta\theta_{ts}$ is variation in terminal voltage phase caused by variation in infinite bus. k_1 represents the effect of Δi_d on power output, based on which DC-link voltage is regulated. PLL effect on DC-link is reflected by k_2, k_3 and k_4. k_3 is the effect of θ_{pll} variation on power output. i_d^s, the d-axis component of grid current aligned to the infinite bus reference frame, is affected by i_d variation as well as θ_{pll} variation. k_4 stands for the impact of θ_{pll} variation on i_d^s. The contribution of i_d^s variation to terminal voltage phase is represented by k_2. k_4 is relatively small. k_2 is positive while k_3 negative, as illustrated in Fig. 4 (c) and Fig. 4 (d). G_{pll} is the small signal transfer function of PLL. Expressions of k_1-k_4 are not presented in the paper due to the limited pages.

It can be observed from Fig. 6 that there exists a signal path from i_d variation to power output variation, represented by ΔP_{e2}, through the effect of PLL. The transfer function is expressed as (2). The steady state gain of $G(s)$, approximately equaling to k_2k_3, is negative due to the negative value of k_3. Power output is reduced with the increment of i_d via the effect of PLL, which is opposite to the desire of DC-link voltage regulation. It indicates that PLL dynamics has a negative influence on DC-link voltage stability.

$$G(s)=\frac{\Delta P_{e2}}{\Delta i_d}=\frac{k_2k_3G_{pll}}{1+k_2k_4G_{pll}} \tag{2}$$

The negative gain of $G(s)$ can be explained as follows. Suppose an increment in VSC power input. i_d is increased to deliver more power to the grid. θ_t increases due to i_d increment. PLL adjusts the rotation speed to catch θ_t variation. The power output is reduced because of the increased phase angle between VSC current vector and the infinite bus, as shown in Fig. 5 (a).

The effect of PLL on power output differs according to whether the inner loop of power control behaves as controlled current source or controlled voltage source. With increase of PLL phase, active power is reduced with inner current vector regulation, while it is increased with inner voltage vector regulation, employed for voltage and phase angle control, as illustrated in Fig. 5 (a) and Fig. 5 (b).

A quantitative analysis about PLL effect on DC-link voltage control is conducted. The steady state gain of $G(s)$ is greatly influenced by VSC power output as well as the value of grid impedance. This is because i_d variation can introduce larger variation in terminal voltage phase at higher power

level or with greater grid impedance. As a result, the steady state gain of $G(s)$ is increased, contributing to deteriorated system stability. Fig. 7 (a) shows the bode diagram of $G(s)$ at different power levels. ω_{cpll} is the bandwidth of PLL in pu with a base value of 10 Hz. The effect of grid impedance on $G(s)$ is similar to that of power level and thus is not presented.

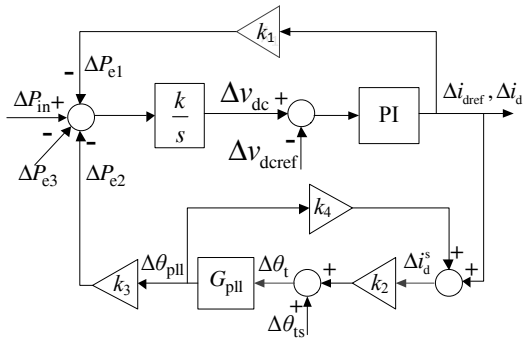

Fig. 6. Small signal model of VSC.

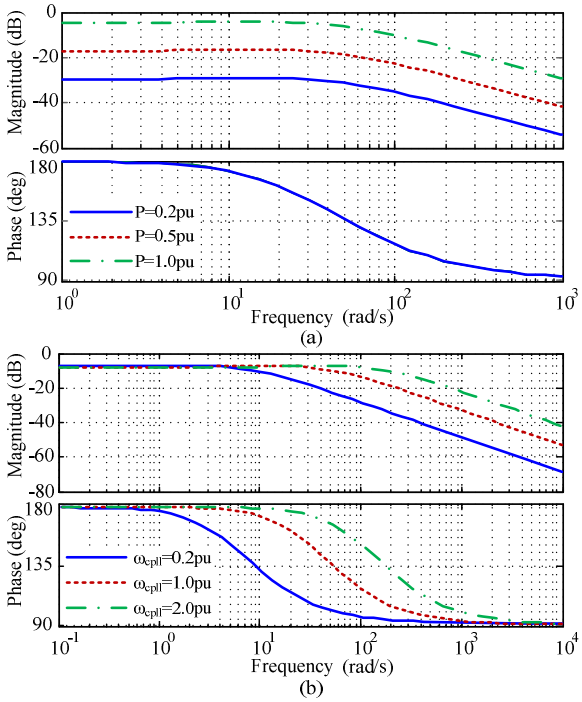

Fig. 7. Bode diagram of $G(s)$ (a) at different power level. (b) with different PLL bandwidth.

PLL bandwidth is another factor that impacts PLL effect. Slower response of PLL can filter out the terminal voltage variation and reduce the negative influence to some extent. Fig. 7 (b) shows the bode diagram of $G(s)$ with different PLL bandwidth. With lower PLL bandwidth, the gain of $G(s)$ is smaller at the DC-link voltage oscillation frequency. The negative effect of PLL is then weakened. On the other hand, at low power level, when PLL effect is insignificant, PLL quick detection of terminal voltage phase can help to reduce power imbalance on DC-link voltage under disturbance of phase shift in the grid.

In conclusion, PLL response has an effect on small signal stability of VSC DC-link voltage control in weak grid. Generally, when the phase angle between the VSC terminal voltage and the infinite bus is small, PLL influence is insignificant. When this phase angle reaches about 50 to 60 degrees with the value of operating short circuit ratio (OSCR) [11] about 1.5, quick PLL response can deteriorate DC-link voltage stability.

V. Effect of PLL on Large Disturbance Stability of DC-Link Voltage Control

Large disturbance performance of VSC is complex due to VSC interactions with the grid as well as the interactions among VSC control loops. In this paper, only some basic concepts of PLL effect on VSC DC-link voltage stability are discussed. The major concerns are how PLL dynamics influences the effect of DC-link voltage control and how PLL can improve the DC-link voltage. Assumptions are made that the control strategies have not switched and that the inner loop current control can still work under the disturbance.

As mentioned above, DC-link voltage performance is much similar to rotor motion of synchronous generator when PLL is assumed to track terminal voltage accurately. Lost of stability of DC-link stability can be anticipated under large disturbances when the charging area excesses the discharging area. Difference between VSC and the synchronous generator lies in that VSC power output is also related to the phase of PLL. DC-link voltage performance is affected by PLL dynamics.

In VSC DC-link voltage control, d-axis current is regulated to increase to transfer more power to the grid when DC-link voltage exceeds its reference value. However, as shown in Fig. 4 (b), increase of d-axis current results in power decrease when the phase angle between PLL and the infinite bus becomes larger than 90 degrees, which can be the case when the phase of terminal voltage, as input of PLL, exceeds 90 degrees during the disturbance. This is adverse to DC-link voltage stability.

If PLL is able to maintain its phase less than 90 degrees relative to that of the infinite bus despite the variation of terminal voltage phase, it can be helpful to transfer more power to the grid. Particularly, keeping a smaller phase angle, the effect of i_d regulation on power output is more significant than with larger ones, as illustrated in Fig.4 (b). In this way, DC-link voltage stability can be enhanced with increased discharging area.

To maintain proper values of the phase angle between PLL and the infinite bus may raise different requirements for PLL response under different situations. For example, when there is disturbance in VSC, slow PLL response can help to filter out PLL response to terminal voltage variation caused by VSC output. The phase angle between PLL and the infinite bus can be kept as pre-fault and power output can be increased effectively with the increase of d-axis current, which can contribute to DC-link voltage stability. While on the other hand, when there are sudden changes in the phase of the infinite bus, quick response of PLL to catch the variation is helpful to maintain the phase angle as pre-fault and benefit DC-link voltage stability.

To conclude, PLL can contribute to DC-link voltage stability. Further researches on PLL impact on DC-link stability and PLL controller tuning for DC-link stability are needed.

VI. Simulation Results

In this section, simulations are conducted in Matlab/Simulink to validate the analysis above. VSC average model is adopted with current control included. Fig. 8 is the response of DC-link voltage to small disturbance of power injected to VSC. DC-link voltage performances with various PLL bandwidths are compared for VSC operating at different OSCRs via the change of VSC power output. At high power level with power angle between terminal voltage and the infinite bus about 50 degrees, system becomes unstable as PLL bandwidth increases, as shown in Fig. 8 (a). While at low power level with the power angle about 20 degrees, the responses are not much different with various PLL bandwidths, as illustrated in Fig. 8 (b).

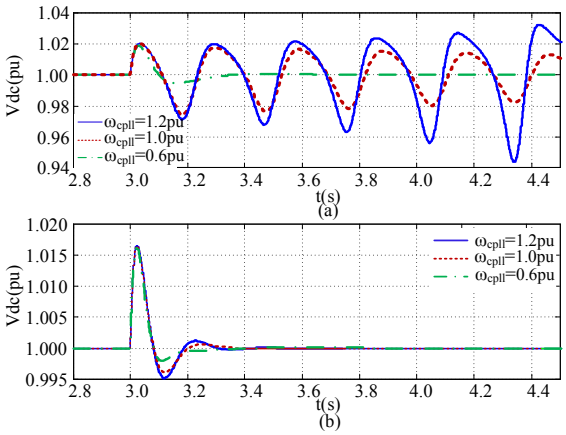

Fig. 8. DC-link voltage response to small disturbance for VSC operating at power angle of (a) 50 degrees. (b) 20 degrees.

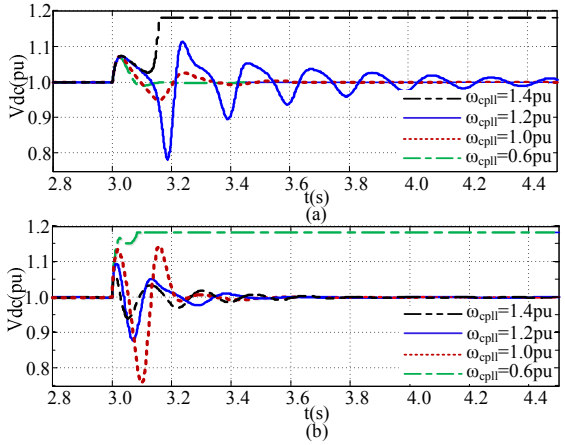

Fig. 9. DC-link voltage response to large disturbance of (a) increase of power injected to VSC. (b) phase shift of the infinite bus.

Fig. 9 shows the DC-link voltage response under large disturbances with various PLL bandwidths. Fig. 9 (a) is the response to disturbance of power injected to VSC. It can be found that DC-link voltage stability is superior with lower PLL bandwidth. Fig. 9 (b) is the response to phase shift in infinite bus. With lower PLL bandwidth, the DC-link voltage becomes unstable. The DC-link voltage is limited to 1.18 pu in simulation.

VII. Conclusion

This paper studies the effect of PLL dynamics on VSC DC-link voltage stability in weak grid. Negative effect of PLL dynamics on DC-link voltage small signal stability is figured out due to the self-tracking property of PLL in weak grid and the introduced inner current loop. When the phase angle between terminal voltage and the infinite bus reaches about 50 to 60 degrees, quick PLL response can lead to instability of DC-link voltage. PLL also has an effect on DC-link voltage large disturbance stability. With tuned PLL controllers, large disturbance stability of DC-link voltage can be guaranteed in some situations.

It seems that PLL effect on DC-link voltage stability with VSC attached to weak grid is not simply an issue of fast and precise PLL detection of terminal voltage phase. Instead, challenge lies in that in weak grid when the terminal voltage is susceptible to VSC power output, how PLL can provide the right information for VSC control to ensure system stability. The tuning of PLL controller for VSC stability in weak grid remains a question that will be further investigated.

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