Analysis of D-Q Small-Signal Impedance of Grid-Tied Inverters

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***Abstract*—This paper analyzes the small-signal impedance of three-phase grid-tied inverters with feedback control and phase-locked loop (PLL) in the synchronous reference (*d-q*) frame. The result unveils an interesting and important feature of three-phase grid-tied inverters – namely, that its *q–q* channel impedance behaves as a negative incremental resistor. Moreover, this paper shows that this behavior is a consequence of grid synchronization, where the bandwidth of the PLL determines the frequency range of the resistor behavior, and the power rating of the inverter determines the magnitude of the resistor. Advanced PLL, current, and power control strategies do not change this feature. An example shows that under weak grid conditions, a change of the PLL bandwidth could lead the inverter system to unstable conditions as a result of this behavior. Harmonic resonance and instability issues can be analyzed using the proposed impedance model. Simulation and experimental measurements verify the analysis.**

***Index Terms*—Impedance, inverters, negative resistance circuits, Nyquist stability, stability, synchronization.**

I. Introduction

GRID-TIED inverters are the key components that deliver renewable energy to the grid [1], [2]. They are typically controlled as current sources injecting current to the grid. With the increasing prevalence of renewable energy resources, power quality and stability issues induced by grid-tied inverters becomes more and more important [3]–[7]. Harmonic pollution could happen due to the interaction between inverter and grid impedance [3], [5], [7]. Large grid impedance could destabilize the inverter system [4], [8]. In order to deliver power to the grid, frequency and phase angle of the inverter output current should synchronize with grid voltage, which is usually served by phase-locked loop (PLL) [9], [10]. Some recent literatures discovered that PLL has a negative impact on the system stability [8], [11]–[14].

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In the past, instability issues of power electronics related systems are mainly believed to be caused by the negative incremental resistors of dc–dc, dc–ac converters in dc systems [15]–[17], and ac–dc converters in ac systems [18]–[20]. The negative incremental resistors are results of the output voltage regulation of these converters. Together with the high efficiency features of these converters, they become constant power loads (CPL), which consumes a fixed amount of power regardless what the supply voltage is. The input current increases when the supply voltage decreases, and vice versa. The negative resistor in combination with other components in the system can under certain conditions constitute a negative resistor oscillator, and is the origin of the system potential instability [16]–[20]. This kind instability can be analyzed by applying Nyquist stability criterion to the impedance ratio between source and load in the dc system [16]. For a three-phase ac system, no dc operation point exits in the stationary frame. By doing a transformation from the stationary frame to the synchronous reference (*d-q*) frame, a three-phase ac system becomes two coupled dc systems. Small-signal impedances in the *d-q* frame can then be derived by doing traditional linearization [8], [22], [23]. Differing from impedances of dc–dc converters, impedances of three-phase ac converters are 2×2 matrices. The CPL behavior and negative incremental resistor behavior is found in the *d–d* channel impedance (Z_{dd}) of the matrices [18], [19]. Measurement techniques and devices for *d-q* frame impedances are also developed [24]–[28]. Small-signal stability of the three-phase ac system can then be analyzed based on *d-q* impedances and generalized Nyquist Criterion (GNC) [29]–[34], [36].

Grid-tied inverters are not CPLs. They are typically controlled as current sources using single output current feedback controller or power sources using both current and power controllers as shown in Fig. 1. Instability in grid-tied inverter systems was not analyzed using the negative incremental resistor concept in the past [3]–[7]. Recently, Harnefors *et al.* [8] modeled the effect of PLL by introducing system and converter *d-q* frames. It shows that high bandwidth PLL increases the negative real part of the inverter output impedance, which could destabilize the system [8], [11]. Wen *et al.* [12] gave the full impedance model of the grid-tied inverter considering current feedback control and PLL in *d-q* frame. The model shows that PLL shapes *q–q* channel output impedance (Z_{qq}) of the grid-tied inverter as a negative incremental resistor within its bandwidth. Later on, Messo *et al.* [21] also showed the same conclusion, using a model that ignores the coupling effect between *d* channel and *q* channel. This model predicts the inverter impedances well for unity power factor application where the coupling effect can be ignored. However, for a three-phase system with reactive

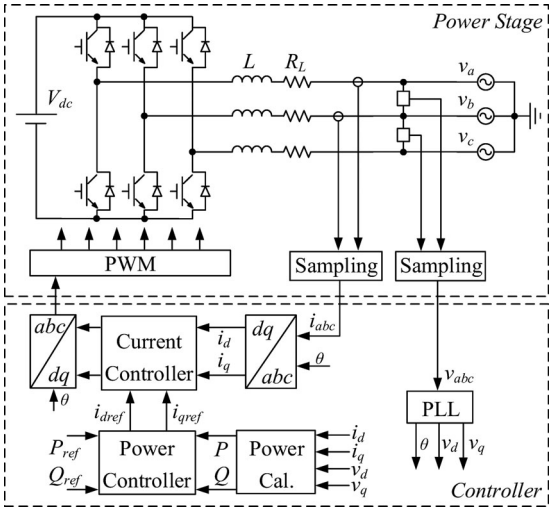

Fig. 1. Grid-tied inverter with feedback control and PLL.

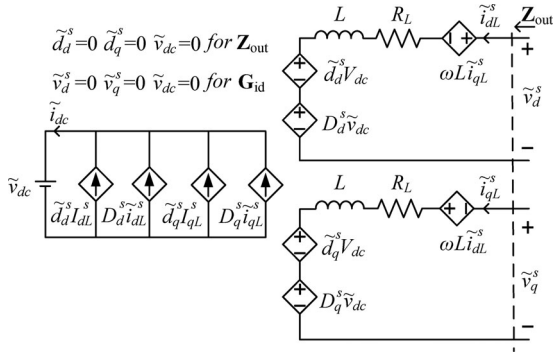

Fig. 2. Small-signal circuit model of inverter in system *d-q* frame.

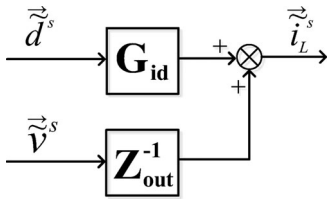

Fig. 3. Inverter power stage small-signal model.

power, the coupling effect between d and q channels is significant; this model cannot predict the impedance under this condition.

Instead, this paper proposes a full analytical model for the output impedance of the three-phase grid-tied inverter in the *d-q* frame, considering the effect of PLL, and feedback control as shown in Fig. 1. Using the proposed model, inverter small-signal impedances are characterized with different control strategies. Specifically, impedance values are shown in the form of Bode plots, which clearly demonstrate the negative resistor behavior of Z_{qq}. An analytical expression for the negative resistor is given. The model shows that a higher PLL bandwidth will produce a wider frequency range of the negative resistor, and a higher power rating of the inverter will result in a lower magnitude of the resistor. The model is verified by measured impedance. The model also indicates that under weak grid conditions, the negative incremental resistor of Z_{qq} could lead the system to unstable conditions.

Small-signal impedances of power converters are the linearization around their dc operation points. Recently, small-signal impedances and stability analysis of three-phase converters were also developed in the stationary frame using harmonic linearization on ac signals [5], [31], [35]. This paper focuses on the traditional *d-q* impedance analysis in the synchronous reference frame.

The rest of this paper includes seven sections. Section II shows the power stage small-signal model of the grid-tied inverter. Section III models the effect of PLL on the inverter impedances. Section IV models the inverter impedances with current feedback control. Section V models the effect of power feedback control on the inverter impedances. Section VI shows the stability analysis using the proposed model. Section VII shows the experimental verification of the proposed model. Section VIII is the conclusion.

II. Power Stage Small-Signal Model

Fig. 2 shows the small-signal circuit model of the grid-tied inverter power stage in the system *d-q* frame [22], [18]. Assume the input of the grid-tied inverter is supplied by a stiff dc source, which could be a dc–dc converter for solar application or an ac–dc converter for wind application. Then, the dynamic from the dc input can be neglected. The small-signal circuit model then can be represented by the transfer function matrix flow chart shown in Fig. 3. $\mathbf{G_{id}}$ is the transfer function matrix from duty ratio vector $\vec{\tilde{d}}^s$ to inductor current vector $\vec{\tilde{i}}_L^s$,$\mathbf{Z_{out}}$ is the output impedance of the power stage.

The open-loop output impedance without PLL can be derived by forcing perturbations of the duty ratio and dc voltage to zero as shown in Fig. 2. The expression of the power stage output impedance is

$$\mathbf{Z_{out\_ol}} = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} = \begin{bmatrix} Ls + R_L & -\omega L \\ \omega L & Ls + R_L \end{bmatrix}. \quad (1)$$

Notice that impedance of the three-phase converter in the *d-q* frame is a 2×2 matrix. Z_{dd} represents the voltage response in d channel when d channel current is perturbed. Z_{qq} represents the q channel voltage response when q channel current is perturbed. Equation (1) shows that Z_{dd} and Z_{qq} are the same as the impedance of the inverter ac inductor. Z_{dq} and Z_{qd} represent the coupling effect between the d and q channel.

The transfer function matrix between the duty-ratio vector and inductor current vector can be derived by forcing perturbations of grid and dc voltage to zero as shown in Fig. 2. The expression of $\mathbf{G_{id}}$ is

$$\mathbf{G_{id}} = \frac{-V_{dc}}{(Ls + R_L)^2 + (\omega L)^2} \begin{bmatrix} Ls + R_L & \omega L \\ -\omega L & Ls + R_L \end{bmatrix}. \quad (2)$$

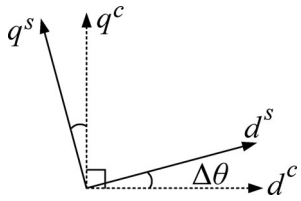

Fig. 4. System and controller *d-q* frames.

III. Influence of PLL

Output impedance of a dc–dc converter is influenced by its power stage parameters and feedback controller [16]. Differing from a dc–dc converter, a grid-tied converter usually needs PLL to synchronize with the grid [10]. The traditional PLL and feedback control of the grid-tied inverter are formulated also in the *d-q* frame. Recently, other synchronization and feedback control strategies were also developed. These included strategies such as power synchronization [37], controller in stationary frame [2] and even a control of grid-tied inverter as a synchronous generator [38]. Note that these topics are out of the scope of this paper. Because of PLL, the inverter system has two *d-q* frames: one is the system *d-q* frame, and another is the controller *d-q* frame [8] as shown in Fig. 4. Grid voltage defines the system *d-q* frame. The controller *d-q* frame is defined by the PLL, which estimates the frequency and angle of grid voltage to find the position of the system *d-q* frame. In a steady state, the controller *d-q* frame is aligned with the system *d-q* frame. When small-signal perturbations are added to the grid voltage, the position of the system *d-q* frame is changed. The controller *d-q* frame is no longer aligned with the system *d-q* frame because of the PLL dynamics (PI regulator of PLL). The angle between two *d-q* frames is $\Delta\theta$ as shown in Fig. 4. Voltage and current vectors in the system *d-q* frame are rotated to the controller *d-q* frame for feedback control by matrix $\mathbf{T}_{\Delta\theta}$. The duty-cycle commands generated by feedback control are then rotated to the system *d-q* frame by the inverse of matrix $\mathbf{T}_{\Delta\theta}$ to control the power semiconductors

$$\mathbf{T}_{\Delta\theta} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix} \tag{3}$$

$$\vec{v}^c = \mathbf{T}_{\Delta\theta}\vec{v}^s, \vec{i}^c = \mathbf{T}_{\Delta\theta}\vec{i}^s, \vec{d}^s = \mathbf{T}_{\Delta\theta}^{-1}\vec{d}^c. \tag{4}$$

Small-signal perturbations of the system voltage propagate to the PLL output angle, and further to the current and duty-ratio vector in the controller *d-q* frame. Perturbations then go to the voltage generated by the inverter power stage, and finally, to the output current of the inverter [12]. This means PLL dynamic influences the output impedance of the grid-tied inverter.

In order to model the small-signal propagation path through PLL, transfer function matrices $\mathbf{G}^{\mathbf{v}}_{\mathbf{PLL}}$, $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$, and $\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$ are defined. $\mathbf{G}^{\mathbf{v}}_{\mathbf{PLL}}$ models the small-signal perturbation path from the system voltage to voltage in the controller *d-q* frame. $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$ models the small-signal perturbation path from system voltage to duty cycle in the controller *d-q* frame.$\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$ models the small-signal perturbation path from the system voltage to current

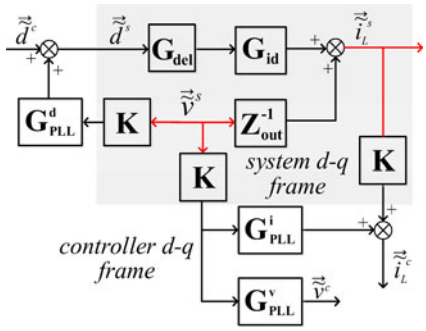

Fig. 5. Inverter small-signal model with PLL.

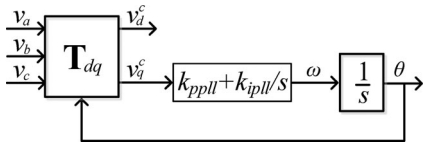

Fig. 6. SRF PLL.

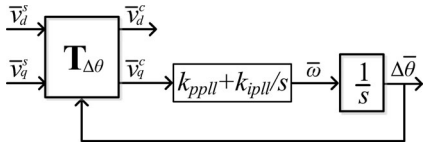

Fig. 7. Average model of SRF PLL.

in the controller *d-q* frame. Fig. 5 shows the transfer function matrix flow chart representation of a grid-tied inverter small-signal model with PLL. $\mathbf{K}$ is the filter transfer function matrix for voltage and current signals conditioning. $\mathbf{G_{del}}$ represents the time delay ($T_{\rm del}$) due to digital control and PWM [39]. Notice that, in the model shown in Fig. 5, adding $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$ is the major difference to the model shown in [8]

$$\mathbf{K} = \begin{bmatrix} \dfrac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} & 0 \\ 0 & \dfrac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \end{bmatrix} \tag{5}$$

$$\mathbf{G_{del}} = \begin{bmatrix} \dfrac{1-0.5T_{\rm del}s}{1+0.5T_{\rm del}s} & 0 \\ 0 & \dfrac{1-0.5T_{\rm del}s}{1+0.5T_{\rm del}s} \end{bmatrix} \tag{6}$$

$$\mathbf{T}_{dq} = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\theta) & \cos\left(\theta-\frac{2}{3}\pi\right) & \cos\left(\theta+\frac{2}{3}\pi\right) \\ -\sin(\theta) & -\sin\left(\theta-\frac{2}{3}\pi\right) & -\sin\left(\theta+\frac{2}{3}\pi\right) \end{bmatrix}. \tag{7}$$

To derive$\mathbf{G}^{\mathbf{v}}_{\mathbf{PLL}}$, $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$, and$\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$, the PLL strategy in the synchronous reference (*d-q*) frame (SRF) [9] shown in Fig. 6 is considered first. The SRF transformation matrix is shown in (7).

In the *d-q* frame, the average model of the PLL is shown in Fig. 7, and the derivation begins from the steady-state relationship of variables in two frames as shown in the following

equation:

$$\vec{V}^c = \vec{V}^s, \vec{I}^c = \vec{I}^s, \vec{D}^s = \vec{D}^c. \tag{8}$$

The aforementioned equation indicates that the angle between vectors in the controller frame and the vector in system frame is 0; using the rotation matrix $\mathbf{T}_{\Delta\theta}$, (8) can be rewritten as

$$\begin{aligned}\vec{V}^c &= \begin{bmatrix}\cos(0) & \sin(0)\\ -\sin(0) & \cos(0)\end{bmatrix}\vec{V}^s\\ \vec{I}^c &= \begin{bmatrix}\cos(0) & \sin(0)\\ -\sin(0) & \cos(0)\end{bmatrix}\vec{I}^s\\ \vec{D}^s &= \begin{bmatrix}\cos(0) & -\sin(0)\\ \sin(0) & \cos(0)\end{bmatrix}\vec{D}^c.\end{aligned} \tag{9}$$

Add small-signal perturbation to (9)

$$\begin{bmatrix}V_d^c+\tilde{v}_d^c\\ V_q^c+\tilde{v}_q^c\end{bmatrix} = \begin{bmatrix}\cos(0+\Delta\tilde{\theta}) & \sin(0+\Delta\tilde{\theta})\\ -\sin(0+\Delta\tilde{\theta}) & \cos(0+\Delta\tilde{\theta})\end{bmatrix} \begin{bmatrix}V_d^s+\tilde{v}_d^s\\ V_q^s+\tilde{v}_q^s\end{bmatrix}. \tag{10}$$

By doing a small angle approximation of trigonometric functions, and canceling the steady-state values, the relationship between voltage vectors in the controller frame, system frame, and PLL output angle can be derived as

$$\begin{bmatrix}V_d^c+\tilde{v}_d^c\\ V_q^c+\tilde{v}_q^c\end{bmatrix} \approx \begin{bmatrix}1 & \Delta\tilde{\theta}\\ -\Delta\tilde{\theta} & 1\end{bmatrix}\cdot\begin{bmatrix}V_d^s+\tilde{v}_d^s\\ V_q^s+\tilde{v}_q^s\end{bmatrix} \tag{11}$$

$$\begin{bmatrix}\tilde{v}_d^c\\ \tilde{v}_q^c\end{bmatrix} \approx \begin{bmatrix}\tilde{v}_d^s+V_q^s\Delta\tilde{\theta}\\ -V_d^s\Delta\tilde{\theta}+\tilde{v}_q^s\end{bmatrix}. \tag{12}$$

Recall that PLL output angle is

$$\Delta\tilde{\theta} = \tilde{v}_q^c\cdot tf_{\mathrm{PLL}}\cdot\frac{1}{s} \tag{13}$$

where

$$tf_{\mathrm{PLL}} = k_{p\mathrm{pll}} + k_{i\mathrm{pll}}\frac{1}{s}. \tag{14}$$

Substitute (13) into (12), the following equation shows the relation between PLL output angle and q channel voltage:

$$\Delta\tilde{\theta} = \frac{tf_{\mathrm{PLL}}}{s+V_d^s tf_{\mathrm{PLL}}}\tilde{v}_q^s. \tag{15}$$

Define G_{PLL} as

$$G_{\mathrm{PLL}} = \frac{tf_{\mathrm{PLL}}}{s+V_d^s tf_{\mathrm{PLL}}}. \tag{16}$$

Then

$$\Delta\tilde{\theta} = G_{\mathrm{PLL}}\tilde{v}_q^s. \tag{17}$$

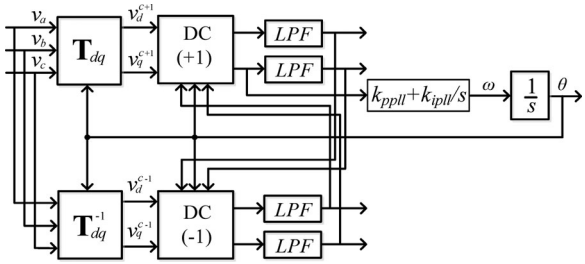

Fig. 8. DDSRF PLL.

For voltage

$$\begin{bmatrix}\tilde{v}_d^c\\ \tilde{v}_q^c\end{bmatrix} \approx \begin{bmatrix}\tilde{v}_d^s+V_q^s G_{\mathrm{PLL}}\tilde{v}_q^s\\ -V_d^s G_{\mathrm{PLL}}\tilde{v}_q^s+\tilde{v}_q^s\end{bmatrix} = \begin{bmatrix}1 & V_q^s G_{\mathrm{PLL}}\\ 0 & 1-V_d^s G_{\mathrm{PLL}}\end{bmatrix}\cdot\begin{bmatrix}\tilde{v}_d^s\\ \tilde{v}_q^s\end{bmatrix}. \tag{18}$$

Then, $\mathbf{G^v_{PLL}}$ is defined as

$$\mathbf{G^v_{PLL}} = \begin{bmatrix}1 & V_q^s G_{\mathrm{PLL}}\\ 0 & 1-V_d^s G_{\mathrm{PLL}}\end{bmatrix}. \tag{19}$$

For duty ratio, similar small-signal analysis can be done, which yields

$$\begin{bmatrix}\tilde{d}_d^s\\ \tilde{d}_q^s\end{bmatrix} \approx \begin{bmatrix}0 & -D_q^s G_{\mathrm{PLL}}\\ 0 & D_d^s G_{\mathrm{PLL}}\end{bmatrix}\cdot\begin{bmatrix}\tilde{v}_d^s\\ \tilde{v}_q^s\end{bmatrix} + \begin{bmatrix}\tilde{d}_d^c\\ \tilde{d}_q^c\end{bmatrix}. \tag{20}$$

Then, $\mathbf{G^d_{PLL}}$ is defined as

$$\mathbf{G^d_{PLL}} = \begin{bmatrix}0 & -D_q^s G_{\mathrm{PLL}}\\ 0 & D_d^s G_{\mathrm{PLL}}\end{bmatrix}. \tag{21}$$

A similar equation can be derived for the inductor current as follows:

$$\begin{bmatrix}\tilde{i}_d^c\\ \tilde{i}_q^c\end{bmatrix} \approx \begin{bmatrix}0 & I_q^s G_{\mathrm{PLL}}\\ 0 & -I_d^s G_{\mathrm{PLL}}\end{bmatrix}\cdot\begin{bmatrix}\tilde{v}_d^s\\ \tilde{v}_q^s\end{bmatrix} + \begin{bmatrix}\tilde{i}_d^s\\ \tilde{i}_q^s\end{bmatrix}. \tag{22}$$

$\mathbf{G^i_{PLL}}$ is defined as

$$\mathbf{G^i_{PLL}} = \begin{bmatrix}0 & I_q^s G_{\mathrm{PLL}}\\ 0 & -I_d^s G_{\mathrm{PLL}}\end{bmatrix}. \tag{23}$$

Solving the equations represented by Fig. 5, the output impedance of an inverter with PLL working on open loop is

$$\mathbf{Z_{out\_ol\_PLL}} = \left(\mathbf{Z_{out}^{-1}} + \mathbf{G_{id}G_{del}G^d_{PLL}K}\right)^{-1}. \tag{24}$$

One important issue in PLL design is the double line frequency ripple caused by three-phase unbalance. Decoupled double SRF (DDSRF) [40], as shown in Fig. 8, is an effective strategy to migrate the double line frequency ripple. The dynamic of the decoupling term is modeled as the transfer function matrix $\mathbf{H}$ in Fig. 9. The expression of $\mathbf{H}$ can be found in [41], and is

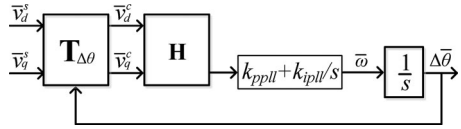

Fig. 9. Average model of DDSRF PLL.

shown from (25) to (29).

$$\mathbf{H} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \tag{25}$$

where

$$H_{11} = H\left(s^3 + 2\omega_f s^2 + 4\omega^2 s + 4\omega_f \omega^2\right) \tag{26}$$

$$H_{22} = H_{11}\frac{s+\omega_f}{\omega_f} \tag{27}$$

$$H_{12} = -H_{21} = -H(2\omega_f \omega s) \tag{28}$$

$$H = \frac{\omega_f}{s^4 + 4\omega_f s^3 + 4\left(\omega_f^2 + \omega^2\right)s^2 + 8\omega_f \omega^2 s + 4\omega_f^2 \omega^2}. \tag{29}$$

The low-pass filter (LPF) in Fig. 8 is

$$\mathrm{LPF} = \frac{\omega_f}{s+\omega_f}. \tag{30}$$

With DDSRF, the relation between PLL output angle and grid voltage is

$$\Delta\tilde{\theta} = G_{\mathrm{PLL1}}\tilde{v}_d^s + G_{\mathrm{PLL2}}\tilde{v}_q^s \tag{31}$$

where

$$G_{\mathrm{PLL1}} = \frac{tf_{\mathrm{PLL}}H_{21}}{s + tf_{\mathrm{PLL}}\left(V_d^s H_{22} - V_q^s H_{21}\right)} \tag{32}$$

$$G_{\mathrm{PLL2}} = \frac{tf_{\mathrm{PLL}}H_{22}}{s + tf_{\mathrm{PLL}}\left(V_d^s H_{22} - V_q^s H_{21}\right)}. \tag{33}$$

Then, $\mathbf{G^v_{PLL}}$, $\mathbf{G^d_{PLL}}$, and $\mathbf{G^i_{PLL}}$ become $\mathbf{G^v_{DDPLL}}$, $\mathbf{G^d_{DDPLL}}$, and $\mathbf{G^i_{DDPLL}}$ with DDSRF PLL, and they are

$$\mathbf{G^v_{DDPLL}} = \begin{bmatrix} 1 + V_q^s G_{\mathrm{PLL1}} & V_q^s G_{\mathrm{PLL2}} \\ -V_d^s G_{\mathrm{PLL1}} & 1 - V_d^s G_{\mathrm{PLL2}} \end{bmatrix} \tag{34}$$

$$\mathbf{G^d_{DDPLL}} = \begin{bmatrix} -D_q^s G_{\mathrm{PLL1}} & -D_q^s G_{\mathrm{PLL2}} \\ D_d^s G_{\mathrm{PLL1}} & D_d^s G_{\mathrm{PLL2}} \end{bmatrix} \tag{35}$$

$$\mathbf{G^i_{DDPLL}} = \begin{bmatrix} I_q^s G_{\mathrm{PLL1}} & I_q^s G_{\mathrm{PLL2}} \\ -I_d^s G_{\mathrm{PLL1}} & -I_d^s G_{\mathrm{PLL2}} \end{bmatrix}. \tag{36}$$

When DDSRF PLL is used, $\mathbf{G^d_{PLL}}$ is replaced by $\mathbf{G^d_{DDPLL}}$ in (24).

IV. Impedance With Current Control and PLL

The current controller can be implemented in either synchronous frame or stationary frame. Stationary frame current regulators can be transformed to synchronous frame using the transformation provided by [42]. Modeling of the impedance of a voltage source converter with a stationary frame current regulator is shown in [43]. The influence of different current regulators will not be elaborated upon; only the current controller in synchronous frame is considered in this paper. Fig. 10 shows the small-signal model of the grid-tied inverter with current feedback control. The current controller matrix is $\mathbf{G_{ci}}$. $\mathbf{G_{dei}}$ is the decoupling term

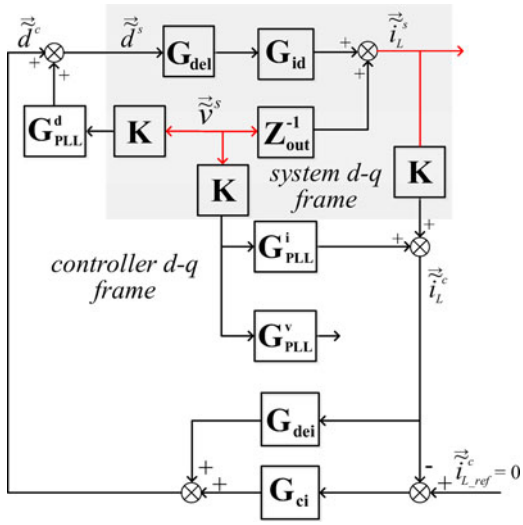

Fig. 10. Small-signal model with PLL and current feedback control.

$$\mathbf{G_{ci}} = \begin{bmatrix} k_{pi} + \frac{k_{ii}}{s} & 0 \\ 0 & k_{pi} + \frac{k_{ii}}{s} \end{bmatrix} \tag{37}$$

$$\mathbf{G_{dei}} = \begin{bmatrix} 0 & -\frac{3\omega L}{V_{\mathrm{dc}}} \\ \frac{3\omega L}{V_{\mathrm{dc}}} & 0 \end{bmatrix}. \tag{38}$$

Solving the equations represented by Fig. 10, the output impedance of a grid-tied inverter system with PLL working under a closed-loop condition is

$$\mathbf{Z_{out\_il\_PLL}} = \left(\mathbf{Z_{out}^{-1}} + \mathbf{G_{id}G_{del}}\left(\left(-\mathbf{G_{ci}} + \mathbf{G_{dei}}\right)\mathbf{G^i_{PLL}} + \mathbf{G^d_{PLL}}\right)\mathbf{K}\right)^{-1} \cdot \left(\mathbf{I} + \mathbf{G_{id}G_{del}}\left(\mathbf{G_{ci}} - \mathbf{G_{dei}}\right)\mathbf{K}\right). \tag{39}$$

When DDSRF PLL is used, $\mathbf{G^d_{PLL}}$ is replaced by $\mathbf{G^d_{DDPLL}}$ and $\mathbf{G^i_{PLL}}$ is replaced by $\mathbf{G^i_{DDPLL}}$ in (39).

Table I in the Appendix shows the parameters of the inverter prototype system. Using these parameters and (24), Fig. 11 shows the Bode plot of the inverter power stage open-loop output impedance ($\mathbf{Z_{out\_ol}}$) over plotted with output impedances open loop with PLL ($\mathbf{Z_{out\_ol\_PLL}}$). Clearly, Z_{qq} of $\mathbf{Z_{out\_ol\_PLL}}$ is shaped as a negative resistor at low frequency. Using these parameters and (39), Fig. 12 shows the Bode plot of inverter output impedances with current feedback control and different PLL designs. The impedances are calculated up to half switching

TABLE I
PARAMETERS OF GRID-TIED INVERTER PROTOTYPE

Symbol	Description	Value
$V_{\rm dc}$	Inverter input dc voltage	270 V
V_d^s	D channel grid voltage	99.6 V
V_q^s	Q channel grid voltage	0 V
i_{dref}	D channel current reference	–11 A
i_{qref}	Q channel current reference	0 A
ω	Line frequency	$2\pi\times400$ rad/s
L	Inductance of inverter output inductor	970 μH
R_L	Resistance of inverter inductor self-resistor	120 mΩ
$f_{\rm sw}$	Switching frequency	20 kHz
k_{pi}	Proportional gain of current controller	0.023
k_{ii}	Integrator gain of current controller	25.59
ω_n	Natural frequency of signal conditioning filter	1.23e6 rad/s
ξ	Damping factor of signal conditioning filter	4.74e-13
$T_{\rm del}$	Time delay due to digital control and PWM	$1.5/f_{sw}$
ω_f	Cut off frequency of LPF in DDSRF PLL	1777 rad/s
k_{ppll}	Proportional gain of inverter PLL	
k_{ipll}	Integral gain of inverter PLL	

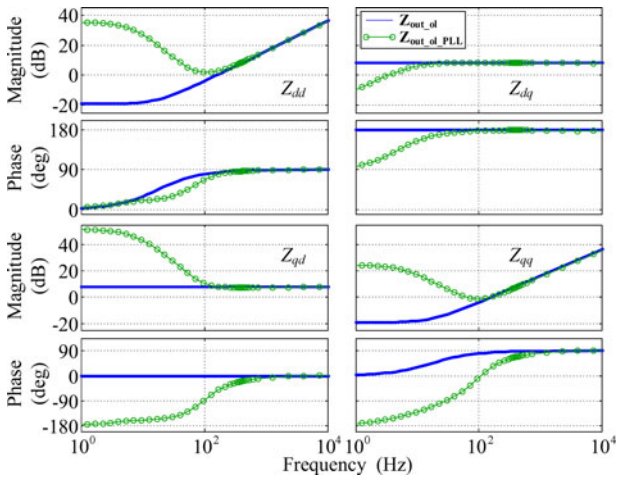

Fig. 11. VSI power stage impedances ($\mathbf{Z_{out\_ol}}$) and open loop with PLL impedances ($\mathbf{Z_{out\_PLL}}$).

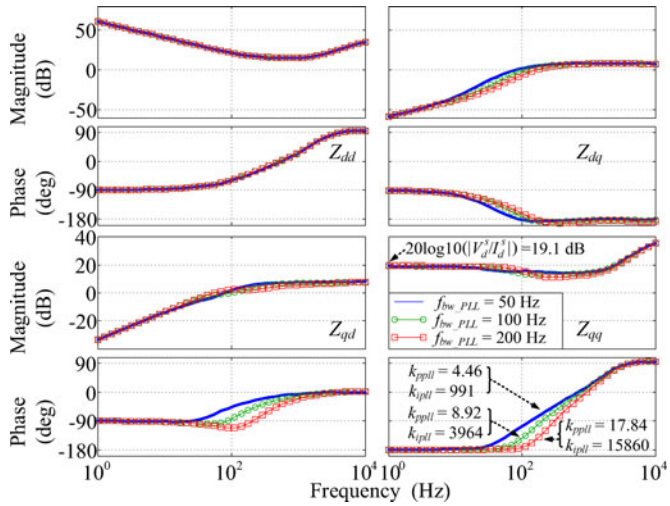

Fig. 12. Impedances of inverter with current control and different PLL bandwidth.

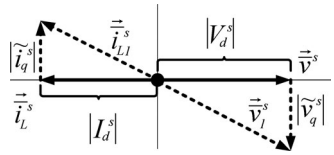

Fig. 13. Phasor diagram of inverter with current feedback control and PLL when perturbation happens in q channel.

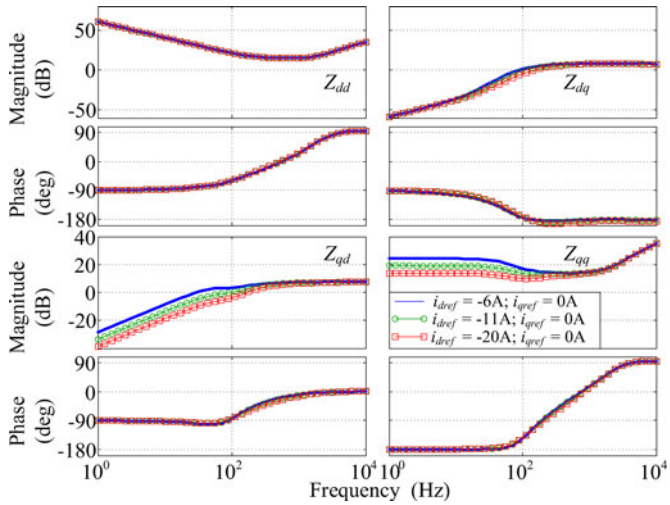

Fig. 14. Impedances of inverter with current control and different $i_{\rm dref}$.

frequency where it is valid to do so

$$Z_{qq} = -\frac{|\tilde{v}_q^s|}{|\tilde{i}_q^s|} = -\frac{|V_d^s|}{|I_d^s|}. \tag{40}$$

As it can be observed in Fig. 12, Z_{dd} shows the current source behavior. In low frequency range, it is shaped by the current controller integrator; in high frequency range, Z_{dd} is the impedance of the ac inductor. Z_{dq} and Z_{qd} are very small within the current controller bandwidth because of unity power factor control. In high frequency range, they behave as the power stage impedance value as shown in (1). Z_{qq} behaves as a negative incremental resistance within PLL bandwidth. Three different PLL designs in which bandwidth ($f_{\rm bw\_PLL}$) varies from 50 to 200 Hz (line frequency is set to be 400 Hz in order to allow a wide range of PLL bandwidth) are chosen to show the influence of PLL. The results show that a higher PLL bandwidth case yields a wider frequency range of negative resistance behavior. The magnitude of the resistance is related to the power rating of the inverter. Especially, as shown in Fig. 13, the current vector of the inverter is synchronized with the grid voltage vector, which is aligned in d channel to inject real power to the grid. When voltage disturbance happens in q channel, the voltage vector $\vec{v}^{\,s}$ becomes $\vec{v}_1{}^{\,s}$. Because of PLL, the current vector will rotate to keep synchronization with the voltage vector. Meanwhile, the current controller keeps current magnitude in d channel unchanged. Then, current vector $\vec{i}_L{}^{\,s}$ becomes $\vec{i}_{L1}{}^{\,s}$ due to the q channel voltage perturbation. Notice that the small-signal response of q channel current is in the opposite direction of q channel voltage perturbation, so, from Fig. 13, Z_{qq} can be calculated by (40)

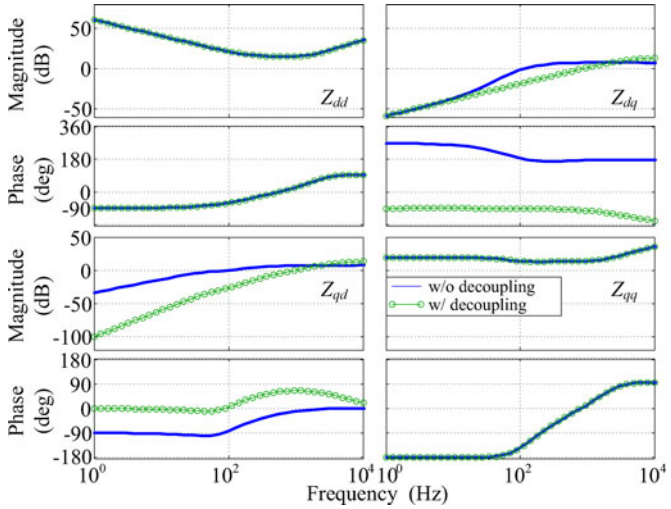

Fig. 15. Impedances of inverter with and without decoupling control.

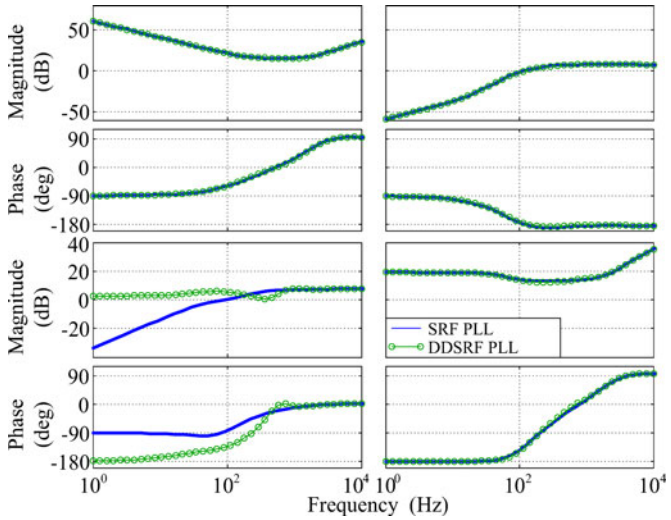

Fig. 16. Impedances with current control and different PLL strategies.

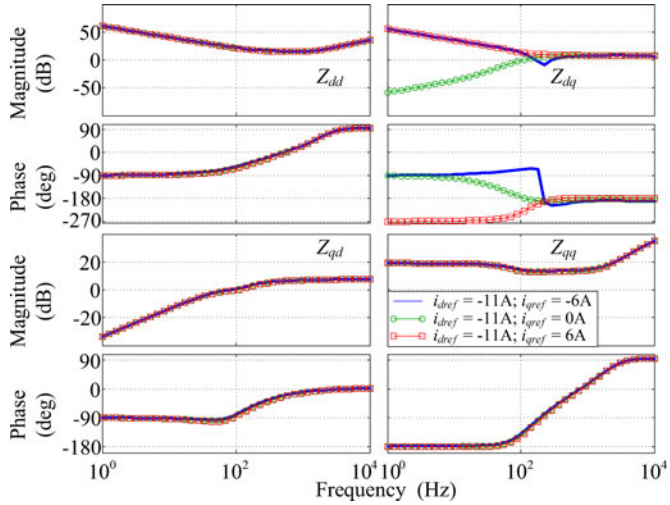

Fig. 17. Impedances of inverter with different reactive current injections.

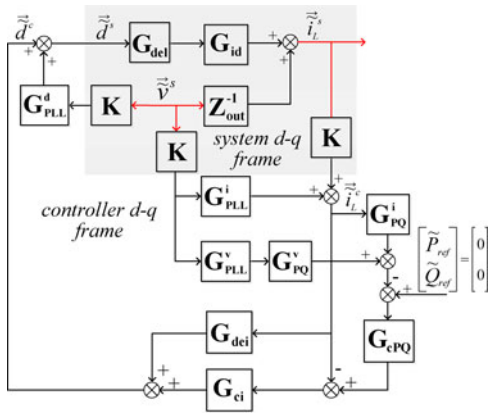

Fig. 18. Inverter small-signal model with PLL, current and power control.

within the bandwidth of PLL. This conclusion is also verified by the magnitude of Z_{qq} in low frequency as shown in Fig. 12. According to (40), an inverter with a high current rating has low impedance in *q*-*q* channel; this is shown in Fig. 14, in which impedances with three different *d* channel current references are plotted.

Fig. 15 shows the impedances of the inverter with and without decoupling control. With decoupling control, Z_{dq} and Z_{qd} are reduced. This is expected, because decoupling control reduces the coupling between *d* and *q* channel, which is reflected by Z_{dq} and Z_{qd}. The use of decoupling control does not change the negative resistance behavior of Z_{qq}.

Fig. 16 shows the impedance with different PLL strategies, which indicates that use of DDSRF PLL does not change the negative resistance behavior of Z_{qq}.

The grid-tied inverter can inject reactive current to support the grid. Fig. 17 shows the impedance of the grid-tied inverter with different reactive power injections. The blue line shows the impedance of the capacitive power injection case; the green line shows the impedance of no reactive power injection, and the red line shows the inductive power injection case. Notice that reactive power injection will increase the impedance of cross-coupling term Z_{dq}; the rest of the impedances are the same with the unit power factor case. The negative resistance feature remains unchanged when the grid-tied inverter injects reactive power to the grid.

V. Influence of Power Flow Control Loop

On top of the current controller, a power flow controller can be added to control the real and reactive power accurately generated by the inverter. The small-signal model is shown in Fig. 18 for the power flow control case. $\mathbf{G_{cPQ}}$ is the transfer function matrix of the power flow controller

$$\mathbf{G_{cPQ}} = \begin{bmatrix} k_{pPQ} + \dfrac{k_{iPQ}}{s} & 0 \\ 0 & k_{pPQ} + \dfrac{k_{iPQ}}{s} \end{bmatrix}. \tag{41}$$

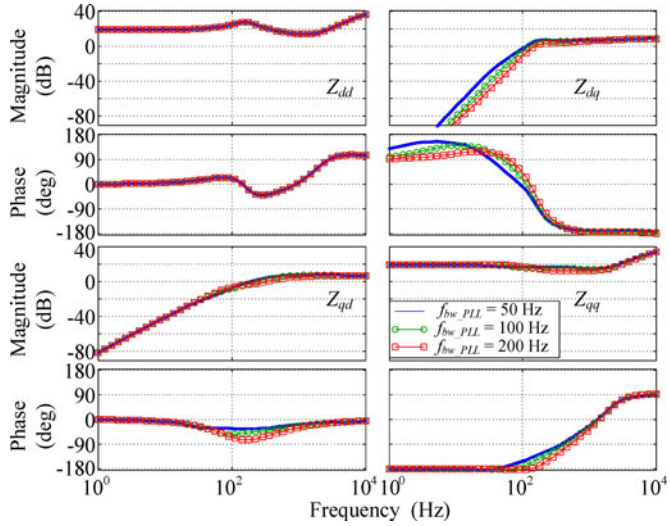

Fig. 19. Impedances of inverter with PLL and power feedback control.

TABLE II
PARAMETERS OF CURRENT AND POWER FEEDBACK CONTROLLER

Symbol	Description	Value
k_{pi}	Proportional gain of current controller	0.023
k_{ii}	Integrator gain of current controller	51.18
k_{pPQ}	Proportional gain of power controller	0.0028
k_{iPQ}	Integrator gain of power controller	7
P_{ref}	Real power reference	–1150 W
Q_{ref}	Reactive power reference	0 Var

$\mathbf{G^i_{PQ}}$ and $\mathbf{G^v_{PQ}}$ are small-signal transfer function matrices of power calculation in *d-q* frame

$$\begin{cases} P = i_d^c v_d^c + i_q^c v_q^c \\ Q = -i_d^c v_q^c + i_q^c v_d^c. \end{cases} \tag{42}$$

By doing linearization to (42), $\mathbf{G^i_{PQ}}$ and $\mathbf{G^v_{PQ}}$ are derived as follows:

$$\mathbf{G^i_{PQ}} = \begin{bmatrix} V_d^s & V_q^s \\ -V_q^s & V_d^s \end{bmatrix} \tag{43}$$

$$\mathbf{G^v_{PQ}} = \begin{bmatrix} I_d^s & I_q^s \\ I_q^s & -I_d^s \end{bmatrix}. \tag{44}$$

Solving the equations represented by Fig. 18, the output impedance of the grid-tied inverter system with PLL and power feedback control is

$$\mathbf{Z_{out\_PQ}} = \left(\begin{array}{l} \mathbf{Z_{out}^{-1}} + \mathbf{G_{id}G_{del}} \\ \left(\begin{array}{l} \mathbf{G^d_{PLL}} - \mathbf{G_{ci}G_{cPQ}G^v_{PQ}G^v_{PLL}} - \\ \left(\mathbf{G_{ci}G_{cPQ}G^i_{PQ}} + \mathbf{G_{ci}} - \mathbf{G_{dei}}\right)\mathbf{G^i_{PLL}} \end{array} \right)\mathbf{K} \end{array} \right)^{-1} \cdot \left(\mathbf{I} + \mathbf{G_{id}G_{del}}\left(\mathbf{G_{ci}G_{cPQ}G^i_{PQ}} + \mathbf{G_{ci}} - \mathbf{G_{dei}}\right)\mathbf{K}\right). \tag{45}$$

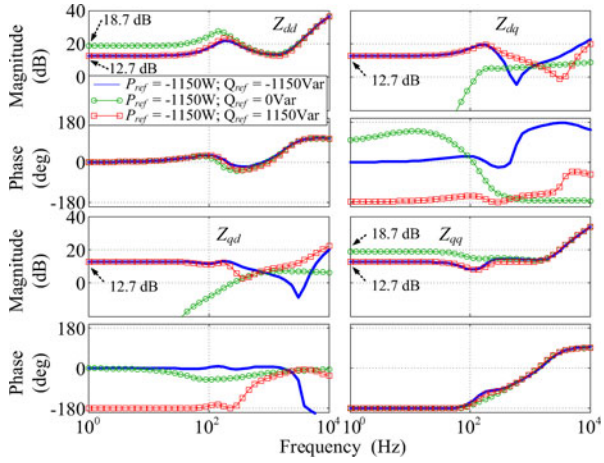

Fig. 20. Impedances of inverter with power feedback control and different reactive power injections.

When DDSRF PLL is used, $\mathbf{G^d_{PLL}}$ is replaced by $\mathbf{G^d_{DDPLL}}$, $\mathbf{G^i_{PLL}}$ is replaced by $\mathbf{G^i_{DDPLL}}$, and $\mathbf{G^v_{PLL}}$ is replaced by $\mathbf{G^v_{DDPLL}}$ in (45).

Fig. 19 shows the impedance of the inverter prototype with power feedback control using the inverter power stage parameters list in Table I and the controller parameters list in Table II in the Appendix. Notice that the integrator gain of the current controller in Table II is increased compared to what is shown in Table I in order to close the power feedback control loop. Once the power flow controller is applied, within its bandwidth, Z_{dd} becomes a positive resistance, and Z_{qq} is still a negative resistance. PLL bandwidth still influences the frequency range of the negative resistance behavior of Z_{qq} as shown in Fig. 19. Z_{dq} and Z_{qd} are still low in the low frequency because of the unity power factor control.

When injecting reactive power into the grid, all four impedances change along with the real and reactive power rating, as shown in Fig. 20. In order to understand the impedance matrix when a power controller is applied, or, in other words, to understand the impedance feature of a constant power source, the following derivations are shown [10]:

$$\begin{cases} P = i_d^s v_d^s + i_q^s v_q^s \\ Q = -i_d^s v_q^s + i_q^s v_d^s. \end{cases} \tag{46}$$

Equation (46) is a good approximation at the frequencies that are below the power regulation bandwidth where P and Q are constant. Then, the voltage vector can be derived as (47) from (46). It can be linearized using the two-variable Taylor series up to the second term as shown in (48). Then, the impedance matrix when frequency is zero is shown in (49). It can be verified by comparing its results with the value shown in Fig. 20 for different reactive injection conditions. (49) as shown bottom of the next page

$$\vec{v}_{dq}^{\,s} = \begin{bmatrix} \dfrac{i_d^s P + i_q^s Q}{\left(i_d^s\right)^2 + \left(i_q^s\right)^2} \\ \dfrac{-i_d^s Q + i_q^s P}{\left(i_d^s\right)^2 + \left(i_q^s\right)^2} \end{bmatrix} \tag{47}$$

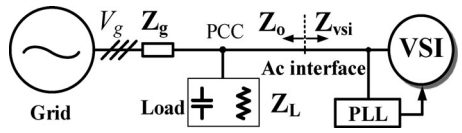

Fig. 21. One line diagram of the inverter system with local load.

$$\begin{aligned}\vec{v}^s_{dq} &= F\left(\vec{i}^s_{dq}\right) \approx F\left(\vec{i}^s_{dq}\right)|_{\vec{I}^s_{dq}} + OF\left(\vec{i}^s_{dq}\right)|_{\vec{I}^s_{dq}} \tilde{\vec{i}}^s_{dq} \\ &= \vec{V}^s_{dq} + \mathbf{Z_{out\_PQ}} \tilde{\vec{i}}^s_{dq} \end{aligned} \tag{48}$$

VI. Stability Analysis Using the Proposed Model

Although this paper focuses on impedance analysis of the three-phase grid-tied inverter, this section gives a brief discussion of stability analysis using the proposed model. This example also shows that increasing PLL bandwidth could cause instability of the grid-tied inverter system under weak grid conditions.

One line diagram representation of the inverter system under study is shown in Fig. 21. In this system, the three-phase inverter is connected to the point of common coupling (PCC) together with the three-phase passive load. This inverter is synchronized with PCC voltage by SRF PLL. Only current feedback control is applied in order to control the amount of power injection to PCC. Each phase of the passive load consists of a parallel connected resistor and capacitor. The grid is connected to PCC through impedance, consisting of an inductor and resistor. The detailed parameters of this system are shown in Table III in the Appendix.

Fig. 22 shows the time-domain simulation results of the inverter system. In the simulation, within the time range from 0 to 10 s, the system is running under stable conditions. At 10 s, proportional gain ($k_{p\mathrm{pll}}$) of PLL PI regulator is increased from 1.5 to 3; both inverter output current as shown in Fig. 22(a) and PLL output frequency of VSI as shown in Fig. 22(b) start to oscillate. The whole system becomes unstable.

In order to predict stable and unstable conditions of the system using the impedance-based method, an ac interface is found at the terminal of the inverter as shown in Fig. 21. As reported by [7], when using impedance-based stability analysis for a grid-tied inverter system, the inverter should be treated as load, and Nyquist stability criterion should be applied to the impedance ratio between the grid-side impedance and inverter impedance as

$$\mathbf{L} = \mathbf{Z_o} \cdot \mathbf{Z_{vsi}^{-1}}. \tag{50}$$

TABLE III
Parameters of Inverter System for Stability Analysis

Symbol	Description	Value
V_g	Grid line-line peak voltage	$120\sqrt{6}$ V
ω_g	Grid voltage frequency	$2\pi \times 60$ rad/s
L	Inductance of inverter	1 mH
V_{dc}	Inverter dc voltage	600 V
f_{sw}	Switching frequency of inverter	20 kHz
I_{dref}	d channel current of inverter	–190 A
I_{qref}	q channel current of inverter	0 A
k_{pi}	Proportional gain of inverter current controller	0.0105
k_{ii}	Integrator gain of inverter current controller	1.1519
k_{ppll}	Proportional gain of inverter PLL	1.5 (stable); 3 (unstable)
k_{ipll}	Integral gain of inverter PLL	3.2
$\mathbf{Z}_{\mathrm{L}}$	Local passive load	R_{Load}: 10 Ω; C_{Load}: 250 μF
$\mathbf{Z}_{\mathrm{g}}$	Grid impedance	R_g: 0.2 Ω; L_g: 2 mH
f_{pll}	PLL output frequency of inverter	

From a small-signal point of view, $\mathbf{Z}_{\mathrm{o}}$ is the parallel of grid impedance $\mathbf{Z}_{\mathrm{g}}$ and load impedance $\mathbf{Z}_{\mathrm{L}}$. The one-phase diagram of $\mathbf{Z}_{\mathrm{o}}$ in stationary frame is shown in Fig. 23. Derivation of $\mathbf{Z}_{\mathrm{o}}$ in *d-q* frame is discussed in [33], using the parameters listed in Table III, $\mathbf{Z}_{\mathrm{o}}$ in *d-q* frame is plotted in Fig. 24 as a solid black line.

Using (39) and inverter parameters listed in Table III, $\mathbf{Z}_{\mathrm{vsi}}$ is calculated and plotted in Fig. 24 as a dashed red line for stable condition ($k_{p\mathrm{pll}} = 1.5$) and a solid red line with a circle marker for unstable conditions ($k_{p\mathrm{pll}} = 3$). The change of PLL design does not change Z_{vsi_dd} in Fig. 24. Significant change has been introduced in Z_{vsi_qq}. There are small variation on Z_{vsi_dq} and Z_{vsi_qd}, but compare to Z_{vsi_qq}, these variation can be ignored, since they are over 30 dB smaller than Z_{vsi_qq}. With bigger value of $k_{p\mathrm{pll}}$, frequency range of negative resistor of Z_{vsi_qq} is extended. Instability is caused by Z_{vsi_qq}.

Using $\mathbf{Z}_{\mathrm{o}}$ and $\mathbf{Z}_{\mathrm{vsi}}$ and applying GNC to impedance ratio $\mathbf{L}$, stability conditions of the example system can be predicted correctly as shown in Fig. 25. In Fig. 25(a), when $k_{p\mathrm{pll}}$ is 1.5, none of the system's characteristic loci encircles the critical point (–1, 0), and the system is stable. In Fig. 25(b), when $k_{p\mathrm{pll}}$ is 3, one of the system's characteristic loci (λ_2) encircles the critical point, which indicates the system is unstable.

In this example, grid-tied inverter is controlled with current controller, the negative resistor is only observed on Z_{qq}, not Z_{dd}. Z_{dq} and Z_{qd} are controlled with very small magnitude under unity power factor. Instability of the system is mainly due to Z_{qq}. More detailed stability analysis using GNC can be

$$\mathbf{Z_{out\_PQ}}(0) = \begin{bmatrix} \dfrac{P}{(I_d^s)^2 + (I_q^s)^2} - \dfrac{2I_d^s\left(I_d^s P + I_q^s Q\right)}{\left((I_d^s)^2 + (I_q^s)^2\right)^2} & \dfrac{Q}{(I_d^s)^2 + (I_q^s)^2} - \dfrac{2I_q^s\left(I_d^s P + I_q^s Q\right)}{\left((I_d^s)^2 + (I_q^s)^2\right)^2} \\ -\dfrac{Q}{(I_d^s)^2 + (I_q^s)^2} - \dfrac{2I_d^s\left(I_q^s P - I_d^s Q\right)}{\left((I_d^s)^2 + (I_q^s)^2\right)^2} & \dfrac{P}{(I_d^s)^2 + (I_q^s)^2} - \dfrac{2I_q^s\left(I_q^s P - I_d^s Q\right)}{\left((I_d^s)^2 + (I_q^s)^2\right)^2} \end{bmatrix} \tag{49}$$

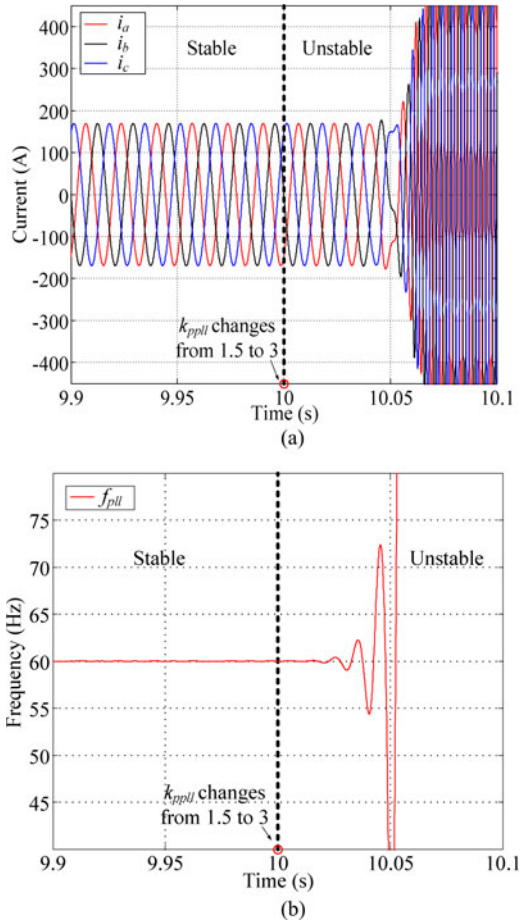

Fig. 22. (a) Inverter output current; (b) PLL output frequency.

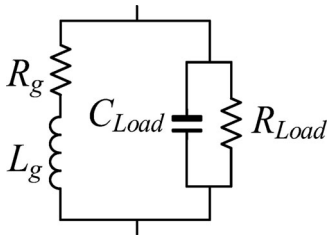

Fig. 23. One phase diagram of $\mathbf{Z}_o$ in stationary frame.

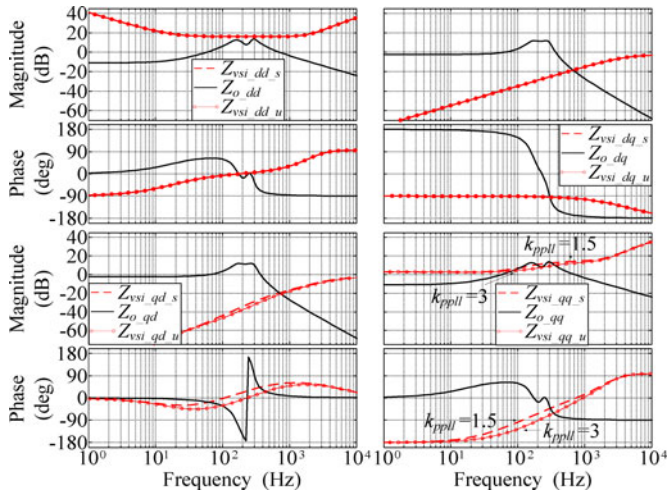

Fig. 24. Impedances of grid side and VSI.

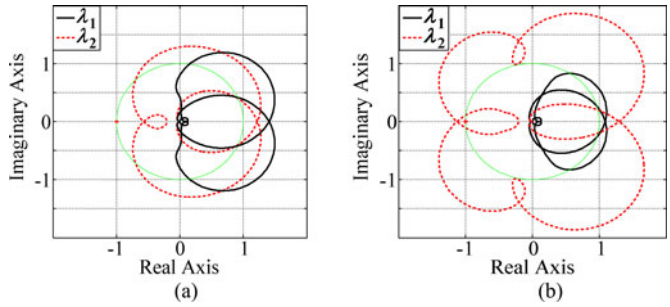

Fig. 25. GNC plots: (a) stable case ($k_{\rm pll} = 1.5$); (b) unstable case ($k_{\rm pll} = 3$).

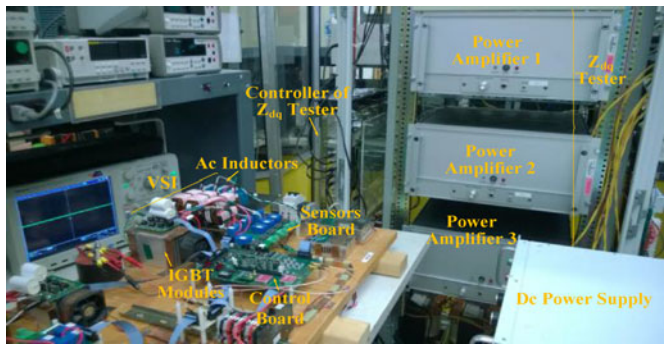

Fig. 26. Experimental system.

found in [29]–[34]; this paper will not elaborate on this particular analysis. When the inverter injects reactive power, magnitude of Z_{dq} becomes significant, but it is still not negative resistor. When power controllers are added and inverter injects reactive power, Z_{dq} and Z_{qd} could also behave as negative resistor as shown in Fig. 20. The impacts of Z_{dq} and Z_{qd} on the system stability under these condition need more discussion in the future.

VII. Experimental Verification

In order to verify the proposed model, a low power prototype of the three-phase grid-tied inverter and *d-q* impedance measurement equipment [44] are built as shown in Fig. 26.

All the impedances were measured from 40 Hz to 10 kHz (half switching frequency of the inverter) with 100 points. For the cases with current feedback control and SRF PLL, an inverter prototype with parameters listed in Table I is used for measurement. For the cases with power feedback control, the parameters listed in Table II are used for measurement.

Fig. 27 shows the measured impedance over-plotted with results calculated using proposed (39) for unit power factor control, where *d* channel current reference is –11 A and the SRF PLL bandwidth is 100 Hz. The results show good accuracy of the proposed model. Fig. 28 shows Z_{qq} with a different SRF PLL bandwidth. The measurement results clearly show the negative

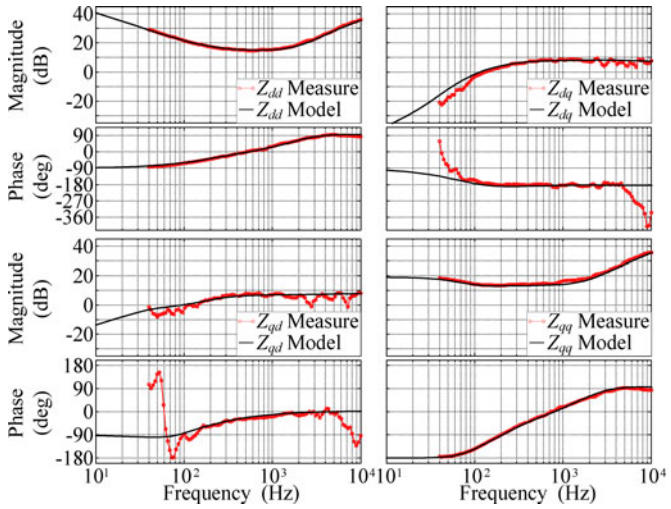

Fig. 27. Measurement results compared with model for $i_{d\mathrm{ref}} = -11A$, $i_{q\mathrm{ref}} = 0A$, $f_{\mathrm{bw\_PLL}} = 100$ Hz.

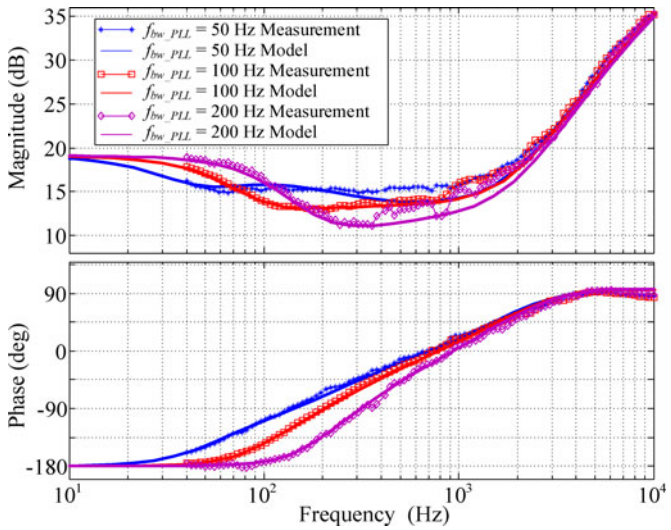

Fig. 28. Measurement results with different PLL bandwidth compared with model for $i_{d\mathrm{ref}} = -11$ A, $i_{q\mathrm{ref}} = 0$ A.

impedance behavior of Z_{qq} and its variation along with PLL bandwidth. Figs. 29 and 30 show the measurement results with inductive and capacitive reactive power under current feedback control with 100-Hz SRF PLL bandwidth. Fig. 31 shows the measurement results with power feedback control where P_{ref} is –1150 W and Q_{ref} is 0 Var. All the measurement results match with the results predicted by the model very well.

VIII. Conclusion

This paper presents an analysis of grid-tied inverter small-signal impedance in *d-q* frame under different control strategies. Influences of PLL, and current and power feedback control to the inverter impedance are discussed. Some important features of inverter impedance are discussed. These features indicate that a grid-tied inverter working as a current source could destabilize the system due to the negative incremental resistor of Z_{qq}. This negative incremental resistor behavior is a result of PLL

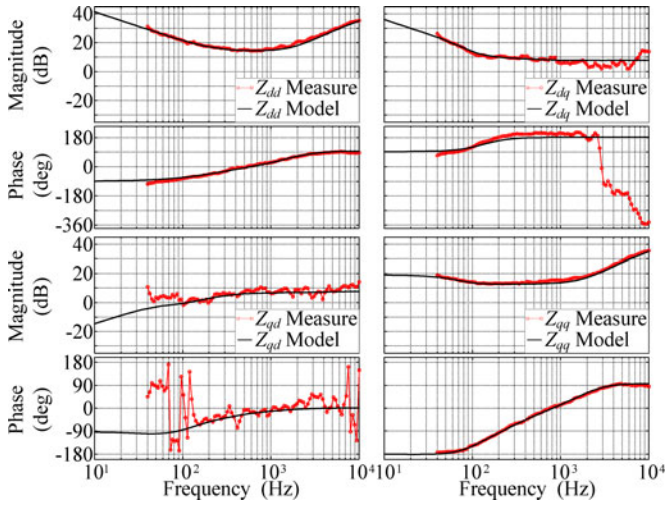

Fig. 29. Measurement results compared with model for $i_{d\mathrm{ref}} = -11$ A, $i_{q\mathrm{ref}} = 6$ A, $f_{\mathrm{bw\_PLL}} = 100$ Hz.

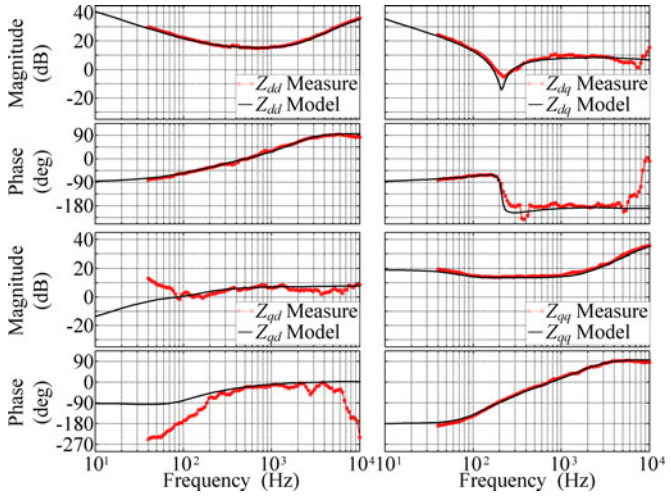

Fig. 30. Measurement results compared with model for $i_{d\mathrm{ref}} = -11$ A, $i_{q\mathrm{ref}} = -6$ A, $f_{\mathrm{bw\_PLL}} = 100$ Hz.

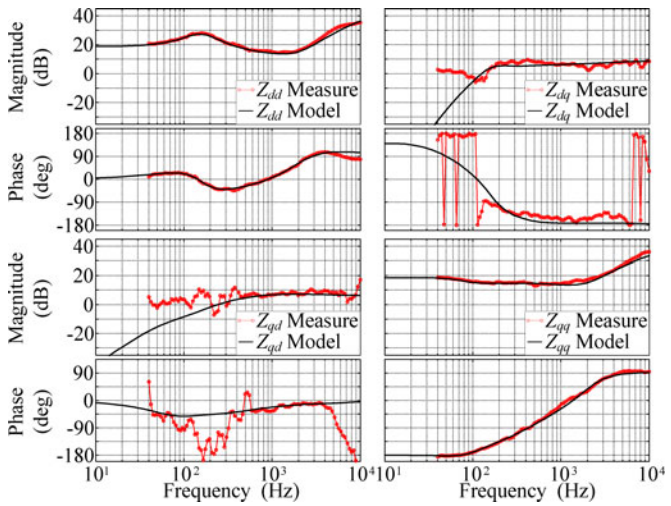

Fig. 31. Measurement results compared with model for $P_{d\mathrm{ref}} = -1150$ W, $Q_{q\mathrm{ref}} = 0$ Var, $f_{\mathrm{bw\_PLL}} = 100$ Hz.

and current injection. Increasing of PLL bandwidth extends the frequency range of this behavior, and increase of inverter power level decreases the absolute value of the resistor. A brief simulation example shows that under weak grid conditions, a small increase of the PLL bandwidth could lead the system to unstable conditions. The example also shows how the proposed model can be used to predict such instability. Hardware measurements verify the proposed model. The model gives insight into the grid-tied inverter's behavior in the grid. Harmonic resonance and instability issues reported in the literature can be analyzed using the characterized impedance model.

APPENDIX

Appendix tables are shown on there own link.

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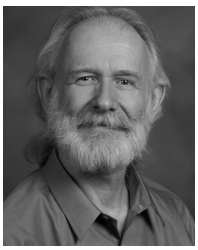

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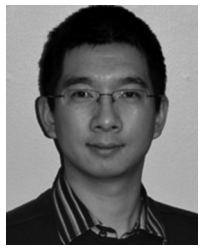

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