

# Small-Signal Modeling and Parameters Design for Virtual Synchronous Generators

Heng Wu, Xinbo Ruan, *Fellow, IEEE*, Dongsheng Yang, *Student Member, IEEE*, Xinran Chen, Wenxin Zhao, Zhipeng Lv, and Qing-Chang Zhong, *Senior Member, IEEE*

**Abstract**—The concept of the virtual synchronous generator (VSG) is emerging as an attractive solution for controlling the grid-connected inverter when the renewable energy has a high penetration level into the grid. This paper focuses on the small-signal modeling and parameters design of the power loop of the VSG, and points out that the bandwidth of the power loop should be far less than twice the line frequency for the purpose of avoiding the VSG output voltage to be severely distorted. Consequently, the line-frequency-averaged small-signal model of the VSG is derived for system analysis and parameters design. Based on the model, the decoupling conditions between the active power loops (APLs) and the reactive power loops (RPLs) of the VSG are given. Finally, a step-by-step parameters design method is proposed to facilitate the design of the control parameters of the VSG. A 10-kVA prototype is built and tested in the laboratory, and the experimental results are given to verify the effectiveness of the theoretical analysis and the proposed parameters design method.

**Index Terms**—Coupling effect, grid-connected inverter, line-frequency-averaged small-signal model, parameters design, virtual synchronous generator (VSG).

## I. INTRODUCTION

NOWADAYS, distributed power generation system (DPGS) based on renewable energy has been drawing more and more attentions for the environmental friendly features. As the interface between the DPGS and the grid, the grid-connected inverter plays an important role in injecting high-quality power into the grid, as well as guaranteeing the safety operation and providing grid support [1].

Manuscript received February 20, 2015; revised December 22, 2015 and February 4, 2016; accepted February 9, 2016. Date of publication March 16, 2016; date of current version June 9, 2016. This work was supported in part by the National Natural Science Foundation of China under Award 50837003, in part by the Jiangsu Province 333 Program for Excellent Talents under Award BRA2012141, and in part by the Project Funded by the Priority Academic Program Development of Jiangsu Higher Education Institutions.

H. Wu, X. Ruan, D. Yang, X. Chen, and W. Zhao are with the Center for More-Electric-Aircraft Power Systems, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: wuhengee@nuaa.edu.cn; ruanxb@nuaa.edu.cn; yangdongsheng@nuaa.edu.cn; chengxinran@nuaa.edu.cn).

Z. Lv is with the China Electric Power Research Institute, Beijing 100192, China (e-mail: lvzhipeng@epri.sgcc.com.cn).

Q.-C. Zhong is with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL 60616 USA, and also with the Department of Automatic Control and Systems Engineering, The University of Sheffield, Sheffield, S10 2TN, U.K. (e-mail: zhongqc@ieee.org).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TIE.2016.2543181

In the past, the DPGS is not required to take part in the power regulation of the grid due to the low penetration level. For example, according to the original grid codes, such as IEEE Standard 1547-2003 and IEC 61727 [2], [3], the DPGS is required to produce as much energy as possible with satisfactory quality of the injected grid current in normal operation, and should cease to energize under grid faults within the certain clearing time. The policy is reasonable since the low penetration level of the DPGS has negligible influence on the grid. Any random power fluctuation of the DPGSs will be compensated by large conventional synchronous generators (SGs), and some of these generators will also take care of the overall power balance, system stability, and fault ride through.

However, when the penetration of the DPGS reaches to a certain level, such “irresponsible” behavior of the DPGS may threaten the stability of the grid [4]. Therefore, the DPGS is required to actively take part in the power regulation of the grid, just like the conventional SGs. Based on this idea, the concept of virtual synchronous generators (VSGs) was proposed to control the grid-connected inverter to emulate the essential behavior of the SGs, including the droop mechanism and the inertial characteristic. As a result, the VSG has the ability of providing grid support by automatically changing its active and reactive powers according to the frequency and amplitude of grid voltage, respectively. Meanwhile, the inertial characteristic emulated by the VSG also contributes to the total inertia of the grid, which is helpful to enhance the transient frequency stability. In addition to the grid-connection mode, the VSG can also be operated in standalone mode and ensures load sharing naturally in the same way as the conventional SG does. Various implementations of the VSG have been proposed [4]–[9]. It was pointed out that the VSG can be considered to be controlled with a droop control method together with virtual inertia introduced by a first-order low-pass filter in the power loop [10]. This conclusion built the bridge between the VSG and droop control and provided the useful insight for the system analysis.

Since the VSG algorithm is implemented in the software, the parameters of the VSG (include the droop coefficients and virtual inertia) are not constrained by the physical design of any real SG and can be set arbitrarily. Therefore, these parameters can be tuned freely to achieve the desired performance.

The instantaneous output power of the VSG pulsates at twice the line frequency ( $2f_{line}$ ) if the local loads or the grid voltages are unbalanced [11], resulting in the double-line-frequency ripple (DLFR) in the frequency and amplitude of the output voltage of the VSG, which is harmful to critical loads. Therefore, the bandwidth of the power loop of the VSG should

be far less than  $2f_{line}$  to attenuate these DLFR. Meanwhile, other conventional control requirements, such as the system stability and robustness, as well as the best possible dynamic performance, should also be taken into consideration in the parameters design.

In the recent years, the parameters design of the VSG has been discussed [12], [13]. Due to the equivalence of the VSG and droop control, the parameters design methods of droop control also provide the design guidance for the VSG [14]–[16]. The root-locus design method was used in [12], but it did not consider the attenuation requirement of the DLFR, thus the designed parameters may not be good enough and they are needed to be further adjusted to obtain the optimized results. In [14]–[16], the closed-loop characteristic equation of the power loop with droop control was derived for system analysis and parameters design. However, due to the coupling effect between the active power loop (APL) and the reactive power loop (RPL), the parameters design of the two loops is very difficult, and the control parameters were partially tuned by trial-and-error.

In this paper, the inherent coupling effect between the APL and RPL is analyzed, and it is pointed out that the inherent coupling effect can be ignored if the phase margin (PM) of the APL and RPL loop gain is greater than  $30^\circ$  and the short-circuit ratio of the system is no less than 10. Therefore, the parameters of each loop can be designed independently, which greatly simplify the design procedure. Hereafter, this paper proposes a simple step-by-step parameters design method with consideration of all the aforementioned control requirements. With this method, the control parameters of the power loops of the VSG can be easily determined without trial-and-error. Moreover, this design method can also be extended to other implementations of VSGs and droop control, such as “virtual synchronous machine (VISMA)” concept proposed in [5] and [6] and “synchronverter” concept proposed in [7]–[9].

This paper is organized as follows. Section II introduces the basic operation principle of the VSG. Section III demonstrates the necessity of lowering the bandwidth of the power loops of the VSG to attenuate the DLFR and derives the line-frequency-averaged small-signal model of the VSG. Based on the model, the decoupling conditions of the APL and RPL are discussed in Section IV, and a step-by-step design method of the power loops of the VSG is presented in detail in Section V. The experimental results are presented in Section VI to verify the theoretical analysis and parameters design method. Section VII concludes this paper.

## II. BASIC OPERATION PRINCIPLE OF THE VSG

Fig. 1 shows the topology and control diagram of the VSG. A typical three-phase voltage-source inverter is connected to the grid at the point of common coupling (PCC) through an LC filter, which is composed of the inverter-side inductor  $L_1$ , and filter capacitor  $C_f$ .  $Z_g$  denotes the grid impedance at the PCC. The control diagram shown in Fig. 1 is similar to that proposed in [8].

The output active and reactive powers of the VSG can be calculated according to the instantaneous power theory [17]. The

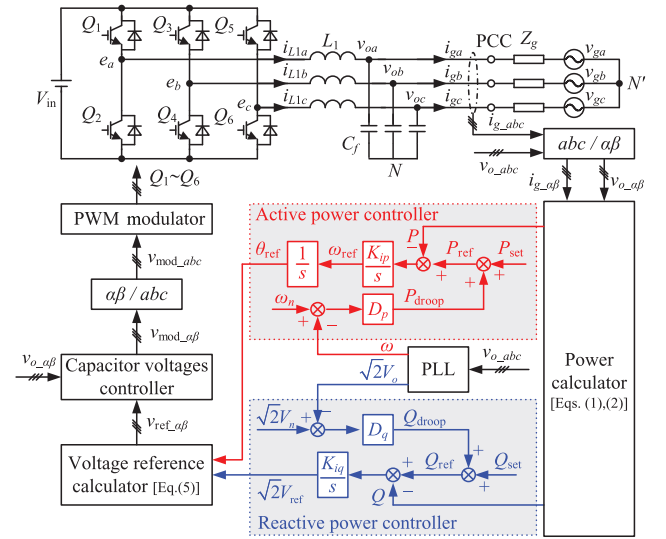


Fig. 1. Topology and control diagram of the VSG.

calculation can be conducted in the  $abc$  frame,  $\alpha\beta$  frame, or  $dq$  frame. In this paper, the  $\alpha\beta$  frame is adopted due to its simple implementation, and the output active and reactive powers of the VSG can be expressed as

$$P = v_{o\alpha}i_{g\alpha} + v_{o\beta}i_{g\beta} \quad (1)$$

$$Q = v_{o\beta}i_{g\alpha} - v_{o\alpha}i_{g\beta} \quad (2)$$

where  $v_{o\alpha}$  and  $v_{o\beta}$  are the capacitor voltages in the  $\alpha\beta$  frame, and  $i_{g\alpha}$  and  $i_{g\beta}$  are the injected grid currents in the  $\alpha\beta$  frame.

The output active power  $P$  is fed into the active power controller to work out the phase angle of the voltage reference  $\theta_{ref}$ , while the output reactive power  $Q$  is fed into the reactive power controller to work out the amplitude of the voltage reference  $\sqrt{2}V_{ref}$ .

The active power reference  $P_{ref}$  consists of the setting value  $P_{set}$  and the droop value  $P_{droop}$ .  $P_{droop}$  is calculated by multiplying the difference between the actual angular frequency of the capacitor voltages  $\omega$  and the nominal angular frequency  $\omega_n$  with a droop coefficient  $D_p$ . Note that,  $\omega$  is obtained by the phase-locked loop (PLL). So,  $P_{ref} = P_{set} + D_p(\omega_n - \omega)$ . Since  $\omega \approx \omega_g$ , the VSG can automatically change its output active power according to the grid frequency, where  $\omega_g$  is the angular frequency of the grid. This introduces the  $P - \omega$  droop mechanism. Meanwhile, the integral term  $K_{ip}/s$  is adopted here to introduce the virtual inertia.

The operating principle of the reactive power controller is similar to that of the active power controller. The  $Q - V$  droop mechanism is introduced by making  $Q_{ref} = Q_{set} + \sqrt{2}D_q(V_n - V_o)$ . Since  $V_o \approx V_g$ , the VSG can automatically change its output reactive power according to the grid voltage, where  $V_g$  is the root-mean-square (rms) value of the grid voltages. The virtual inertia is embodied by the integral term  $K_{iq}/s$ .

So, the power control scheme shown in Fig. 1 is indeed reproducing the essential behavior of a real SG, including the droop mechanism and the inertial characteristic, which is beneficial to improve the grid stability.

According to Fig. 1, we have

$$\omega_{\text{ref}} = K_{ip} \int [P_{\text{set}} + D_p (\omega_n - \omega) - P] dt \quad (3)$$

$$\sqrt{2}V_{\text{ref}} = K_{iq} \int [Q_{\text{set}} + \sqrt{2}D_q (V_n - V_o) - Q] dt. \quad (4)$$

$\theta_{\text{ref}}$  is the integral of  $\omega_{\text{ref}}$ . Thus, the voltage references in the  $\alpha\beta$  frame  $v_{\text{ref}\alpha}$  and  $v_{\text{ref}\beta}$  can be calculated as

$$\begin{cases} v_{\text{ref}\alpha} = \sqrt{2}V_{\text{ref}} \cos \theta_{\text{ref}} \\ v_{\text{ref}\beta} = \sqrt{2}V_{\text{ref}} \sin \theta_{\text{ref}}. \end{cases} \quad (5)$$

The capacitor voltages controller in the  $\alpha\beta$  frame is introduced here to make the capacitor voltages accurately track the voltage references. The outputs of the capacitor voltages controller are transformed into the  $abc$  frame from the  $\alpha\beta$  frame, and then they are fed into the pulse width modulation (PWM) modulator to generate the drive signals of power switches  $Q_1$ – $Q_6$ .

With a proper design of the capacitor voltages' control loop, the capacitor voltages can accurately track the voltage references. Thus, we have

$$\omega \approx \omega_{\text{ref}} \quad (6a)$$

$$\theta \approx \theta_{\text{ref}} \quad (6b)$$

$$V_o \approx V_{\text{ref}}. \quad (6c)$$

Note that when the voltages and currents are sampled, the values are usually proportionally scaled, which may introduce extra sampling coefficients to the control loops. For simplicity, the digital signal processor (DSP) is programmed to automatically transform the sampled values to the actual ones once receiving them, so that the sampling coefficients can be equivalently considered as 1, and they are omitted in the control diagrams in this paper. This paper focuses on the modeling and parameters design of the power loop of the VSG, and the parameters design of the inner capacitor voltages loop, which has been discussed in [18], is not presented here.

### III. LINE-FREQUENCY-AVERAGED SMALL-SIGNAL MODEL OF THE VSG

#### A. Calculation of the Average Values of the Active and Reactive Powers Over Half of the Line Period

If the local loads or the grid voltages are unbalanced, the instantaneous output power of the VSG will pulsate at  $2f_{\text{line}}$ . As shown in Fig. 2, if the DLFR in the active and reactive powers is not well attenuated by the power control loops, it may be reflected in the frequency and amplitude of the voltage reference. As a consequence, the capacitor voltages of the VSG will be distorted. To avoid this problem, the APL and RPL must be designed to have sufficiently low loop gain at  $2f_{\text{line}}$  to attenuate the DLFR in the active and reactive powers. With this consideration, it is unnecessary to model the system's high-frequency behavior when designing the low-bandwidth power loops of the VSG. So, the instantaneous powers can be replaced by their low-frequency averaged values during the modeling procedure [19], expressed as

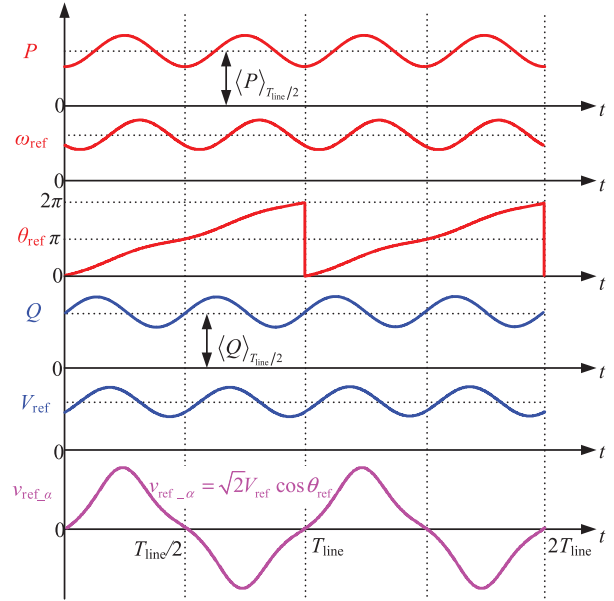


Fig. 2. DLFR in the instantaneous output power distort the PWM reference of the VSG.

$$P \approx \langle P \rangle_{T_{\text{line}}/2} = \frac{2}{T_{\text{line}}} \int_{T_{\text{line}}/2} P dt \quad (7)$$

$$Q \approx \langle Q \rangle_{T_{\text{line}}/2} = \frac{2}{T_{\text{line}}} \int_{T_{\text{line}}/2} Q dt \quad (8)$$

where  $\langle P \rangle_{T_{\text{line}}/2}$  and  $\langle Q \rangle_{T_{\text{line}}/2}$  denote the average values of  $P$  and  $Q$  over half the line period ( $T_{\text{line}}/2$ ), respectively. Averaging over  $T_{\text{line}}/2$  removes the DLFR, leaving the underlying low-frequency variations which are of concern.

The phasor representations of the sinusoidal voltage and current can be used to calculate the active and reactive powers [19]. When the three-phase grid voltages are balanced,  $\vec{V}_g = V_g \angle 0^\circ$  and  $\vec{V}_o = V_o \angle \delta$  can be used to represent the phasors of the grid voltages and the capacitor voltages, respectively, where  $\delta$  is the power angle, which is expressed as [20]

$$\delta = \int (\omega - \omega_g) dt. \quad (9)$$

The grid impedance can be represented by  $Z_g = r + jX_s$ , where  $r$  denotes the resistive component, while  $X_s$  denotes the inductive component. On that basis, the phasor of the injected grid currents can be written as

$$\vec{I}_g = \frac{\vec{V}_o - \vec{V}_g}{r + jX_s}. \quad (10)$$

Thus, the output complex power of the VSG can be expressed as

$$\begin{aligned} S &= 3\vec{V}_o \cdot \vec{I}_g = 3\vec{V}_o \cdot \frac{\vec{V}_o - \vec{V}_g}{r + jX_s} \\ &= 3 \cdot \frac{V_o^2 - V_o V_g (\cos \delta + j \sin \delta)}{r - jX_s} \end{aligned} \quad (11)$$

where  $\vec{V}_o$ ,  $\vec{V}_g$ , and  $\vec{I}_g$  are the conjugate phasors of  $\vec{V}_o$ ,  $\vec{V}_g$ , and  $\vec{I}_g$ , respectively.

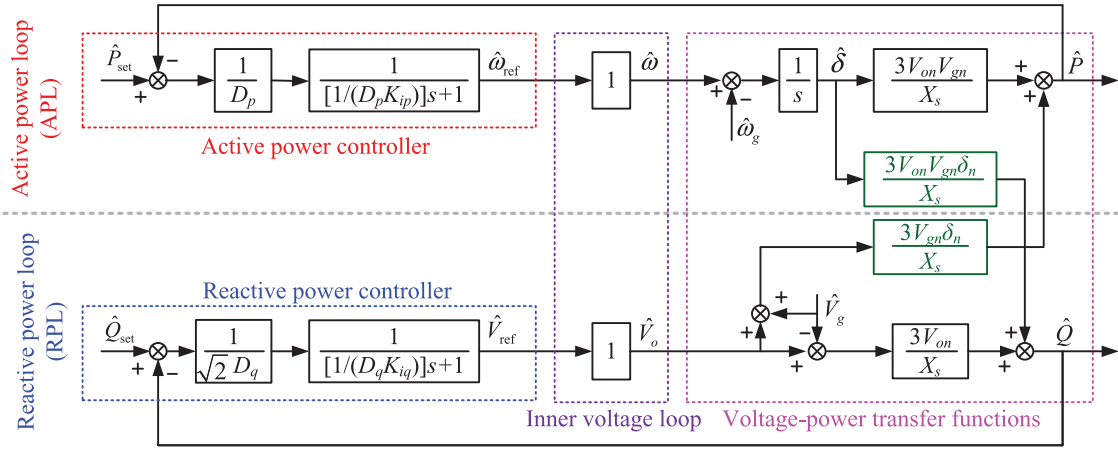


Fig. 3. Line-frequency-averaged small-signal model of the VSG.

In this paper, it is assumed that the impedance  $Z_g$  is mainly inductive. If not, a virtual inductor can be introduced to be in series with it through the control strategy, and thus making the impedance to be inductive [21]. Therefore,  $X_s \gg r$  can always be guaranteed, and (11) can be rewritten as

$$S \approx 3V_o V_g \sin \delta / X_s + j3(V_o - V_g \cos \delta) V_o / X_s = P + jQ \quad (12)$$

where

$$P = 3V_o V_g \sin \delta / X_s \quad (13)$$

$$Q = 3(V_o - V_g \cos \delta) V_o / X_s. \quad (14)$$

Given that (13) and (14) are the mathematical descriptions of the average values of the instantaneous active and reactive powers over  $T_{line}/2$ , the model to be derived based on these equations is only valid for the frequency range that is lower than the line frequency [19]. Nevertheless, it is enough for system analysis and parameters design, and hereinafter, this model is called line-frequency-averaged small-signal model.

### B. Derivation of Line-Frequency-Averaged Small-Signal Model of the VSG

The mathematical descriptions of the VSG, i.e., (3), (4), (6), (9), (13), and (14), are used to derive the small-signal ac model of the VSG at the quiescent operating point. It is assumed that any state variable  $x$  in these equations is equal to the corresponding quiescent value  $X_n$ , plus superimposed small ac variation  $\hat{x}$ . Hence, we have

$$\omega = \omega_n + \hat{\omega} \quad (15a)$$

$$\omega_{ref} = \omega_n + \hat{\omega}_{ref} \quad (15b)$$

$$\omega_g = \omega_{gn} + \hat{\omega}_g \quad (15c)$$

$$\delta = \delta_n + \hat{\delta} \quad (15d)$$

$$V_o = V_{on} + \hat{V}_o \quad (15e)$$

$$V_{ref} = V_{on} + \hat{V}_{ref} \quad (15f)$$

$$V_g = V_{gn} + \hat{V}_g \quad (15g)$$

$$P = P_n + \hat{P} \quad (15h)$$

$$Q = Q_n + \hat{Q} \quad (15i)$$

$$P_{set} = P_{set\_n} + \hat{P}_{set} \quad (15j)$$

$$Q_{set} = Q_{set\_n} + \hat{Q}_{set}. \quad (15k)$$

Substituting (6a), (15b), (15h), and (15j) into (3), and substituting (6c), (15f), (15i), and (15k) into (4), then neglecting the dc terms, and applying Laplace transformation to the equations, we have

$$\begin{cases} \hat{\omega}_{ref}(s) = \frac{1}{D_p} \frac{\hat{P}_{set}(s) - \hat{P}(s)}{\frac{1}{D_p K_{ip}} s + 1} \\ \hat{V}_{ref}(s) = \frac{1}{\sqrt{2} D_q} \frac{\hat{Q}_{set}(s) - \hat{Q}(s)}{\frac{1}{D_q K_{iq}} s + 1}. \end{cases} \quad (16)$$

From (16), the small-signal model of the active and reactive power controllers in Fig. 1 can be derived, as shown in Fig. 3. As observed, each controller is equivalent to a proportional term and a first-order low-pass filter in the forward path of the power loop. The proportional terms correspond to the droop coefficients in Fig. 1, reflecting the droop mechanism, while the first-order low-pass filters correspond to the integral terms in Fig. 1, reflecting the virtual inertia.

Substituting (15a) and (15b) into (6a), and substituting (15e) and (15f) into (6c), then neglecting the dc terms, and applying Laplace transformation to the equations, we have

$$\begin{cases} \hat{\omega}(s) = \hat{\omega}_{ref}(s) \\ \hat{V}_o(s) = \hat{V}_{ref}(s). \end{cases} \quad (17)$$

According to (17), the inner capacitor voltages loop in Fig. 1, including the voltage reference calculator, capacitor voltages controller, PWM modulator, and the LC filter, can be considered as a follower in the forward path of the power loop, as depicted in Fig. 3.

Moreover, by substituting (15a), (15c), and (15d) into (9), substituting (15d), (15e), (15g), and (15h) into (13), and substituting (15d), (15e), (15g), and (15i) into (14), then applying the approximations  $\sin \delta_n \approx \delta_n$ ,  $\sin \hat{\delta} \approx \hat{\delta}$ ,  $\cos \delta_n \approx 1$ , and  $\cos \hat{\delta} \approx 1$ , neglecting the dc terms, second-order, and higher order ac terms, and applying Laplace transformation to the equations, we have



$$\begin{cases} \hat{\delta}(s) = \frac{\hat{\omega}(s) - \hat{\omega}_g(s)}{s} \\ \hat{P}(s) = \frac{3V_{on}V_{gn}}{X_s} \hat{\delta}(s) + \frac{3V_{gn}\delta_n}{X_s} (\hat{V}_o(s) + \hat{V}_g(s)) \\ \hat{Q}(s) = \frac{3V_{on}}{X_s} (\hat{V}_o(s) - \hat{V}_g(s)) + \frac{3V_{on}V_{gn}\delta_n}{X_s} \hat{\delta}(s). \end{cases} \quad (18)$$

From (18), the transfer functions from the capacitor voltages to the output powers, which are related to the grid impedances, grid voltages, and power calculator in Fig. 1, can be derived, as shown in Fig. 3. This completes the line-frequency-averaged small-signal model of the VSG.

It is clear that the APL and RPL, which are shown, respectively, in the upper and lower parts of Fig. 3, are coupled due to the inherent nature of the output active and reactive powers of the VSG, as both  $\hat{P}(s)$  and  $\hat{Q}(s)$  are related to  $\hat{\delta}(s)$  (which is resulted from the APL) and  $\hat{V}_o(s)$  (which is resulted from the RPL), which brings difficulty to system analysis and parameters design.

#### IV. DECOUPLING OF THE APL AND RPL

According to Fig. 3, if the coupling items are ignored, the loop gains of the APL and RPL,  $T_p(s)$  and  $T_q(s)$ , can be obtained as

$$T_p(s) = \frac{3V_{on}V_{gn}}{X_s} \frac{1}{D_p} \frac{1}{\frac{1}{D_p K_{ip}} s + 1} \frac{1}{s} \quad (19)$$

$$T_q(s) = \frac{3V_{on}}{X_s} \frac{1}{\sqrt{2}D_q} \frac{1}{\frac{1}{D_q K_{iq}} s + 1}. \quad (20)$$

##### A. Decoupling of the APL

As shown in Fig. 3, when deriving the loop gain of the APL,  $\hat{Q}_{set}$ ,  $\hat{\omega}_g$ , and  $\hat{V}_g$  can be regarded as the perturbations of the APL, and they are set to zero. Thus, the loop gain of the APL when considering the coupling effect  $T_{pc}$  is derived as

$$T_{pc}(s) \approx T_p(s) \left( 1 - \frac{T_q(s)}{1 + T_q(s)} \delta_n^2 \right). \quad (21)$$

In (21), the term  $T_q/(1 + T_q)$  stands for the closed-loop transfer function of the RPL (regardless of the coupling effect), and its magnitude is smaller than  $1/\sin PM$  over the whole frequency range [22], where PM is the phase margin of  $T_q(s)$ . To ensure system stability and robustness,  $PM > 30^\circ$  is usually expected. So, we have

$$\left| \frac{T_q(s)}{1 + T_q(s)} \right| \leq \frac{1}{\sin PM} \leq \frac{1}{\sin 30^\circ} = 2. \quad (22)$$

According to (13), we have

$$P_n = \frac{3V_{on}V_{gn}}{X_s} \sin \delta_n \approx \frac{3V_{on}V_{gn}}{X_s} \delta_n. \quad (23)$$

Equation (23) can be rewritten as

$$\delta_n = \frac{P_n X_s}{3V_{on}V_{gn}} = \frac{(P_n/3)/V_{on}}{V_{gn}/X_s} = \frac{I_n}{I_{SC}}. \quad (24)$$

where  $I_n = (P_n/3)/V_{on}$  is the nominal current, and  $I_{SC} = V_{gn}/X_s$  is the short-circuit current of the grid at PCC. Normally,  $I_{SC}/I_n$ , which is defined as the short-circuit ratio, is required to be no less than 10 [23], yielding

$$\delta_n \leq 0.1 \text{ rad}. \quad (25)$$

According to (22) and (25), it can be obtained that

$$\left| \frac{T_q(s)}{1 + T_q(s)} \delta_n^2 \right| \leq 0.02 \ll 1. \quad (26)$$

Equation (26) indicates that the magnitude of the coupling term is far less than one and can be neglected. Therefore, (21) can be simplified as

$$T_{pc}(s) \approx T_p(s). \quad (27)$$

##### B. Decoupling of the RPL

The loop gain of the RPL when considering the coupling effect  $T_{qc}$  can be derived by letting  $\hat{P}_{set}$ ,  $\hat{\omega}_g$ , and  $\hat{V}_g$  to be zero in Fig. 3, and it is expressed as

$$T_{qc}(s) \approx T_q(s) \left( 1 - \frac{T_p(s)}{1 + T_p(s)} \delta_n^2 \right). \quad (28)$$

Similarly, the term  $T_p/(1 + T_p)$  stands for the closed-loop transfer function of the APL (regardless of the coupling effect), and its magnitude is smaller than  $1/\sin PM$  over the whole frequency range, where PM is the phase margin of  $T_p(s)$ . If  $PM > 30^\circ$ ,  $|T_p/(1 + T_p)| < 2$  will be guaranteed. Considering this and (25), it can be obtained that

$$\left| \frac{T_p(s)}{1 + T_p(s)} \delta_n^2 \right| \leq 0.02 \ll 1. \quad (29)$$

Therefore, the coupling term of the RPL can also be neglected, and (28) can be approximated as

$$T_{qc}(s) \approx T_q(s). \quad (30)$$

In conclusion, the coupling effect between the APL and RPL can be neglected if the following conditions are satisfied.

- 1) The PM of  $T_p(s)$  and  $T_q(s)$  is greater than  $30^\circ$ .
- 2) The short-circuit ratio  $I_{SC}/I_n$  is not less than 10.

As a consequence, the control parameters of the APL and RPL can be designed independently, which greatly simplify the design procedure. Usually, the first condition can be satisfied by tuning the parameters of the APL and RPL, which will be discussed in the following section. The second condition is always satisfied for the VSG.

Fig. 4 shows the root locus plots of the APL and RPL with and without the coupling terms. As seen clearly, the loop gains of APL (RPL) with and without the coupling terms have similar poles, which are almost coincided with each other. The additional poles and zeros introduced by the coupling terms are very close and are cancelled by each other. Therefore, their impact on the control performance of the system can be neglected.

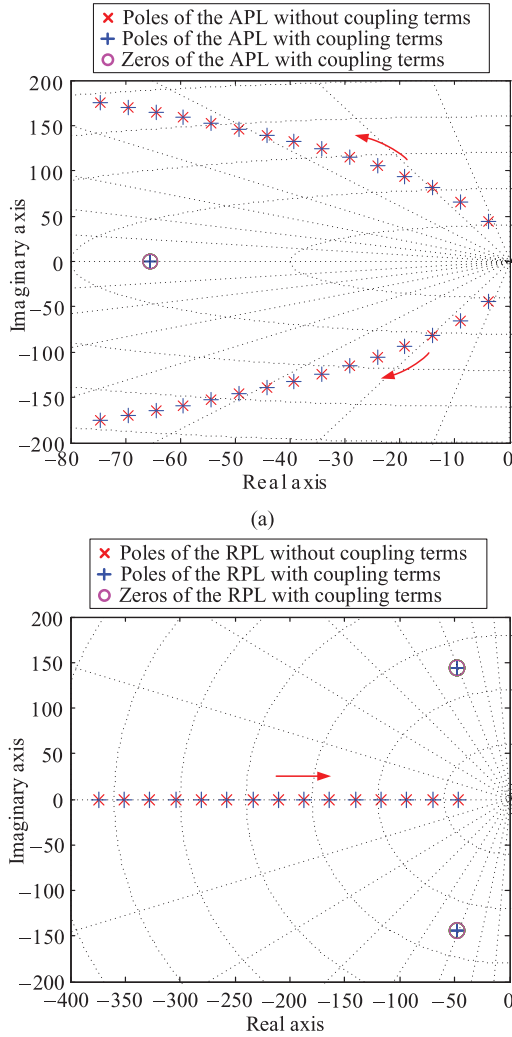


Fig. 4. Root locus plot of the APL and RPL with and without the coupling terms. (a) APL with  $K_{ip}$  varies from 0.005 to 0.1. (b) RPL with  $K_{iq}$  varies from 0.045 to 0.03.

## V. PARAMETERS DESIGN OF THE POWER LOOPS OF THE VSG

Since the coupling terms between the APL and RPL can be ignored, the line-frequency-averaged small-signal model of the VSG shown in Fig. 3 can be simplified into that shown in Fig. 5. This section will propose an optimized parameters design method of the APL and RPL considering the requirements of system stability margin, DLFR attenuation, as well as the dynamic performance improvement. A design example will also be presented in this section to verify the effectiveness of the design method.

### A. Parameters Design of the APL

There are two parameters to be determined in the APL, which are the integral coefficient  $K_{ip}$  and droop coefficient  $D_p$ . Basically,  $D_p$  is usually decided by the grid code. Thus, only  $K_{ip}$  needs to be designed for ensuring the system stability and for meeting the requirement of attenuating the DLFR in the APL.

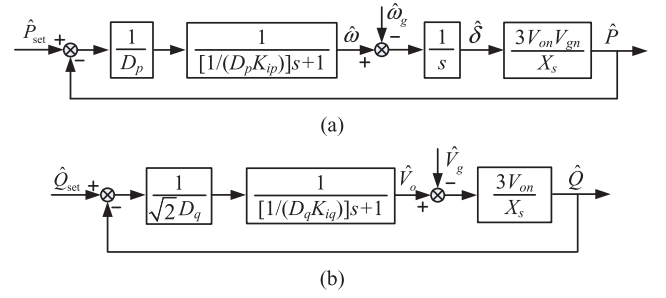


Fig. 5. Line-frequency-averaged small-signal model of the VSG regardless of the coupling terms. (a) APL. (b) RPL.

The corner frequency of the first-order low-pass filter in the APL can be expressed as

$$f_{pL} = \frac{D_p K_{ip}}{2\pi}. \quad (31)$$

Equation (31) indicates that a smaller  $K_{ip}$  results in lower  $f_{pL}$ , which means a better attenuation ability of the DLFR. However, when  $f_{pL}$  decreases, the phase lag introduced by the first-order low-pass filter increases, resulting in the reduction in the PM of the APL, and the whole system stability is degraded. So, there is a tradeoff in choosing  $K_{ip}$ .

The magnitude of the APL loop gain at the crossover frequency  $f_{pc}$  is unity. Thus, according to (19), we have

$$|T_p(j2\pi f_{pc})| = \frac{3V_{on}V_{gn}}{X_s D_p} \frac{1}{\left| \frac{j2\pi f_{pc}}{D_p K_{ip}} + 1 \right|} \frac{1}{|j2\pi f_{pc}|} = 1. \quad (32)$$

According to (32),  $K_{ip}$  can be calculated as

$$K_{ip} = \frac{2\pi f_{pc}}{D_p \sqrt{\left( \frac{3V_{on}V_{gn}}{2\pi f_{pc} X_s D_p} \right)^2 - 1}}. \quad (33)$$

According to (19), the magnitude of the APL loop gain at  $2f_{line}$  can be expressed as

$$|T_p(j2\pi \cdot 2f_{line})| = \frac{3V_{on}V_{gn}}{X_s D_p} \frac{1}{\left| \frac{j4\pi f_{line}}{D_p K_{ip}} + 1 \right|} \frac{1}{|j4\pi f_{line}|}. \quad (34)$$

Since  $f_{pL}$  is far below  $2f_{line}$  to ensure the DLFR attenuation, the following approximation can be satisfied:

$$\frac{1}{\left| \frac{j4\pi f_{line}}{D_p K_{ip}} + 1 \right|} \approx \frac{1}{\left| \frac{j4\pi f_{line}}{D_p K_{ip}} \right|}. \quad (35)$$

Thus, (34) can be simplified as

$$|T_p(j2\pi \cdot 2f_{line})| \approx \frac{3V_{on}V_{gn}K_{ip}}{16\pi^2 f_{line}^2 X_s}. \quad (36)$$

To attenuate the DLFR in the APL, the APL must have sufficiently small loop gain at  $2f_{line}$ . Define  $a_p$  as the magnitude requirement of the loop gain of the APL at  $2f_{line}$ , then  $|T_p(j2\pi \cdot 2f_{line})| \leq a_p$ . So, we have

$$K_{ip} \leq \frac{16\pi^2 f_{line}^2 X_s a_p}{3V_{on}V_{gn}} \triangleq K_{ip \max}. \quad (37)$$

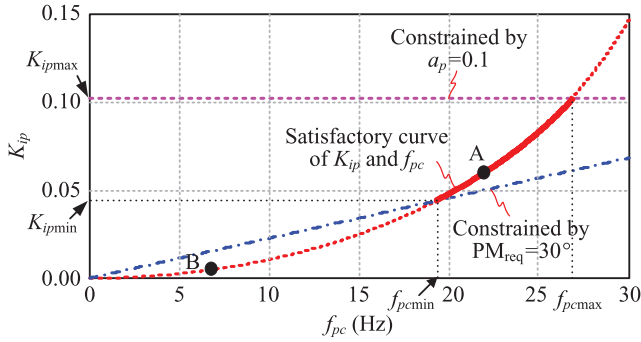


Fig. 6. Satisfactory curve of  $K_{ip}$  and  $f_{pc}$  constrained by  $PM_{req}$  and  $a_p$ .

To meet the required phase margin  $PM_{req}$ , the following condition should be satisfied:

$$PM = 180^\circ + \angle T_p(j2\pi f_{pc}) \geq PM_{req}. \quad (38)$$

Substituting (19) into (38), yields

$$90^\circ - \arctan \frac{2\pi f_{pc}}{D_p K_{ip}} \geq PM_{req}. \quad (39)$$

According to (39),  $K_{ip}$  can be calculated as

$$K_{ip} \geq \frac{2\pi f_{pc}}{D_p} \tan PM_{req} \triangleq K_{ipmin}. \quad (40)$$

The design procedure of the parameters of the APL is proposed as follows.

- Step 1): Determine the specifications of the loop gain of the APL. In general, PM is required in the range of  $30^\circ$  to  $70^\circ$  for achieving good dynamic response and robustness.  $a_p \leq 0.1$  is required to ensure good attenuation of the DLFR in the APL.
- Step 2): Based on the given specifications, according to (33), (37), and (40), the curves of  $K_{ip}$  as the function of  $f_{pc}$  are depicted as shown in Fig. 6, where  $f_{pcmax}$  is the maximum crossover frequency of APL determined by (33) and (37), while  $f_{pcmin}$  is the minimum crossover frequency of APL determined by (33) and (40). The thick solid line is the satisfactory curve of the  $K_{ip}$  and  $f_{pc}$ .
- Step 3): Choose an appropriate  $f_{pc}$  within the satisfactory curve. A larger  $f_{pc}$  in the corresponding satisfactory range is recommended, since it is beneficial to improving the dynamic performance of the system. After  $f_{pc}$  is determined,  $K_{ip}$  can be directly calculated according to (33).
- Step 4): Check the loop gain of the APL to ensure that all the specifications are well satisfied.

### B. Parameters Design of the RPL

There are two parameters to be determined in the RPL, which are the integral coefficient  $K_{iq}$  and droop coefficient  $D_q$ .  $D_q$  is usually decided by the grid code. So,  $K_{iq}$  should be carefully designed to ensure the system stability and meet the requirement of attenuating the DLFR in the RPL.

TABLE I  
PARAMETERS OF THE PROTOTYPE

Parameters	Value	Parameters	Value
Input voltage $V_{in}$	800 V	Switching frequency $f_s$	10 kHz
Grid voltage $V_g$ (rms)	220 V	Inverter-side inductor $L_1$	3.2 mH
Rated power	10 kVA	Filter capacitor $C$	10 $\mu$ F
Line frequency $f_{line}$	50 Hz	Grid-side inductor $L_g$	1.2 mH

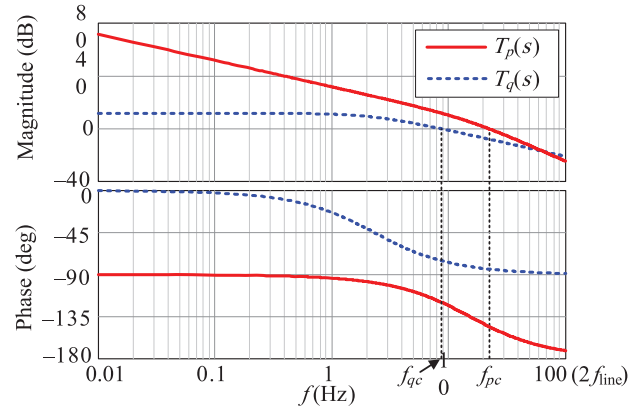


Fig. 7. Bode diagram of the loop gain.

The corner frequency of the first-order low-pass filter in the RPL is expressed as

$$f_{qL} = \frac{D_q K_{iq}}{2\pi}. \quad (41)$$

Similar to the analysis of the APL,  $f_{qL}$  is decreased with the decreasing of  $K_{iq}$ , which means a better DLFR attenuation ability, a reduced PM, and a slower dynamic response. So, there is a tradeoff in choosing  $K_{iq}$ .

As observed in Fig. 5(b), there is only a first-order low-pass filter in the RPL, the maximum phase lag introduced by this filter is  $-90^\circ$ , which means the minimum PM of the RPL is  $90^\circ$ , and the PM requirement is always satisfied. Only the requirement of the DLFR attenuation as well as the dynamic performance needs to be considered.

According to (20), the magnitude of the RPL loop gain at  $2f_{line}$  can be expressed as

$$|T_q(j2\pi \cdot 2f_{line})| = \frac{3V_{on}}{\sqrt{2}X_s D_q} \frac{1}{\left| \frac{j4\pi f_{line}}{D_q K_{iq}} + 1 \right|}. \quad (42)$$

Since  $f_{qL}$  is far below  $2f_{line}$  to ensure the DLFR attenuation, the following approximation can be satisfied:

$$\frac{1}{\left| \frac{j4\pi f_{line}}{D_q K_{iq}} + 1 \right|} \approx \frac{1}{\left| \frac{j4\pi f_{line}}{D_q K_{iq}} \right|}. \quad (43)$$

Thus, (42) can be simplified as

$$|T_q(j2\pi \cdot 2f_{line})| \approx \frac{3V_{on} K_{iq}}{4\sqrt{2}\pi f_{line} X_s}. \quad (44)$$

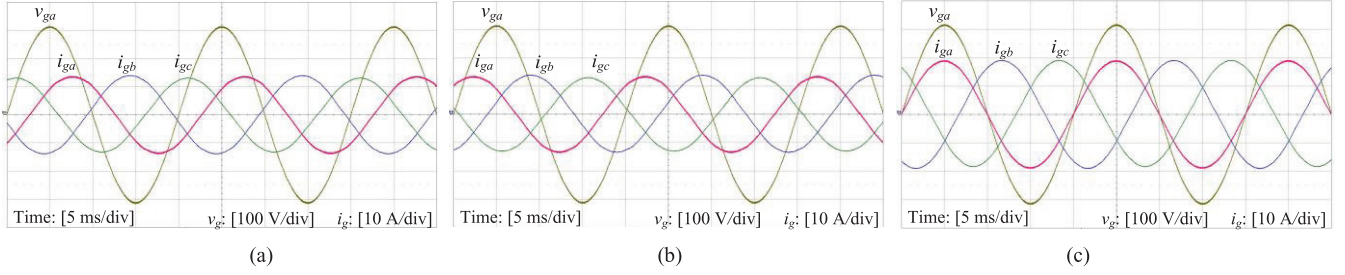


Fig. 8. Steady-state experimental results with  $K_{ip} = 0.06$  and  $K_{iq} = 0.045$ . (a)  $P_{set} = 5$  kW and  $Q_{set} = 5$  kvar (inductive). (b)  $P_{set} = 5$  kW and  $Q_{set} = -5$  kvar (capacitive). (c)  $P_{set} = 10$  kW and  $Q_{set} = 0$  var.

Define  $a_q$  as the magnitude requirement of the loop gain of the RPL at  $2f_{line}$ , then  $|T_q(j2\pi \cdot 2f_{line})| \leq a_q$ . So, we have

$$K_{iq} \leq \frac{4\sqrt{2}\pi f_{line} X_s a_q}{3V_{on}} \triangleq K_{iq\max}. \quad (45)$$

Equation (45) gives the upper limit of  $K_{iq}$ , which is constrained by the requirement of attenuating the DLFR in the RPL. There is no lower limit of  $K_{iq}$ , since the PM requirement of the RPL is always satisfied. However,  $f_{qL}$  is decreased when  $K_{iq}$  decreases, which affects the dynamic performance of the system, so  $K_{iq}$  should not be too small. In practice, it is reasonable to choose  $K_{iq}$  to be slightly smaller than  $K_{iq\max}$  to ensure good attenuation ability, robustness, and dynamic performance.

The design procedure of the parameters of the RPL is similar to that of the APL and is not repeated here.

### C. Design Example

To verify the proposed design method, an example is given. The prototype parameters are given in Table I.

1) **Determination of  $D_p$  and  $D_q$ :**  $D_p$  and  $D_q$  are often determined based on the grid code. According to EN 50438 [24], it is required that the change of 100% active power corresponds to the change of 2% grid frequency, while the change of 100% reactive power corresponds to the change of 10% grid nominal voltage. So, the droop coefficients can be obtained as

$$D_p = \frac{\Delta P_{\max}}{\Delta \omega_{\max}} = \frac{10000}{(2\pi \cdot 50) \cdot 2\%} = 1592 (\text{W} \cdot \text{s/rad}) \quad (46)$$

$$D_q = \frac{\Delta Q_{\max}}{\Delta V_{\max}} = \frac{10000}{220\sqrt{2} \cdot 10\%} = 321 (\text{A}). \quad (47)$$

2) **Determination of  $K_{ip}$ :** For the loop gain of the APL, it is required that  $\text{PM}_{req} = 30^\circ$  and  $a_p = 0.1$ . Based on the specifications and the parameters listed in Table I, according to (33), (37), and (40), the satisfactory curves of  $K_{ip}$  and  $f_{pc}$  are obtained, as shown with the solid line in Fig. 6. As observed, the minimum value of  $K_{ip}$  is constrained by the PM requirement, while the maximum value of  $K_{ip}$  is constrained by the requirement of attenuating the DLFR in the APL. According to Fig. 6,  $f_{pc} = 22$  Hz, which corresponds to point A, is selected. Then,  $K_{ip}$  is calculated as 0.06 from (33).

3) **Determination of  $K_{iq}$ :** As mentioned before, the PM requirement for the RPL is always satisfied, and only the requirement of attenuating the DLFR needs to be considered. By setting  $a_q = 0.1$  and calculating the maximum value of  $K_{iq}$

according to (45), we have  $K_{iq\max} = 0.051$ . Here, we choose  $K_{iq} = 0.045$ .

When  $D_p$ ,  $D_q$ ,  $K_{ip}$ , and  $K_{iq}$  are obtained, the bode diagrams of the loop gains of the APL and RPL are depicted in Fig. 7. As observed, the crossover frequency of the APL is 22 Hz, the PM is  $34.6^\circ$ , and the magnitude of the loop gain at  $2f_{line}$  is  $-24.75$  dB (which corresponds to 0.058). While the crossover frequency of the RPL is 8.6 Hz, the PM is  $105^\circ$ , and the magnitude of the loop gain at  $2f_{line}$  is  $-21.05$  dB (which corresponds to 0.089). It is obvious that all the specifications are satisfied as required.

## VI. EXPERIMENTAL RESULTS

The prototype of a 10-kVA three-phase grid-connected inverter with an LC filter is fabricated and tested in the laboratory. The key parameters of the prototype are listed in Table I. The inverter is implemented using six insulated-gate bipolar transistor modules (CM100DY-24NF), which are driven by M57962L. The grid voltages and the capacitor voltages are sensed by voltage halls (LV25-P). The injected grid currents  $i_g$  are sensed by current halls (LA55-P). All the signals are sampled by a 14-bit A/D converter (MAXIM-1324ECM). The VSG algorithm is implemented in a DSP (TMS320F2812), and the active and reactive powers are calculated in the DSP and are output through a D/A converter (DAC7664). A programmable ac source (Chroma 61512) is used to simulate the grid voltages, for the purpose of arbitrarily setting the frequency and amplitude of the grid voltages to test the dynamic performance of the VSG.

Fig. 8 shows the steady-state waveforms of the VSG with  $K_{ip} = 0.06$ ,  $K_{iq} = 0.045$ ,  $\omega_g = \omega_n$ , and  $V_g = V_n$ . As observed, the system is stable and works well in the steady state.

Fig. 9 shows the dynamic waveforms of the VSG when (a)  $P_{set}$  steps between 5 and 10 kW, and (b)  $Q_{set}$  steps between 5 and 10 kvar. As observed, the output active and reactive powers track their setting values accurately and the overshoot is relatively small. The rising time of the active power is shorter than that of the reactive power, indicating faster dynamic response of the active power. This is because the crossover frequency of the APL (which is 22 Hz) is higher than that of the RPL (which is 8.6 Hz). However, the active power oscillates for a longer time than the reactive power as the PM of the APL (which is  $34.6^\circ$ ) is smaller than that of the RPL (which is  $105^\circ$ ).

Fig. 10 shows the dynamic waveforms of the VSG when (a) the grid frequency drops 1% and then returns back to its



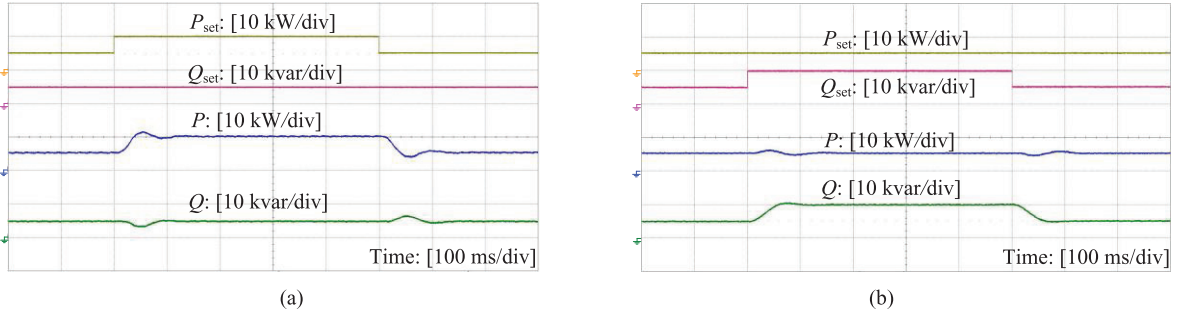


Fig. 9. Dynamic responses with  $K_{ip} = 0.06$  and  $K_{iq} = 0.045$  when (a)  $P_{set}$  steps between 5 and 10 kW and (b)  $Q_{set}$  steps between 5 and 10 kvar.

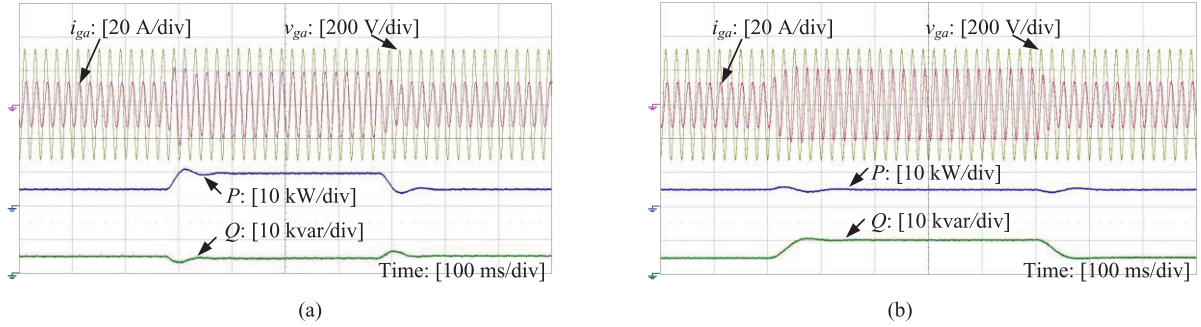


Fig. 10. Dynamic responses with  $K_{ip} = 0.06$  and  $K_{iq} = 0.045$  when (a) grid frequency drops 1% and then returns back to its nominal value and (b) amplitude of grid voltage drops 5% and then returns back to its nominal value.

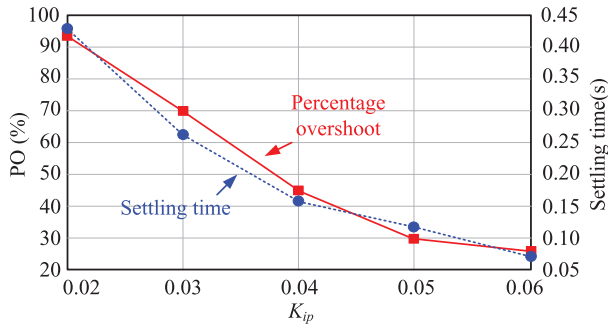


Fig. 11. Settling time and PO of the active power when the grid frequency drops 1% with  $K_{ip}$  varies.

nominal value, and (b) the amplitude of grid voltage drops 5% and then returns back to its nominal value. It can be observed that the VSG changes its output active (reactive) power at the moment when the grid frequency (voltage) changes, which demonstrates that the VSG has the ability of providing grid support.

Figs. 8–10 illustrate that the VSG has satisfactory steady and dynamic performances with  $K_{ip} = 0.06$  and  $K_{iq} = 0.045$ , which verifies the effectiveness of the parameters design method proposed in Section V.

Fig. 11 shows the diagram of the measured settling time and the percentage overshoot (PO) of the active power when the grid frequency drops 1% with different  $K_{ip}$ . When  $K_{ip}$  decreases from 0.06 to 0.02, the settling time increases from 0.08 to 0.42 s, while the PO increases from 24% to 96%. As discussed in Section V, the crossover frequency and PM of the APL are decreased when  $K_{ip}$  decreases, resulting in the degradation of system dynamic performance.

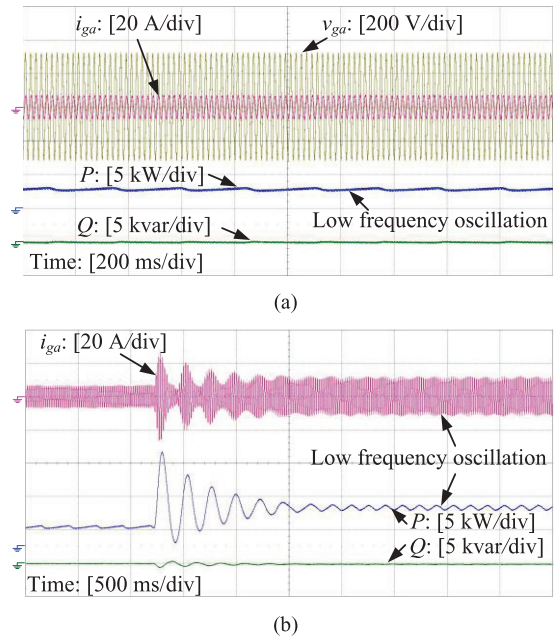
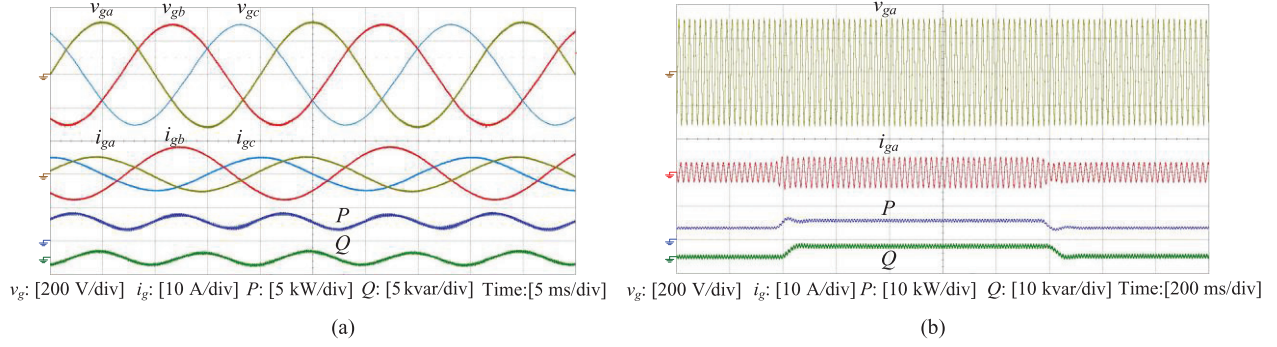
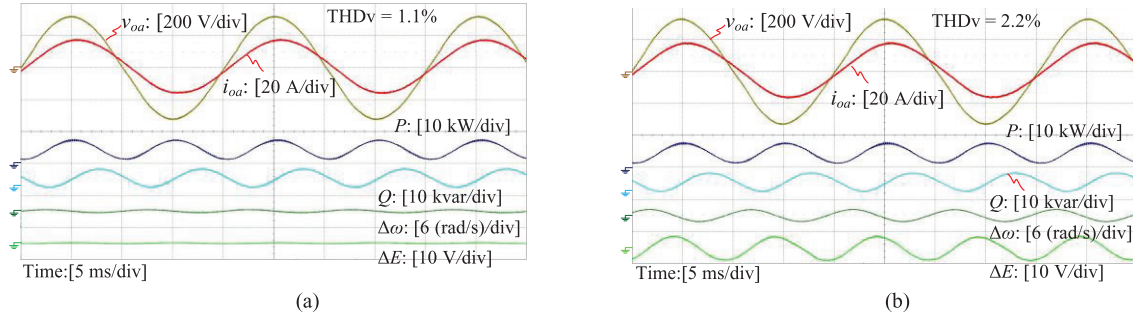


Fig. 12. Experimental results with  $K_{ip} = 0.005$  and  $K_{iq} = 0.045$ . (a) Steady state with  $P_{set} = 3$  kW and  $Q_{set} = 0$  var. (b) Dynamic waveform when the grid frequency drops 0.6%.

Fig. 12 shows the steady-state and dynamic waveforms of the VSG when  $K_{ip}$  is decreased to 0.005, corresponding to point B outside the satisfactory curve in Fig. 6. In this case, the crossover frequency of the APL is 6.93 Hz and the PM is only  $10.4^\circ$ . Obviously, the PM is not large enough to guarantee the system stability. Therefore, the system is more susceptible to disturbance. As a result, low-frequency oscillation appears in the injected grid current and the active power. The experimental



**Fig. 13.** Steady-state and dynamic waveforms of the VSG under unbalanced grid voltage condition. (a) Steady state with  $P_{set} = 3$  kW and  $Q_{set} = 0$  var. (b) Dynamic waveform with power demands step between  $P_{set} = 3$  kW and  $Q_{set} = 0$  var, and  $P_{set} = 6$  kW and  $Q_{set} = 3$  kvar.



**Fig. 14.** Experimental results when VSG works in the standalone mode with 100% unbalanced  $R$ - $L$  loads ( $18 + j3 \Omega$  load in phase A and no load in phase B and phase C). (a)  $f_{pc} = 22$  Hz and  $f_{qc} = 8.6$  Hz. (b)  $f_{pc} = 35$  Hz and  $f_{qc} = 20$  Hz.

results are in well agreement with the line-frequency-averaged small-signal model, and confirm its effectiveness to predict the low-frequency oscillation behavior due to the inappropriately designed control parameters.

Fig. 13 shows the steady-state and dynamic waveforms of the VSG under unbalanced grid voltage condition, the positive and negative-sequences of the grid voltages are set to 0.97 and 0.03 p.u., respectively. As observed, the VSG works stably and the dynamic performance is satisfactory. The output active and reactive powers of the VSG pulsate at  $2f_{line}$  due to the unbalanced grid voltages. As pointed out in [9], the VSG is essentially a voltage-controlled inverter, and its output voltages are controlled to be balanced. Therefore, the unbalanced grid voltages will result in unbalanced injected grid current, which can be observed in Fig. 13(a). How to improve the quality of the injected grid currents under unbalanced grid voltages will be discussed in the near future.

Fig. 14 shows the experimental waveforms when the VSG works in the standalone mode with 100% unbalanced resistive-inductive ( $R$ - $L$ ) loads ( $18 + j3 \Omega$  load in phase A, no load in phase B, and phase C). Due to the unbalanced  $R$ - $L$  loads, the instantaneous output active and reactive powers of the VSG pulsate at  $2f_{line}$ . As discussed in Section III, if not properly attenuated, the DLFR in the instantaneous active power will be reflected in the output frequency of the VSG through the APL, while the DLFR in the instantaneous reactive power will reflect in the amplitude of the output voltage of the VSG through the RPL, which results in the degradation of the quality of the output voltage.

Fig. 14(a) shows the experimental waveforms with the designed parameters ( $f_{pc} = 22$  Hz and  $f_{qc} = 8.6$  Hz, and the corresponding loop gains of the APL and RPL at  $2f_{line}$  are 0.058 and 0.089, respectively). As observed, the output frequency ripple is 0.15 Hz, the ripple of the voltage amplitude is 1.5 V, and the THD of the output voltage is 1.1%. For comparison, Fig. 14(b) shows the experimental waveforms with  $f_{pc}$  and  $f_{qc}$  are deliberately increased to 35 and 20 Hz, respectively (the corresponding loop gains of APL and RPL at  $2f_{line}$  are 0.233 and 0.185, respectively). It can be seen that the output frequency ripple is increased to 0.38 Hz, while the ripple of the output voltage amplitude is increased to 7.5 V, and the THD of the output voltage is increased to 2.2%. The experimental results in Fig. 14 are in well agreement with the theoretical analysis in Section III.

Fig. 15 shows the dynamic waveform of the VSG operating in standalone mode with the designed parameters ( $f_{pc} = 22$  Hz and  $f_{qc} = 8.6$  Hz). The load in phase A steps between no load and  $18 + j3 \Omega$ , while phase B and phase C keep no load. From Fig. 15, it is clear that the VSG responds quickly to the load step changes, and the dynamic performance is satisfactory. Meanwhile, the frequency and amplitude of the output voltage of the VSG are decreased with the increasing output active and reactive power, reflecting the  $P$ - $\omega$  and  $Q$ - $V$  drooping characteristic of the VSG. Reference [25] has pointed out that not only the droop effect, but also the load effect, will cause the output voltage drop when the load is increasing. There are related research discussing how to reduce the voltage drop caused by droop effect and load effect [25], [26], and it is not discussed here.



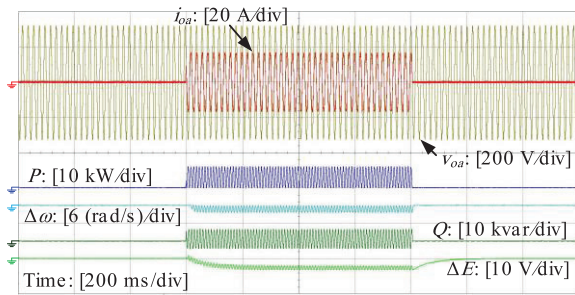


Fig. 15. Dynamic waveform of the VSG operating in the standalone mode with load in phase A steps between no load and  $18 + j3 \Omega$ .

## VII. CONCLUSION

The VSG is the concept of controlling the grid-connected inverter to behave as an SG to take part in the power regulation of the grid when the renewable energy has a high penetration level into the grid. This paper discusses the small-signal modeling and parameters design of the power loops of the VSG. First, this paper points out that the bandwidth of the power control loops of the VSG should be far less than twice the line frequency to attenuate the impact of the DLFR in the instantaneous output power of the VSG, and thus the line-frequency-averaged small-signal model of the VSG is derived. Second, based on the model, the coupling effect between the APL and RPL of the VSG is discussed, and the decoupling conditions between the APL and RPL are analyzed. Finally, a simple step-by-step parameters design method, which takes the requirements of system stability margin, DLFR attenuation, and the dynamic performance improvement into consideration, is proposed in this paper. With this method, the control parameters of the power loop of the VSG can be easily determined without trial-and-error. A 10-kVA prototype is fabricated and tested in the laboratory, and the experimental results are given to verify the effectiveness of the theoretical analysis and the proposed parameters design method.

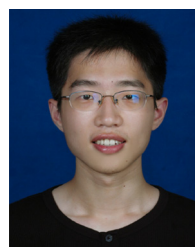
## ACKNOWLEDGMENT

The authors would like to thank L. Jia, a Master's student from Nanjing University of Aeronautics and Astronautics, for his great support in the experimental verification and paper revision.

## REFERENCES

- [1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
- [2] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, IEEE Std. 1547-2003, Jul. 28, 2003.
- [3] *Characteristics of the Utility Interface for Photovoltaic (PV) Systems*, IEC 61727, 2004.
- [4] T. Loix, "Participation of inverter-connected distributed energy resources in grid voltage control," Ph.D. dissertation, Dept. Elect. Eng., Katholieke Univ. Leuven, Leuven, Belgium, 2011.
- [5] H.-P. Beck and R. Hesse, "Virtual synchronous machine," in *Proc. 9th Int. Conf. Elect. Power Qual. Util. (EPQU)*, 2007, pp. 1–6.
- [6] Y. Chen, R. Hesse, D. Turschner, and H.-P. Beck, "Improving the grid power quality using virtual synchronous machines," in *Proc. Int. Conf. Power Eng. Energy Elect. Drives (POWERENG)*, 2011, pp. 1–6.

- [7] Q.-C. Zhong and G. Weiss, "Static synchronous generators for distributed generation and renewable energy," in *Proc. Power Syst. Conf. Expo. (PSCE)*, 2009, pp. 1–6.
- [8] Q.-C. Zhong and G. Weiss, "Synchronverters: Inverters that mimic synchronous generators," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1259–1267, Apr. 2011.
- [9] Q.-C. Zhong, P.-L. Nguyen, Z. Ma, and W. Sheng, "Self-synchronised synchronverters: Inverters without a dedicated synchronisation unit," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 617–630, Feb. 2014.
- [10] D. Arco and J. Suul, "Equivalence of virtual synchronous machines and frequency-droops for converter-based microgrids," *IEEE Trans. Smart Grid*, vol. 5, no. 1, pp. 394–395, Jan. 2014.
- [11] X. Li *et al.*, "Power management unit with its control for a three-phase fuel cell power system without large electrolytic capacitors," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3766–3777, Dec. 2011.
- [12] Y. Du, J. Guerrero, L. Chang, J. Su, and M. Mao, "Modeling, analysis, and design of a frequency-droop-based virtual synchronous generator for microgrid applications," in *Proc. Energy Convers. Congr. Expo. (ECCE Asia)*, 2013, pp. 643–649.
- [13] S. Arco, J. Suul, and O. Fosso, "Control system tuning and stability analysis of virtual synchronous machines," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2013, pp. 2664–2671.
- [14] E. Coelho, P. Cortizo, and P. Garcia, "Small signal stability for single phase inverter connected to stiff ac system," in *Proc. IEEE IAS Annu. Meeting*, 1999, pp. 2180–2187.
- [15] J. Guerrero, L. García de Vicuña, J. Matas, M. Castilla, and J. Miret, "A wireless controller to enhance dynamic performance of parallel inverters in distributed generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1205–1213, Sep. 2004.
- [16] J. Guerrero, J. Matas, L. García de Vicuña, M. Castilla, and J. Miret, "Decentralized control for parallel operation of distributed generation inverters using resistive output impedance," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 994–1004, Apr. 2007.
- [17] H. Akagi, E. Watanabe, and M. Aredes, *Instantaneous Power Theory and Applications to Power Conditioning*. Piscataway, NJ, USA: IEEE Press, 2007.
- [18] X. Chen, X. Ruan, D. Yang, H. Wu, and W. Zhao, "Step-by-step controller design of voltage closed-loop control for virtual synchronous generator," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2015, pp. 3760–3765.
- [19] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.
- [20] P. Kundur, *Power System Stability and Control*. New York, NY, USA: McGraw-Hill, 1994.
- [21] J. Guerrero, L. García de Vicuña, J. Matas, M. Castilla, and J. Miret, "Output impedance design of parallel-connected UPS inverters with wireless load-sharing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126–1135, Aug. 2005.
- [22] S. Hu, *Automation Control Theory*, 5th ed. Beijing, China: Science Publishing House, 2007.
- [23] *Technical Rule for Distributed Resources Connected to Power Grid*, Q/GDW 480-2010, 2010.
- [24] *Requirements for the Connection of Micro Generators in Parallel With Public Low-Voltage Distribution Networks*, EN 50438, 2008.
- [25] Q.-C. Zhong, "Robust droop controller for accurate proportional load sharing among inverters operated in parallel," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1281–1290, Apr. 2013.
- [26] Q.-C. Zhong and T. Hornik, *Control of Power Inverters in Renewable Energy and Smart Grid Integration*. Hoboken, NJ, USA: Wiley/IEEE Press, 2013.



**Heng Wu** was born in Jiangsu Province, China, in 1990. He received the B.S. degree in electrical engineering and automation and the M.S. degree in power electronic engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2012 and 2015, respectively.

He is currently an Electrical Engineer with NR Electric Co., Ltd., Nanjing, China. His research interests include digital control techniques, renewable energy generation systems, and flexible ac transmission systems (FACTS).



**Xinbo Ruan** (M'97–SM'02–F'16) received the B.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively.

In 1996, he joined the College of Automation Engineering, NUAA, where he became a Professor in 2002. From 2008 to 2011, he was also with the College of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China. He has authored/coauthored seven books and more than 200 technical papers published in journals and conference proceedings. His research interests include soft-switching power electronics converters, power electronics system integration, and renewable energy generation systems.

Dr. Ruan served as Vice President of the China Power Supply Society from 2005 to 2013. Currently, he serves as an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING.



**Dongsheng Yang** (S'13) was born in Jiangsu Province, China, in 1984. He received the B.S. and M.S. degrees in electrical engineering and automation from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2008 and 2011, respectively, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include grid-connected inverter control and renewable energy generation systems.



**Xinran Chen** was born in Jiangsu Province, China, in 1990. He received the B.S. degree in electrical engineering and automation from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2013, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include digital control techniques and renewable energy generation systems.



**Wenxin Zhao** was born in Jiangsu Province, China, in 1991. He received the B.S. degree in electrical engineering and automation from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2014, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include digital control techniques and renewable energy generation systems.



**Zhipeng Lv** was born in 1984. He received the Ph.D. degree in electrical and information engineering from Hunan University, Changsha, China, in 2012.

He is currently an Electrical Engineer with the China Electric Power Research Institute, Beijing, China. His research interests include smart grids and renewable energy generation systems.



**Qing-Chang Zhong** (M'04–SM'04) received the Ph.D. degree in control and power engineering from Imperial College London, London, U.K., in 2004 (awarded the Best Doctoral Thesis Prize), and the Ph.D. degree in control theory and engineering from Shanghai Jiao Tong University, Shanghai, China, in 2000.

He holds the Max McGraw Endowed Chair Professor in Energy and Power Engineering with the Department of Electrical and Computer Engineering, Illinois Institute of Technology,

Chicago, IL, USA.

Dr. Zhong is a Fellow of the Institution of Engineering and Technology (IET), U.K., the Vice-Chair of the IFAC Technical Committee on Power and Energy Systems, and was a Senior Research Fellow of the Royal Academy of Engineering, U.K. (2009–2010) and the U.K. Representative to the European Control Association (2013–2015). He serves as an Associate Editor for the IEEE TRANSACTIONS ON AUTOMATIC CONTROL, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON CONTROL SYSTEMS TECHNOLOGY, IEEE ACCESS, and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is a Distinguished Lecturer of the IEEE Power Electronics Society and the IEEE Control Systems Society.