A BENCHMARK MODEL FOR HVDC SYSTEM STUDIES

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INTRODUCTION

The idea of establishing a benchmark system to study certain phenomena is not new. However this is a first attempt to create a common reference for HVDC studies, especially one related to control strategies and recovery performance.

Another benefit that results from such a standard system is the possible comparison of different simulation methods and results.

In another publication by Szechtman et al (1), results obtained from distinct simulators/computer programs have been shown, indicating that the "well-established" simulation sources led to nearly identical results, for the same set of parameters.

In this paper, some aspects that have not been discussed by Szechtman et al in (1) are presented, such as assumptions and reasons for selecting the HVdc benchmark model as it is now, with the objectives of promoting more discussions on this subject, and evolving the degree of information and exchange among power system engineers.

This work results from a joint effort of regular members of CIGRE Working Group 14-02 (Control in HVdc Systems) which have undertaken the task of developing and presenting a benchmark system for dc control studies.

THE BENCHMARK SYSTEM

The system configuration described in Figure 1 is being considered as benchmark no. 1. In the future, depending on the impact of subsequent experience, other configurations could be selected as benchmark numbers 2, 3, etc.

The system adopted as benchmark no. 1 has been proposed by Ainsworth in (2) and will be briefly described. The rated frequency is 50 Hz.

In the selection of parameters some degree of "difficulty" was intended in order to make this benchmark system really a significative and suitable exercise.

The ac System Representation

Different ac system equivalents have been selected at both ends of the HVdc system. At the rectifier a R-R-L circuit was chosen which provides the same impedance angle of 84° for the fundamental and third harmonic. This is likely to be more representative of a region where power generation is predominant. The R-L-L circuit chosen for the inverter side exhibits a higher damping at third harmonic as compared to fundamental, with impedance angles of 69° and 75°, respectively. This is more representative for an inverter in close proximity to loads.

The short-circuit-ratio (SCR) at both ends has been chosen as 2.5, giving an effective ratio (ESCR) of 1.9 (with damping angle of 70° and 82° at the inverter and rectifier respectively). These figures can be considered as "mean" values for low SCR ac/dc systems and provide some degree of difficulty to the dc controls. In another publication by Wess et al (3), simulations were carried out with SCR lower than 2.

Reactive Compensation Arrangement

The converter reactive compensation is provided by a combination of capacitor banks and ac filters, as shown in Figure 1.

The ac filters are of the damped-arm type. In order to verify the influence of this type of filter arrangement upon system performance, comparative simulations were also carried out with tuned-arm (11th and 13th) filters. The behaviour of the system was practically the same for both cases, leading to the conclusion that in this case, a higher degree of filter losses found in the damped-arm type does not have a dominant influence upon the results.

The ac system plus filters/capacitor banks at the inverter end shows an impedance versus frequency characteristic as depicted in Figure 2. It is clearly evident a parallel resonance very close to the 2nd harmonic. This is a deliberate "difficulty" included in the system.

The dc Line

The dc line parameters were chosen to represent a high voltage cable of about 100 Km length. High capacitances normally give rise to more problems as far as dc control settings are concerned. Figure 3 shows its impedance variation with frequency.

The input impedance of the dc cable plus smoothing reactors has a minimum of 5Ω or 0.02 pu at f = 56.5 Hz and a maximum of 9.25 kΩ or 37 pu at f = 40 Hz. The combination of antiresonance at the 2nd harmonic on the ac side, and resonance at approximately the fundamental on the dc side is another particularity onerous but deliberate "difficulty". The presence of a 2nd uncharacteristic harmonic in the ac would cause a 1st and a 3rd component in the dc. In turn, a fundamental component on the dc side causes a dc component and a 2nd (at the antiresonant frequency) on the ac side. The dc component can cause transformer saturation, and this, in combination with the harmonic transfer loops may impose

unfavourable conditions on the dc control actions.

Converter Stations

The converter stations are represented by one-12 pulse group per station. Both the rectifier firing angle and inverter extinction angle are assumed to be 15 degrees.

Converter Transformers

The parameters adopted (based on ac rated conditions) are considered as typical for transformers found in HVDC installations such as leakage reactance: x = j*0.18 pu; saturated reactance, primary: xls = j*0.344 pu, secondary: x2s = j*0.172 pu; mutual reactance in the saturated state: Ms = j*0.168 pu; voltage at the saturation limit: 1.22 pu. A more detailed description of these characteristics can be found in Szechtman et al (1).

DC CONTROL SYSTEM

Figure 4 shows the steady-state Vd x Id characteristic utilized in the simulation.

The characteristic CBA of the inverter is used primarily to increase current margin in the recovery process after faults, where the increased current margin speeds up the dc voltage recovery. Another purpose is that the risk of commutation failures will be reduced in the recovery period after rectifier ac faults as pointed out by Joetten et al (4). Such commutation failures can occur if the current margin method alone would be applied. Also, it should be noted that the DCBA characteristic represents a positive apparent resistance, always giving stable operating points when the rectifier characteristic XY is shifted downwards.

The characteristic CBA is similar to one published earlier by Bowles (5) and provides approximately a constant reactive consumption which can be very important to improve system performance as shown by Szechtman et al (6). The characteristic CD is similar to the usually found current error control.

A sudden voltage decrease in the inverter ac system may lead to commutation failures, causing collapse of the inverter dc voltage and a current overshoot followed by a phase-back in the rectifier current controller. It is common practice to reduce the current reference at the rectifier when the dc voltage is depressed by the inverter side. This is the so-called voltage-dependent-current-order limit (VDCOL).

The VDCOL, once activated is characterized by an unavoidable delay due to the ramping up process, the speed of which can be selected slow enough to avoid the occurrence of postfault commutation failures.

However, it has been postulated by Joetten (7) that following a commutation failure at the inverter, due to an ac fault for instance, the inverter dc current need not be reduced to zero, or to a minimum level, by the rectifier control, and that the inverter is able to recover even without current reduction and without an undesirable voltage reversal, if the usually provided alpha-min-limit for the inverter is flexibly adapted to the type of fault.

This philosophy was incorporated in the control system and the simulation results demonstrate its adequacy to low SCR ac/dc systems. Therefore current reduction during faults to relieve the ac system, may not be an essential measure.

It should also be mentioned that the adopted characteristics apply only for short-time disturbances. For longer duration faults, a VDCOL action would be required at the rectifier to protect the inverter valves. In the cases simulated here, only short-time (5 cycles) faults have been applied.

SIMULATION RESULTS

For preparation of the CIGRE report by Szechtman et al (1), the benchmark system was set up in the following simulation sources:

- FGH Parity Simulator
- EMTDC
- EMTP
- NETOMAC

The results achieved full agreement. Therefore, in this paper only results obtained with the real-time parity simulator will be shown.

In the oscillograms of Figures 5, 6 and 7, the following traces are shown:

V_a,rec	Phase a, b and c voltage at the rectifier ac bus
V_b,rec	
V_c,rec	
V_a,inv	Phase a, b and c voltage at the inverter ac bus
V_b,inv	
V_c,inv	
V_dL	Mid-point dc cable voltage
I_d,rec	dc current at the rectifier side
I_d,inv	dc current at the inverter side

Figure 5 shows the results for a three-phase inverter ac fault. The characteristic shown in Figure 4 is used, so the rectifier current control maintains full current during the fault period. In the gate control unit, the pulses are continued after the voltage collapse, referred to the alpha-zero-reference marks stored from prefault conditions. This leads to a valve bypass and relieves the transformer from dc current circulation in its windings.

Because of the "difficulties" pointed out earlier, a good coordination between rectifier and inverter control strategies becomes necessary in order to counteract with the influence of transformer inrush current, visibly superimposed on the fundamental, and which dies out quite slowly.

It is also interesting to notice that there are no ac overvoltages in the post clearing period, since dc power and consequently the normal reactive consumption are quickly restored.

Figure 6 shows the results obtained when applying a dc fault at the rectifier cable end.

For dc faults in overhead lines, the usual method to clear the fault is by control action of converters, without relying on circuit breakers or other switching equipment. The dc line protection distinguishes the line fault from commutation failures mainly by the step voltage waves along the line. Thus the protection reaction was included in this case, although the dc side parameters of the benchmark system are those of a cable. The protective reaction is a controlled setting of the rectifier firing angles into inverter range after a delay of 20 ms. The current control prevents an excessive overcurrent, independently from the line protection. The direct current reaches zero 30 ms after fault initiation. After a preset waiting time, 200 ms in this case, the firing angles are reset to initial values and then changed until the current control and the extinction angle control take over at the rectifier and inverter, respectively.

The recovery is relatively fast and smooth. During the fault period, because of the lack of current, there is a temporary ac voltage rise, reaching 1.4 pu and 1.3 pu at the rectifier and inverter ends respectively, and with the consequent appearance of slight voltage distortions.

To complete the set of simulations Figure 7 shows the results obtained for a three-phase fault at the rectifier ac system. During the fault period, the influence of the CBA characteristic can be observed, keeping the current level at approximately 0.4 pu. The recovery in this case differs from the case of the inverter fault, showing more distorted oscillograms in the dc quantities. In both cases, no commutation failures were observed.

CONCLUSIONS

A first benchmark dc system has been established for the purpose of comparing various dc control strategies, recovery performances and different simulation methods and results.

The benchmark system deliberately includes some onerous conditions for dc control operation, namely employing low ESCR connected systems, a filter/system parallel resonance near 2nd harmonic, and a dc side (with cable) resonance at fundamental frequency.

The benchmark system has been "tested" using a number of simulator/digital models with excellent comparative results.

Results are shown from a benchmark simulation using a particular control strategy and for inverter, dc line and rectifier side faults. In this case, rectifier current reduction during inverter side faults was not found to be an essential measure to produce good dc recovery in a low ESCR system.

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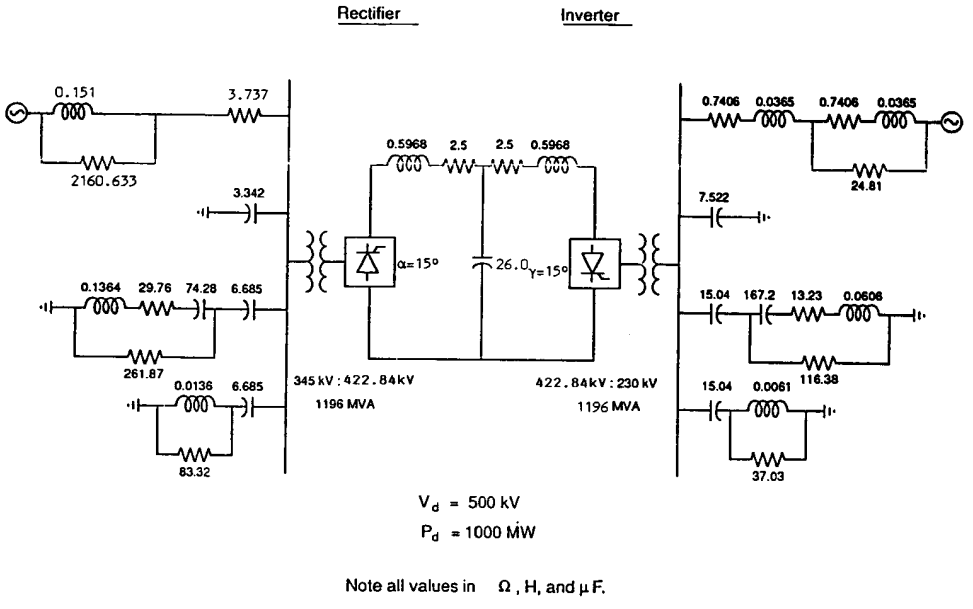

Figure 1 Benchmark ac/dc system configuration

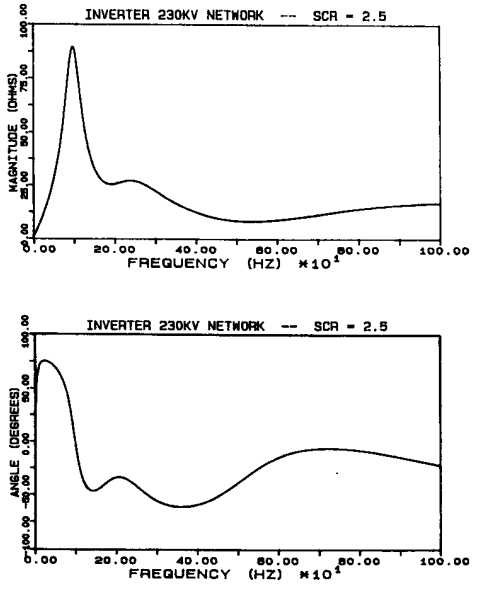

Figure 2 Inverter ac system impedance with frequency
a) magnitude characteristic; b) angle

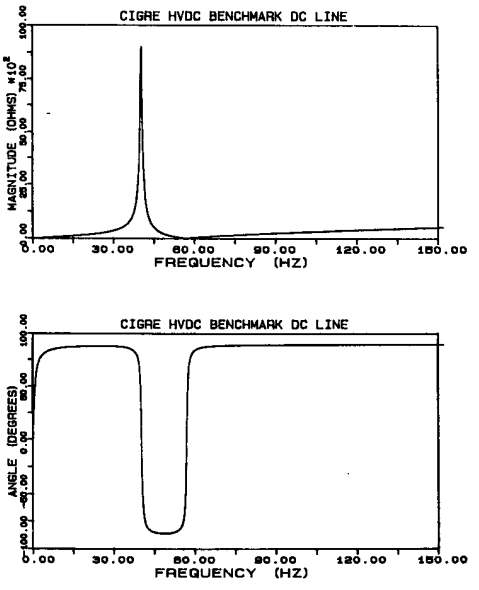

Figure 3 Impedance versus frequency characteristic of the dc line
a) magnitude characteristic; b) angle

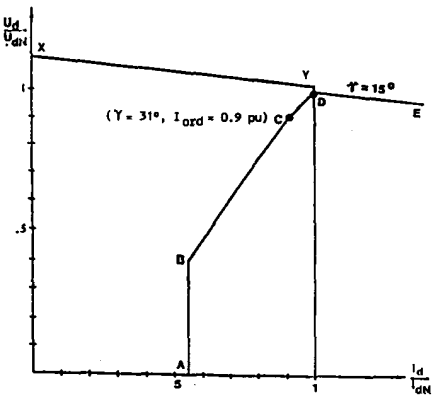

Figure 4 Steady-state Vd x Id characteristic

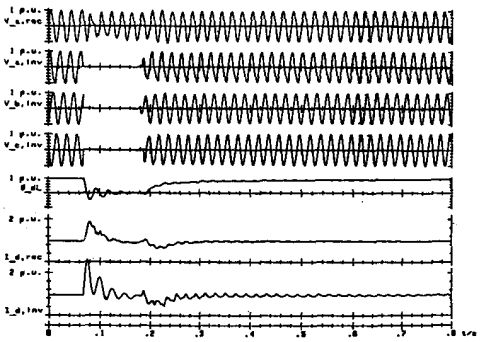

Figure 5 Oscillograms for a 3-phase inverter ac system fault

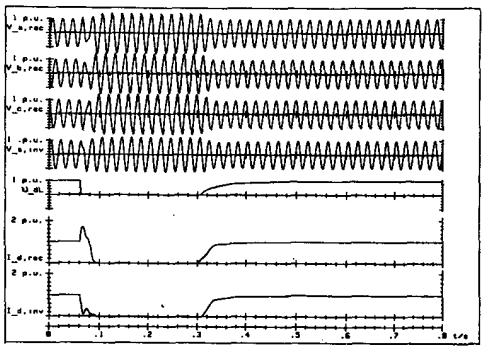

Figure 6 Oscillograms for a dc fault at the rectifier cable end

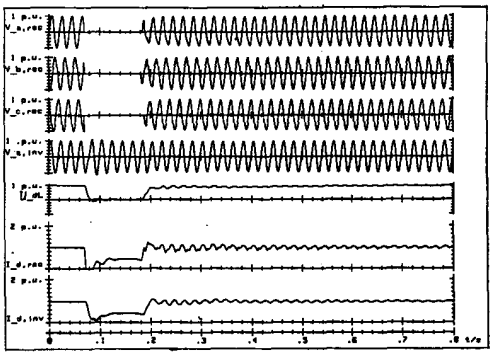

Figure 7 Oscillograms for a 3-phase rectifier ac system fault