

Modeling of CIGRE HVDC Benchmark System in MATLAB/ SIMULINK

¹A.Tirupati Rao, ²P.Ramana, ³P. Kanata Rao

^{1,2,3}Dept. of EEE, GMRIT, Rajam, Srikakulam, AP, India

Abstract

A benchmark system provides a good common base for trying out the new concepts and to make comparisons between the simulation results and published results. This benchmark system has a rather simple, but operationally difficult configuration. It is a two terminal DC scheme where the main circuit values proposed are arbitrary and do not represent any particular HVDC scheme. The main purpose of this benchmark model proposed by CIGRE is to encourage comparison of performance of different DC control equipment and strategies of various manufacturers and institutes by means of HVDC simulator or digital computer studies made on this model

Keywords

Voltage Dependent Current Order Limiter, Commutation Failure Prevention Control, CIGRE

I. Introduction

High Voltage Direct Current Technology is a most attractive transmission technology when power has to be transmitted over long distances. The first commercial HVDC transmission project has been installed in Sweden in 1954. In last half century, its application has widely increased. A total of around 70000MW of transmission capacity is transmitted around the world through 95 HVDC projects [1]. Due to the burgeoning demand for electrical power in one area and concentration of electrical generation in another area, a number of high capacity long distance HVDC systems are planned where bulk power from one region to another region is being transmitted.

II. CIGRE HVDC Benchmark System

The first CIGRE HVDC benchmark system shown in fig. 1 was proposed in 1985. The system is a mono-polar 500-kV, 1000-MW HVDC link with 12-pulse converters on both rectifier and inverter sides, and connected to weak AC systems (short circuit ratio of 2.5 at a rated frequency of 50Hz) that provide a considerable degree of difficulty for DC controls.

AC filters are added to absorb the harmonics generated by the converter as well as to supply reactive power to the converter. The simulation of CIGRE HVDC Benchmark System is carried out in MATLAB/SIMULINK.

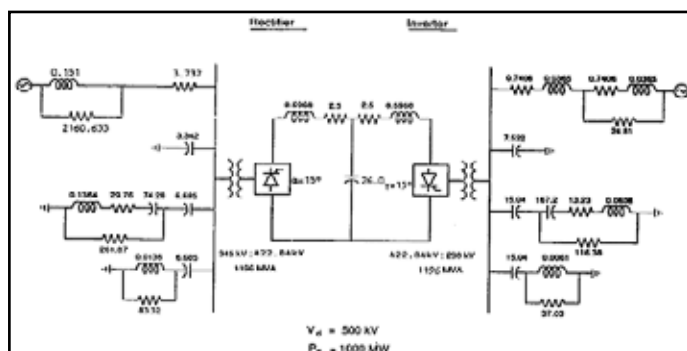


Fig. 1: First CIGRE HVDC Benchmark System

Table 1: Details of First CIGRE HVDC Benchmark System

Parameters	Rectifier side	Inverter side
Base AC voltage	345kV (Line –Line)	230kV (Line –Line)
Base Power	1000 MW	1000 MW
Base Impedance	119.03 Ω	52.9 Ω

III. Modeling of CIGRE HVDC Benchmark System

A. Modeling of AC System at Rectifier and Inverter

AC system at Rectifier and Inverter in MATLAB is modeled as balanced sinusoidal three phase infinite bus voltage behind impedance. The source impedance at rectifier is modeled as R, RL parallel type and at inverter is modeled as impedance type. At the inverter there is an additional series RL branch (0.7406 Ω and 0.0365 H) in the CIGRE benchmark model is also modeled.

Table 2: Parameters Entered in the MATLAB for AC System at Rectifier and Inverter

Parameters	Rectifier side	Inverter side
System Frequency	50Hz	50Hz
Source Voltage (L-L, RMS)	345kV	230kV
R,RL parallel Impedance $R_s + (R_p // L_p)$	$R_s = 3.737 \Omega$ $R_p = 2160.633 \Omega$ $L_p = 0.151 \text{ H}$	$Z_1 = 10.177 \Omega, \Phi_1 = 62.140$, Additional RL Branch $R_s = 0.7406 \Omega$ $L_s = 0.0365 \text{ H}$

B. Modeling of Converter Transformer & Valve Parameters

The converters along with the converter transformers are modeled using six pulse share valve group present in MATLAB. This valve group has the facility to model firing and valve blocking controls, current and extinction angle measurements, optional dc reactor, built-in RC Snubber circuits for each thyristor etc. Thyristor valves are modeled as ideal devices and therefore, negative turn-off and firing due to large (dv/dt) or (di/dt) are not considered. Transformers are modeled by three phase two winding transformer; one with grounded Y- Y connection and the other with grounded Y- Δ connection.

C. Modeling of DC System

DC system parameters are given below, these are taken as the base values while modeling the control circuit. The DC line is modeled using an equivalent T network with smoothing reactors inserted on both sides. The R, L, C values of DC line including the smoothing reactor is given below.

Table 3: DC System Parameters

Parameters	DC side
Base Voltage	500 kV
Base Current	2000 A
Base Impedance	250 Ω
Base Power	1000 MW

Table 4: R, L, C Parameters for DC line

Parameters	DC side
Reactance on each side	0.5968 H
Resistance on each side	2.5 Ω
Capacitance	26.0 μ F

D. Modeling of AC Filters at Rectifier

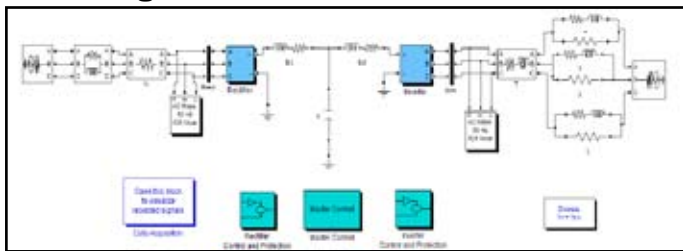


Fig. 2: CIGRE HVDC Benchmark System

The AC filters modeled in rectifier side as MVAR, Quality factor and tuning frequency are calculated by using R, L, C values.

With all the input parameters explained above, the schematic of CIGRE HVDC benchmark system modeled in MATLAB is shown in fig. 2.

IV. Steady State Characteristics of CIGRE HVDC Benchmark System

A. Rectifier Operating Characteristics

The Initial rectifier voltage at R_1 in the characteristic is given by

$$V_d = \frac{3\sqrt{2}}{\pi} V_l \cos \alpha \quad (1)$$

Rectifier is operated in minimum α mode from R_1 to R_2 governed by the equation

$$V_d = \frac{3\sqrt{2}}{\pi} V_l \cos \alpha - \frac{3\omega l}{\pi} I_d \quad (2)$$

Rectifier is operated in constant current controller mode from R_2 to R_3 governed by the equation

$$V_d = \frac{3\sqrt{2}}{\pi} V_l \cos \alpha - \frac{3\omega l}{\pi} I_{d(const)} \quad (3)$$

B. Inverter Operating Characteristics

Inverter is operated in constant extinction angle mode from I_1 to I_2 governed by equation

$$V_d = \frac{3\sqrt{2}}{\pi} V_l \cos \gamma - \frac{3\omega l}{\pi} I_d \quad (4)$$

Inverter controller is operated in constant current control mode from I_1 to I_3 governed by the equation

$$V_d = \frac{3\sqrt{2}}{\pi} V_l \cos \beta + \frac{3\omega l}{\pi} I_d \quad (5)$$

Where $\beta = \pi - \alpha$ is called the conduction angle.

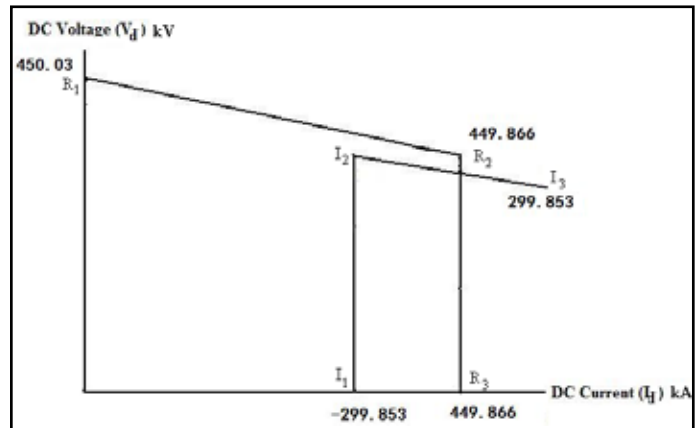


Fig. 3: Modified Rectifier & Inverter Characteristics

From the above values derived at rectifier and inverter the steady state HVDC characteristic are shown in fig. 3.

V. Modeling of HVDC Controllers

A. Master Control

Master control generates the reference currents for the Rectifier as well as Inverter. To avoid loss of margin these rectifier and inverter reference currents should be equal. The converter starting and stopping is ignited by the master controller and the current reference can be ramped up or down. A current step can be added to the current reference for testing purpose. At start up both converters are de blocked and ramped up to minimum current allowed in steady-state with an adjustable time in the "Start/Stop & ramping unit" subsystem. After the system stabilization the current is ramped up to its final value with an adjustable rate and execution time. Before stopping the converters the current is ramped down to the minimum reference.

In the Master control, pulse generators are de-blocked and the power transmission started by ramping the reference current at $t=20$ msec. The reference reaches the minimum value of 0.1 pu in 0.3 sec. At $t=0.4$ sec, the reference current is ramped from 0.1 to 1 pu (2kA) in 0.18s (5pu/s). The DC current reaches to steady state, at the end of the starting sequence at approximately 0.58s. The rectifier controls the current and the inverter controls the voltage. Master control circuit modeled as shown in fig. 4.

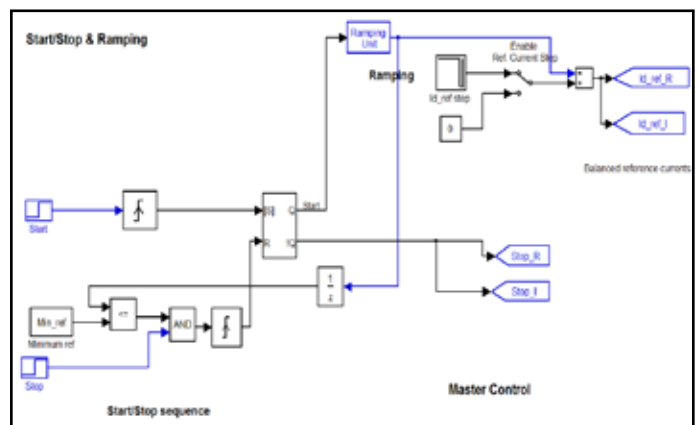


Fig. 4: SIMULINK Diagram of Master Control

B. Voltage Dependent Current Order Limiter (VDCOL)

Another important control function VDCOL is implemented to change the reference current according to the value of the DC voltage. This control automatically reduces the reference current (I_{d-ref}) set point when V_d decreases. Reducing the I_d reference currents also reduces the reactive power demand on the AC system, helping to recover from fault. The I_{d-ref} valve starts to decrease when the V_d line voltage falls below a threshold value $V_{d-thresh}$ (0.6).

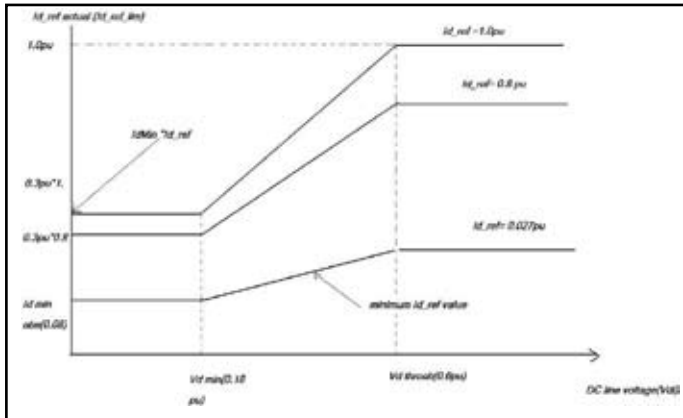


Fig. 5: Characteristic of VDCOL

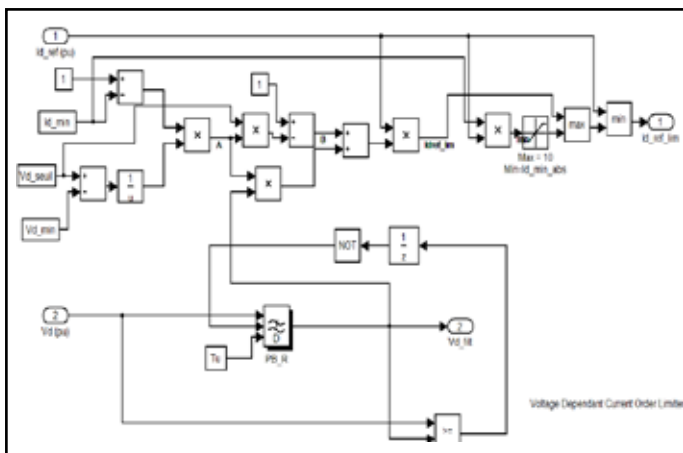


Fig. 6: Voltage Dependent Current Order Limiter

The actual reference current used by the controllers is available at the second Controller's output, named $I_{d-ref-lim}$. $I_{d-minabs}$ is the absolute minimum I_{d-ref} value, set at 0.08 pu. When the DC line voltage falls below the V_d thresh value, the VDCOL drops instantaneously to I_{d-ref} . However, when the DC voltage recovers, VDCOL limits the I_{d-ref} rise time with a time constant defined by parameter T_{up} (Ex: 80 ms). VDCOL circuit is modeled as shown in fig. 6.

C. Commutation Failure Prevention Control (CFPREV)

The protective function, used in the inverter mitigates commutation failures due to AC voltages dips. After fault detection (3- ϕ or 1- ϕ) a value (γ_{min} -CFPREV) is sent to the converter in order to be deducted from the maximum delay angle limit (α -max). Practically the commutation margin is consequently enlarged reducing the risk of commutation failure. The Clark's transformation is used for 3- ϕ fault detection and the zero-sequence voltage evaluation. The detection is based on instantaneous values, which ensure fast reaction of the control system when AC faults occur. Commutation failure prevention control is modeled as shown in fig. 7.

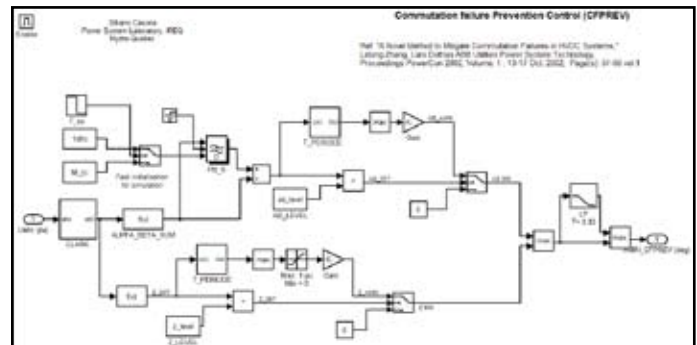


Fig. 7: Commutation Failure Prevention Controller

VI. Simulation Results

The simulation of first CIGRE HVDC Benchmark system modeled in MATLAB/SIMULINK. To study the simulation result, AC fault at inverter side is created [9]. The fault component is modeled as 3 phase line to ground fault at inverter bus and the controls are build to apply the fault at a specific point on wave and for required duration. The fault is initiated at the positive zero crossing of the phase. A voltage for a duration of 5 cycles is observed. Inverter Phase voltages, phase voltage of the rectifier, DC Current of the Inverter as well as Rectifier, Midpoint DC voltage for this particular fault are plotted in fig. 8. From the results it is observed that the HVDC controls response is as per the requirement.

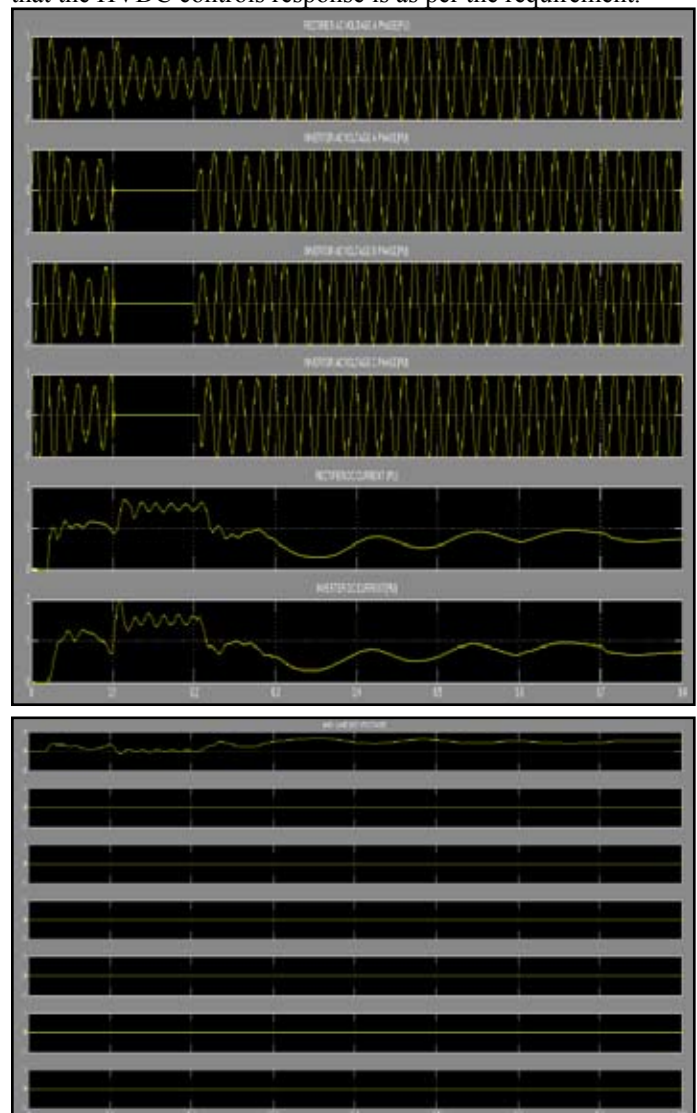


Fig. 8: Simulation Results for a 5-cycle 3-phase Inverter Fault

VII. Conclusion

This paper presents Simulation of CIGRE HVDC Benchmark System carried out in MATLAB/SIMULINK. The HVDC controls are modeled in detail in MATLAB to test the performance of HVDC BENCH MARK system. Simulation results are verified for 3Phase to ground fault at inverter and found that obtained results are satisfactory.

References

- [1] D.Madhan Mohan, Bhim Singh ,B.K Panigrahi “HVDC Technology for Power Transmission”, July 2008, Electical India
- [2] Dipti Khare, C.Prabhakar, K.S.Meera, P.V. Balasubramanya-m, Sujitha Subhash,A.K Tripathy,“RTDS Simulation Studies on the upcoming Multi—infeed HVDC Systems in India” B4-106,CIGRE 2008,CPRI Bangalore India.
- [3] Paulo Fischer de Toledo, Bernt Bergdhal, Gunnar Asplund, “Multiple Infeed Short Circuit Ratio – Aspects related to Multiple HVDC into one AC Network”, 2005 IEEE/PES, Transmission and Distribution Conference &Exhibition: Asia and Pacific, Dalian, China
- [4] Lidong Zhang, Lars Dofnas,“A Novel Method to mitigate Commutation Failures in HVDC systems”, International conference on power systems technology 2002, proceedings. POWERCON-2002, Vol. 1.
- [5] K.R.Padiyar,“HVDC power Transmission Systems”.
- [6] IEEE Guide for planning DC Links Terminating at AC Locations Having Low Short- Circuit Capacities,“IEEE Std 1204-1997”.
- [7] Working Group B4-41. CIGRE,“Systems with Multiple HVDC In feed”.
- [8] E.Rahimi, A.M.Gole, J.B.Davies, I.T.Fernando, K.L.Kent “Commutation Failure in Single – and Multi-in feed HVDC Systems” The 8 th IEEE international conference on AC and DC power Transmission 2006.
- [9] M.Szechtman, T.Wess, C.V.Thio,"First Benchmark Model for HVDC control studies", CIGRE -WG 14.02., ELECTRA, No. 135, PP.54-73, April 1991.
- [10] M.D.Singh, K.B.Khanchandani,“Power Electronics”.
- [11] J.Arrillaga, D. A.Brodley, P. Sbodger,“Power System Harmonics”.