ECE-447-CMU-Homework

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Homework 1

- Paper summary
  - *Requirements, Bottlenecks, and Good Fortune: Agent for Microprocessor Evolution -- Proceeding of IEEE 2001*
    - From the part I "Basic Framework", we can conclude that computer architecture is a science of "tradeoffs". When we talk about microprocessor, we often talk about ISA, microarchitecture, and circuits. The ISA is implements upon a set of hardware structures collectively referred to as the microarchitecture. Each hardware structure and its interconnections are made of electronic digital circuits. For the design of a microprocessor, it depends on who we design for, some customers' most important consideration is the high availability, therefore we can accept lower performance and high cost. In other cases, a little loss in performance is acceptable as long as it is combined with substantial savings in energy requirements. In each case, **it is the problem we are addressing that dedicate the design and the resulting tradeoffs that must be made.** The basic three parts of process is 1) supply the instruction to the core 2) supply the data the instruction need to the core 3) perform the operations required by each instruction.
    - From the part II "Agents for evolution", we can conclude that there are three pieces of main factors that piques the evolution of microprocessor. The first is new requirement. In this paper, the author mentioned power consumption and human-computer interaction. At present, it seems that the two factors are still new requirements that motivate the development of microprocessor. Besides these, the heterogeneous computing becomes new challenge and requirement for microprocessor. (Similar to what mentioned in IV "The One-billion-transistor-chip future") The second is bottlenecks. In my opinion this agent is related to the three parts of process, **for different part of process, the bottleneck is different.**
    - In the next parts, the author reviewed the development of microprocessors since 1970s and then described the future microprocessor.
    - **Personal comment and thinking**

  - *Memory Performance Attacks: Denial of Memory Service in Multi-Core Systems*
    - Background and motivations
      - Processors has evolved from single-core to multi-core system. In current memory system, an application may be a *memory performance hog (MPH)* that could maliciously destroy the memory related performance of another application running on the same chip. More specifically, a memory-intensive application may with particular memory access pattern may occupy shared resources in the memory system and prevent other threads from using those resources efficiently. The potential discomforting of MPHs include the follows:
        - Destroy memory related performance of other programs
          - fool computer users into believing that some other applications are inherently slow
          - unfair billing procedures on grid-like computing systems where users are charged based on CPU hours
        - Cannot be prevented in software, since operating system and compiler has no direct control over the way memory requests are scheduled in the DRAM memory system.
        - A regular application can unintentionally behave like an MPH and damage the memory-related performance of co-scheduled applications
    - The main contribution -- a new memory system design -- a "fair" hardware algorithm --- a new memory scheduling algorithm