```
valid=1, fpga_axi_wready=1
             4781305=> soc_is_cfg_write : wbs_adr=30003000, wbs_sel=0001, wbs_wdata=00000003
             4781305=> soc txen_ctl=1
             4781305=> fpga txen_ctl=1
Enable interrupt, set aa_regs offset 0, bit 0 = 1
             4782025=> soc_aa_cfg_write : wbs_adr=30002100, wbs_sel=1111, wbs_wdata=00000001
             4782625=> soc_aa_cfg_read : wbs_adr=30002100, wbs_sel=1111
             4782625=> soc wishbone read data result : send soc_cfg_read_event
             4782625=> soc_aa_cfg_read : got soc_cfg_read_event
             4782625=> test007_aa_internal_soc_mb_interrupt_en [PASS] cfg_read_data_expect_value=00000001, cfg_read_data_captured=00000001
Read interrupt status, aa_regs offset 4, bit 0 should be 0 by default
             4783225=> soc_aa_cfg_read : wbs_adr=30002104, wbs_sel=1111
             4783225=> soc wishbone read data result : send soc_cfg_read_event
             4783225=> soc_aa_cfg_read : got soc_cfg_read_event
             4783225=> test007_aa_internal_soc_mb_interrupt_en [PASS] cfg_read_data_expect_value[0]=0, cfg_read_data_captured[0]=0
             4783425=> test007_fpga_mail_box_write done
Read mb_regs offset 0
             4784305=> soc_aa_cfg_read : wbs_adr=30002000, wbs_sel=1111
             4784305=> soc wishbone read data result : send soc_cfg_read_event
             4784305=> soc_aa_cfg_read : got soc_cfg_read_event
             4784305=> Result: mb_regs offset 0 [PASS] cfg_read_data_expect_value=11111111, cfg_read_data_captured=11111111
Check interrupt status, read aa_regs offset 4, bit 0
             4784985=> soc_aa_cfg_read : wbs_adr=30002104, wbs_sel=1111
             4784985=> soc wishbone read data result : send soc_cfg_read_event
             4784985=> soc_aa_cfg_read : got soc_cfg_read_event
             4784985=> Read soc_mb_interrupt_status [PASS] cfg_read_data_expect_value[0]=1, cfg_read_data_captured[0]=1
Clear interrupt status, write aa_regs offset 4, bit 0 = 1
             4785305=> soc_aa_cfg_write : wbs_adr=30002104, wbs_sel=1111, wbs_wdata=00000001
             4785905=> soc_aa_cfg_read : wbs_adr=30002104, wbs_sel=1111
             4785905=> soc wishbone read data result : send soc_cfg_read_event
             4785905=> soc_aa_cfg_read : got soc_cfg_read_event
             4785905=>Read soc_mb_interrupt_status [PASS] cfg_read_data_expect_value[0]=0, cfg_read_data_captured[0]=0
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             4786405=> Final result [PASS], check_cnt = 115301, error_cnt = 0000
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$finish called at time : 4786405 ns : File "/home/ubuntu/SoC_Design/caravel-soc_fpga-lab/fsic-sim/fsic_fpga/rtl/user/testbench/tb_fsic.v" Line 444
run: Time (s): cpu = 00:04:43 ; elapsed = 00:05:14 . Memory (MB): peak = 2851.340 ; gain = 0.000 ; free physical = 145 ; free virtual = 8881
## quit
INFO: xsimkernel Simulation Memory Usage: 126992 KB (Peak: 170836 KB), Simulation CPU Usage: 143850 ms
ubuntu@ubuntu2004:~/SoC_Design/caravel-soc_fpga-lab/fsic-sim/fsic_fpga/rtl/user/testbench/tc$
```