DSPIC Final Project

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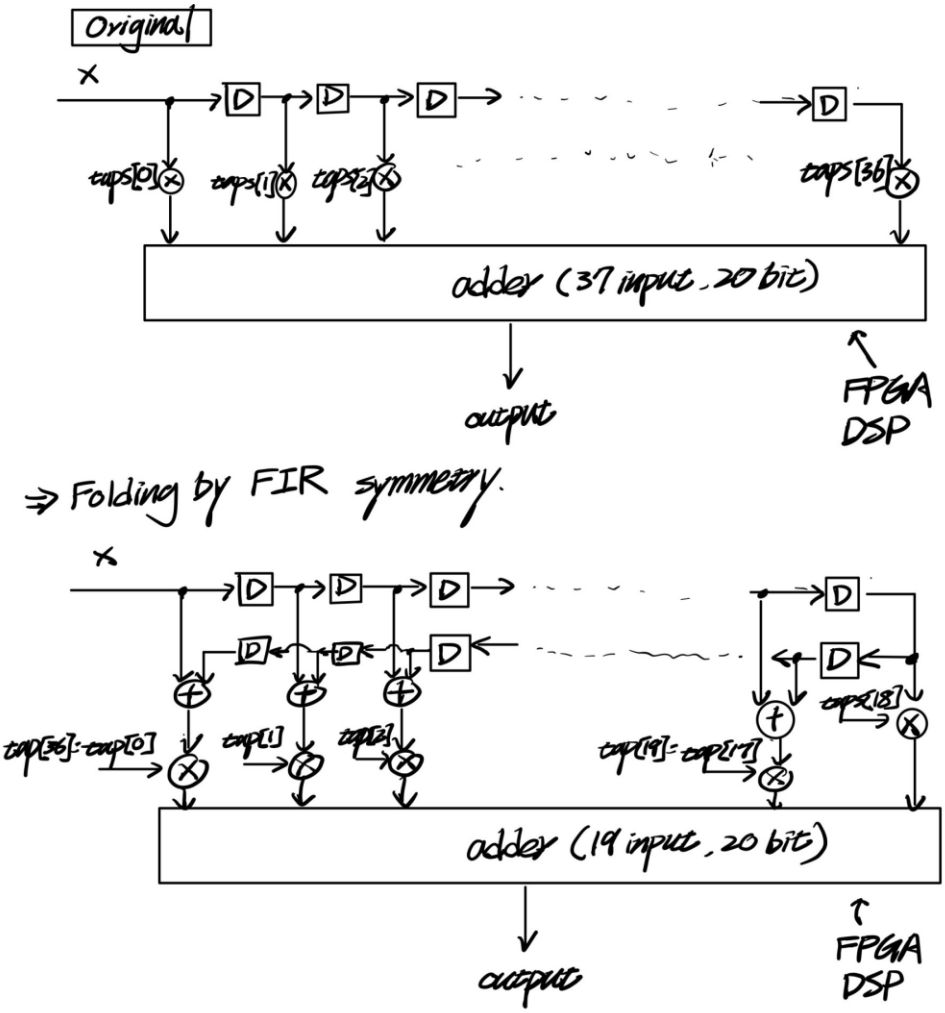
In final project, I design an optimized FIR based on HW4. I follow the same procedure in HW4. Using C to simulate the floating point FIR, then performing fixed point FIR to compare the performance. Choosing the word length and MAC word length to design the hardware. Further, I design a booth multiplier for less resource usage, but decrease the throughput. Finally, synthesis the hardware design to check the performance and resource usage.

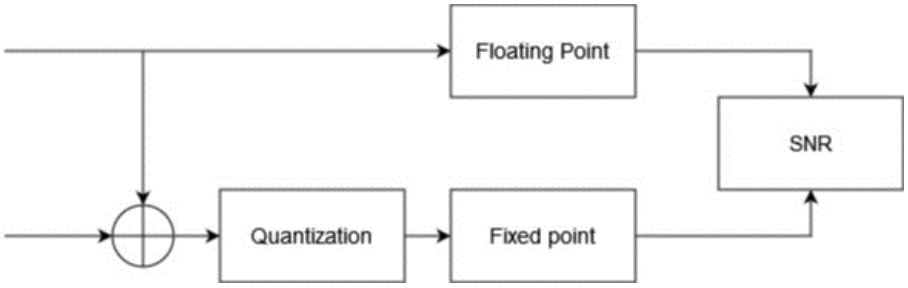
1. Optimized FIR design structure



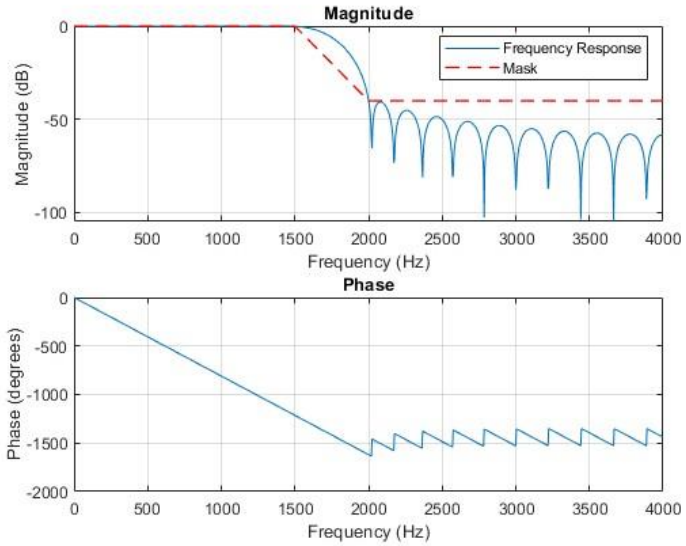
Due to the FIR symmetry, the tap[0] and tap[36] are equal, tap[1] and tap[35] are equal,… and so on. We observe symmetry to reduce the usage of multiplier. Originally, we need 37 multipliers for hardware design. After folding, we only need 19 multipliers, but we need to fold the input to sum up the x[0] and x[36] first. Besides, the final adder will be 19 input, 20 bit rather than 37 input 20 bit, reducing the cost of the adder (In FPGA, is DSP).

2. C simulation (code explanation and choosing word length)

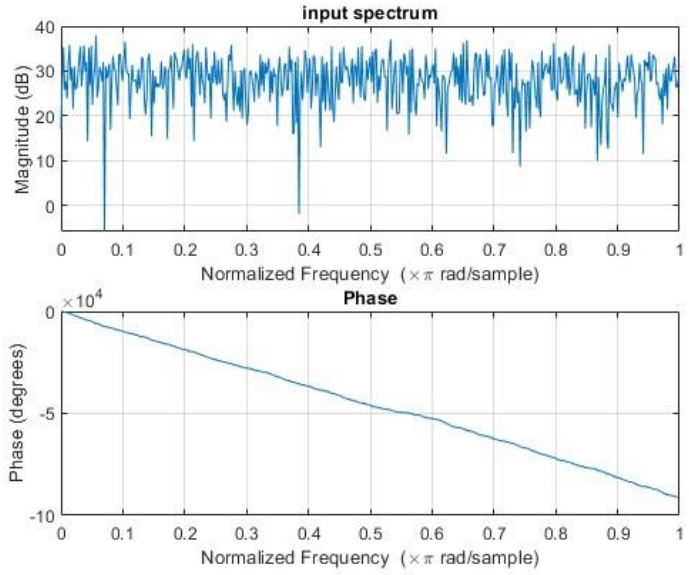
In original system, we add the channel noise in quantization. Therefore, each input after quantization will be affected by certain error. In original design, we direct use these quantization signal to multiply with coefficient to get output. After the SNR calculation, we decide the word length = 14, and the MAC word length = 20.



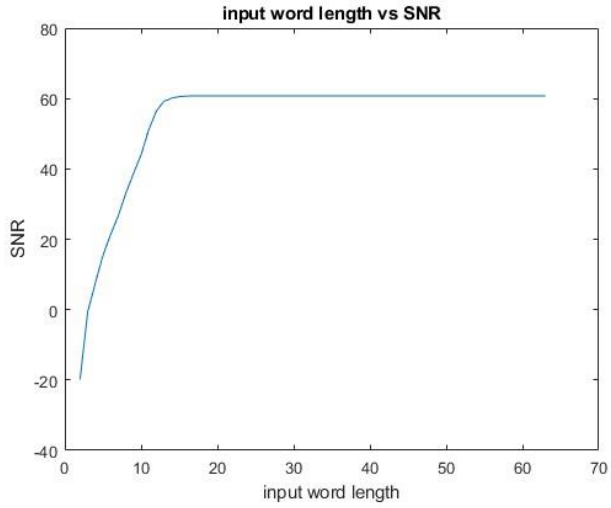
Frequency response of FIR (To decide the coefficient)



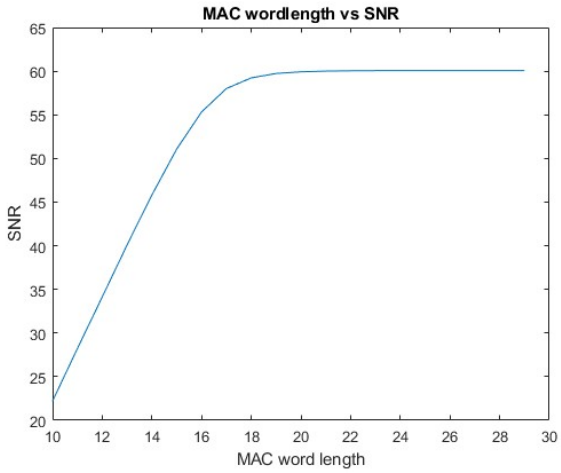
Input signal



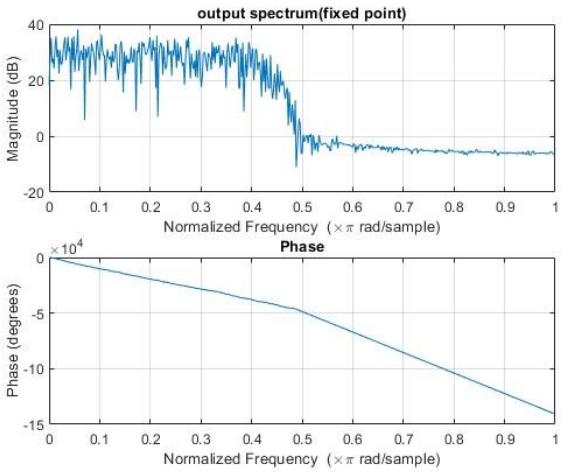
Input word length vs SNR



MAC word length vs SNR



Output signal (fixed)



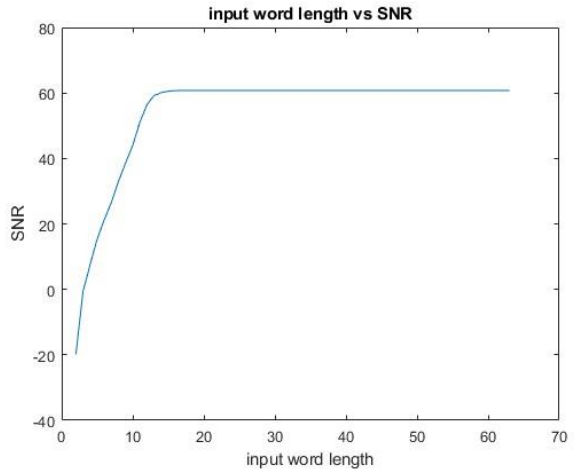
However, If we change the Design to folded FIR, the quantization error would be sum up when we are doing x[0]+ x[36]. This may cause the Final SNR Change, so we need to perform the same procedure.

Simulation C code

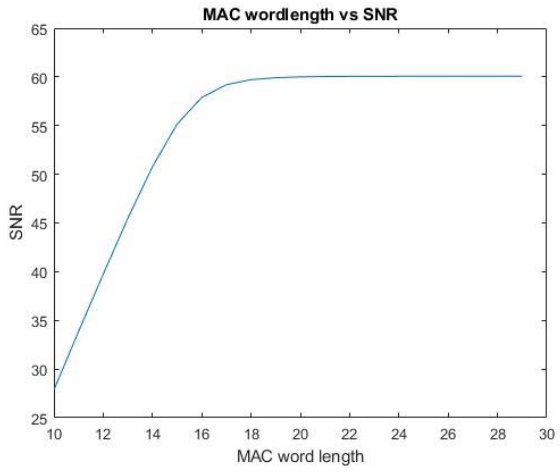
```
for(auto input : inputsignal){
    for(int i=N-1;i>0;i--){
        inputbuffer[i]=inputbuffer[i-1];
    }

    inputbuffer[0] = input;

    for(int i=0;i<(M-1);i++){
        buffer_tmp[i] = inputbuffer[i]+inputbuffer[(N-1)-i];
    }
    buffer_tmp[M-1] = inputbuffer[M-1];
```

I create the temp buffer for storing the adder result for multiplier input. Once accept the new input data, we need to update each temp buffer. After counting out the output signal, we compare the SNR.

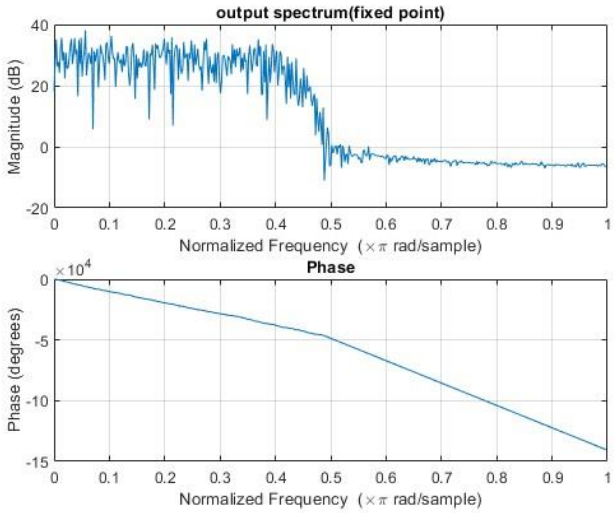
Input word length vs SNR



MAC word length vs SNR



Output signal (fixed)



From our result, we still use the same word length(14) and MAC word length(20) for our design.

3. Hardware design of FIR and booth multiplier

To operate the hardware, we need to notice the bit of the temp buffer. To avoid overflow, we need to use a 15 bit buffer to store the result of x[0] + x[36] in Verilog. This is how I design the temp buffer.

```
reg signed [WL:0] temp_buffer [(fold_length-1):0];
//-----------------------------------------------

//initialize the temp_buffer and the behavior of adder
//-----------------------------------------------
integer ii;
always@(posedge clk or negedge rst_n) begin
    if(~rst_n) begin
        for(ii=0;ii<(fold_length-1);ii=ii+1) begin
            temp_buffer[ii] <= 15'd0;
        end
    end else begin
        for(ii=0;ii<(fold_length-1);ii=ii+1) begin
            temp_buffer[ii] <= inputbuffer[ii] + inputbuffer[36-ii];
        end
            temp_buffer[18] <= inputbuffer[18];
    end
end
```

Besides the temp buffer, I design a 16*16 multiplier rather than directly using the DSP. I choose booth algorithm to design the multiplier. To design the multiplier, we should use the start and done signal to control the multiplier. I also use the **w_valid** signal as the valid signal for testbench knows when the data is valid to be read.

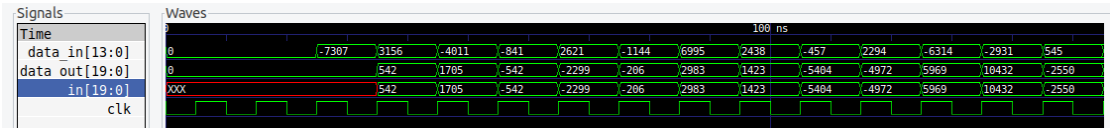
```
input  wire                     axis_clk, //
input  wire                     axis_rst_n, ,
input  wire [din0_WIDTH - 1 : 0] din0,
input  wire [din1_WIDTH - 1 : 0] din1,
output wire [dout_WIDTH - 1 : 0] dout,

input  wire                     start,
output wire                     done
```

We design two folded FIR, one is using DSP, and the other is using booth multiplier. We will compare the performance and resource usage in next part. Both resource and critical path are reduced, but the throughput is also reduced. Here is the waveform and simulation log of our 2 design.

Simulation log (DSP):

```
[Correct] [Pattern       1015] Golden answer:   258881, Your answer:   258881
[Correct] [Pattern       1016] Golden answer:   178140, Your answer:   178140
[Correct] [Pattern       1017] Golden answer:   196836, Your answer:   196836
[Correct] [Pattern       1018] Golden answer:   292065, Your answer:   292065
[Correct] [Pattern       1019] Golden answer:   341854, Your answer:   341854
[Correct] [Pattern       1020] Golden answer:   231594, Your answer:   231594
[Correct] [Pattern       1021] Golden answer:   -25636, Your answer:   -25636
[Correct] [Pattern       1022] Golden answer:  -275277, Your answer:  -275277
[Correct] [Pattern       1023] Golden answer:  -360223, Your answer:  -360223
$finish called at time : 10335 ns : File "/home/ubuntu/DSPIC_Final/project_1/tb/
fir_tb.v" Line 94
```

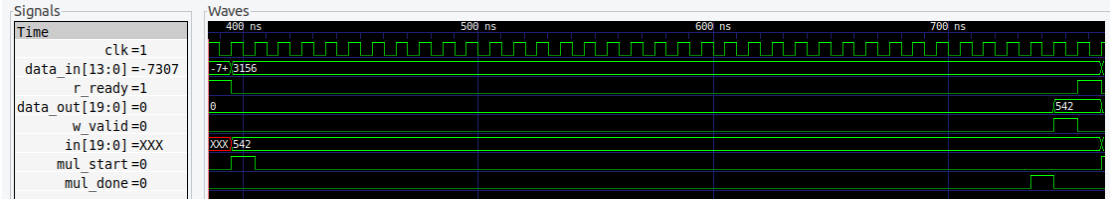
Waveform (DSP):



Simulation log (Booth):

```
[Correct] [Pattern       1017] Golden answer:   196836, Your answer:   196836
[Correct] [Pattern       1018] Golden answer:   292065, Your answer:   292065
[Correct] [Pattern       1019] Golden answer:   341854, Your answer:   341854
[Correct] [Pattern       1020] Golden answer:   231594, Your answer:   231594
[Correct] [Pattern       1021] Golden answer:   -25636, Your answer:   -25636
[Correct] [Pattern       1022] Golden answer:  -275277, Your answer:  -275277
[Correct] [Pattern       1023] Golden answer:  -360223, Your answer:  -360223
$finish called at time : 379295 ns : File "/home/ubuntu/DSPIC_Final/project_2/tb
/fir_tb.v" Line 95
```

Waveform (Booth):



First, the r_ready signal is set to 1, means the system is ready to accept the input data from host. Once the input data accept, the mul_start set to 1 to start the multiplier. When the multiplication result is count out. The mul_done signal

will set to 1, mean the result is available. Then, the w_valid is set to 1, mean the output signal is ready to write to host. After data is read from host, the system can read next input signal from host.

4. Hardware design resource usage (Compare to the basic design):

I set all hardware system clock = 10 ns and watch out the difference.

1. Original design (basic)

Resource usage(basic):

Name 1	Slice LUTs (53200)	Slice Registers (106400)	DSPs (220)	Bonded IOB (125)	BUFGCTRL (32)
N fir	313	518	35	36	1

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	313	0	0	53200	0.59
LUT as Logic	313	0	0	53200	0.59
LUT as Memory	0	0	0	17400	0.00
Slice Registers	518	0	0	106400	0.49
Register as Flip Flop	518	0	0	106400	0.49
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	35	0	0	220	15.91
DSP48E1 only	35				

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	36	0	0	125	28.80
Bonded IPADs	0	0	0	2	0.00
Bonded IOPADs	0	0	0	130	0.00
PHY_CONTROL	0	0	0	4	0.00
PHASER_REF	0	0	0	4	0.00
OUT_FIFO	0	0	0	16	0.00
IN_FIFO	0	0	0	16	0.00
IDELAYCTRL	0	0	0	4	0.00
IBUFDS	0	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	200	0.00
ILOGIC	0	0	0	125	0.00
OLOGIC	0	0	0	125	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	16	0.00
MMCME2_ADV	0	0	0	4	0.00
PLLE2_ADV	0	0	0	4	0.00
BUFMRCE	0	0	0	8	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	16	0.00

Clock(basic):

Since the MAC is synthesis as DSP in the FPGA, and the speed of DSP on the FPGA is very high. Therefore, the maximum delay path isn't in the calculation, but the routing and shift register. We can find out this situation in the timing reports.

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.731 ns	Worst Hold Slack (WHS):	0.152 ns	Worst Pulse Width Slack (WPWS):	
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TF	
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	
Total Number of Endpoints:	504	Total Number of Endpoints:	504	Total Number of Endpoints:	

All user specified timing constraints are met.

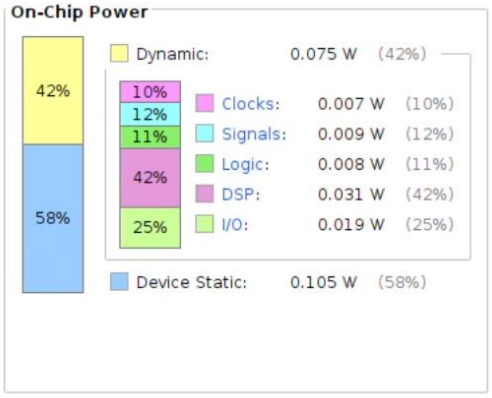
```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             8.731ns  (required time - arrival time)
  Source:                 inputbuffer_reg[9][13]/C
                            (rising edge-triggered cell FDCE clocked by clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            inputbuffer_reg[10][13]/D
                            (rising edge-triggered cell FDCE clocked by clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (clk rise@10.000ns - clk rise@0.000ns)
  Data Path Delay:        0.869ns  (logic 0.478ns (55.006%)  route 0.391ns (44.994%))
  Logic Levels:           0
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 12.128 - 10.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

Power(basic):

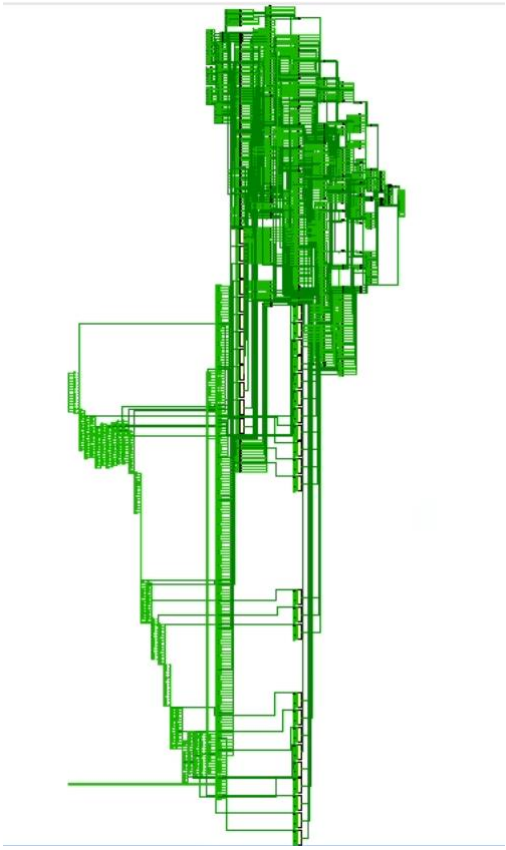
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.181 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (4.9 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Synthesis Schematic(basic):



2. **Optimized design (DSP)**

   Resource usage (DSP):

Name 1	Slice LUTs (53200)	Slice Registers (106400)	DSPs (220)	Bonded IOB (125)	BUFGCTRL (32)
N fir	197	518	18	36	1

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	197	0	0	53200	0.37
LUT as Logic	197	0	0	53200	0.37
LUT as Memory	0	0	0	17400	0.00
Slice Registers	518	0	0	106400	0.49
Register as Flip Flop	518	0	0	106400	0.49
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	18	0	0	220	8.18
DSP48E1 only	18				

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	36	0	0	125	28.80
Bonded IPADs	0	0	0	2	0.00
Bonded IOPADs	0	0	0	130	0.00
PHY_CONTROL	0	0	0	4	0.00
PHASER_REF	0	0	0	4	0.00
OUT_FIFO	0	0	0	16	0.00
IN_FIFO	0	0	0	16	0.00
IDELAYCTRL	0	0	0	4	0.00
IBUFDS	0	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	200	0.00
ILOGIC	0	0	0	125	0.00
OLOGIC	0	0	0	125	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	16	0.00
MMCME2_ADV	0	0	0	4	0.00
PLLE2_ADV	0	0	0	4	0.00
BUFMRCE	0	0	0	8	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	16	0.00

Clock (DSP):

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.731 ns	Worst Hold Slack (WHS):	0.152 ns	Worst Pulse Width Slack (WPWS):	
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TP	
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	
Total Number of Endpoints:	504	Total Number of Endpoints:	504	Total Number of Endpoints:	

All user specified timing constraints are met.

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             8.731ns  (required time - arrival time)
  Source:                 inputbuffer_reg[18][13]/C
                            (rising edge-triggered cell FDCE clocked by clk  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            inputbuffer_reg[19][13]/D
                            (rising edge-triggered cell FDCE clocked by clk  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (clk rise@10.000ns - clk rise@0.000ns)
  Data Path Delay:        0.869ns  (logic 0.478ns (55.006%)  route 0.391ns (44.994%))
  Logic Levels:           0
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 12.128 - 10.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

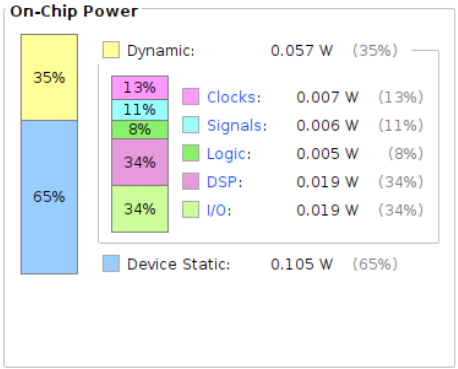
Power (DSP):

Summary

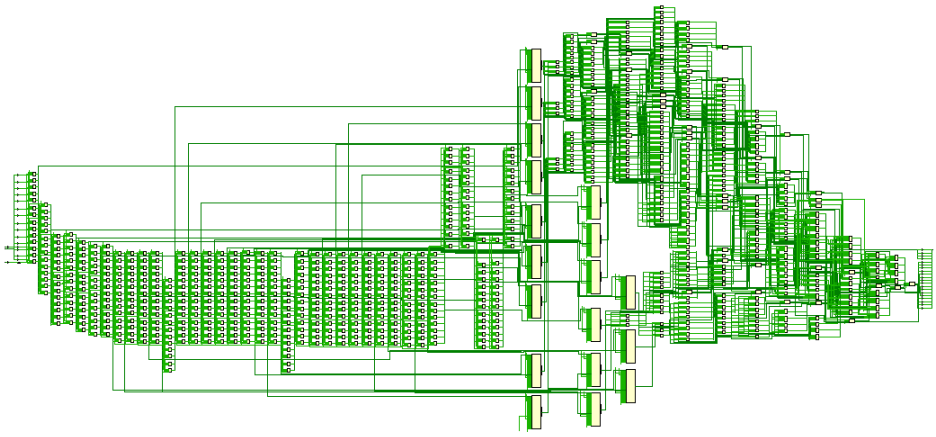
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.162 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.9°C**
Thermal Margin:	58.1°C (4.9 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Synthesis Schematic (DSP):



Compared to basic design, in the same clock speed situation, we can use less resource and less power to achieve the same function without changing the throughput. It's reasonable to perform this optimization.

3. **Optimized design (Booth)**

   I set all hardware system clock = 10 ns and watch out the difference.

   Resource usage (Booth):

Name	Slice LUTs (53200)	Slice Registers (106400)	Bonded IOB (125)	BUFGCTRL (32)
> N fir	1594	1738	38	1

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	1594	0	0	53200	3.00
LUT as Logic	1594	0	0	53200	3.00
LUT as Memory	0	0	0	17400	0.00
Slice Registers	1738	0	0	106400	1.63
Register as Flip Flop	1738	0	0	106400	1.63
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	220	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	38	0	0	125	30.40
Bonded IPADs	0	0	0	2	0.00
Bonded IOPADs	0	0	0	130	0.00
PHY_CONTROL	0	0	0	4	0.00
PHASER_REF	0	0	0	4	0.00
OUT_FIFO	0	0	0	16	0.00
IN_FIFO	0	0	0	16	0.00
IDELAYCTRL	0	0	0	4	0.00
IBUFDS	0	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	200	0.00
ILOGIC	0	0	0	125	0.00
OLOGIC	0	0	0	125	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	16	0.00
MMCME2_ADV	0	0	0	4	0.00
PLLE2_ADV	0	0	0	4	0.00
BUFMRCE	0	0	0	8	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	16	0.00

Clock (Booth):

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.599 ns	Worst Hold Slack (WHS):	0.137 ns	Worst Pulse Width Slack (WPWS):	
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TF	
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	
Total Number of Endpoints:	3328	Total Number of Endpoints:	3328	Total Number of Endpoints:	

All user specified timing constraints are met.

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.599ns  (required time - arrival time)
  Source:                 genblk1[5].booth_U/dout_reg_reg[11]/C
                            (rising edge-triggered cell FDCE clocked by clk  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            add_reg[19]/D
                            (rising edge-triggered cell FDCE clocked by clk  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (clk rise@10.000ns - clk rise@0.000ns)
  Data Path Delay:        9.265ns  (logic 4.987ns (53.826%)  route 4.278ns (46.174%))
  Logic Levels:           13  (CARRY4=6 LUT2=1 LUT3=3 LUT4=3)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 12.128 - 10.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

Power (Booth):

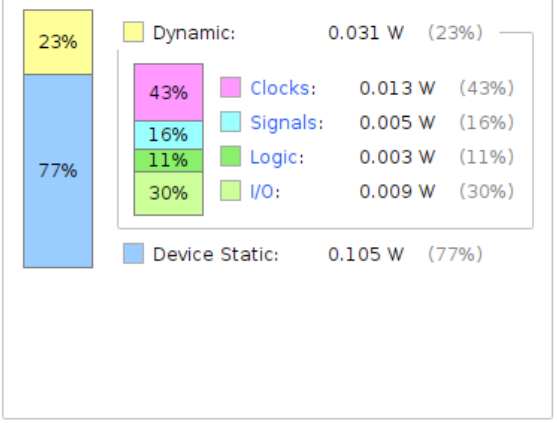
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

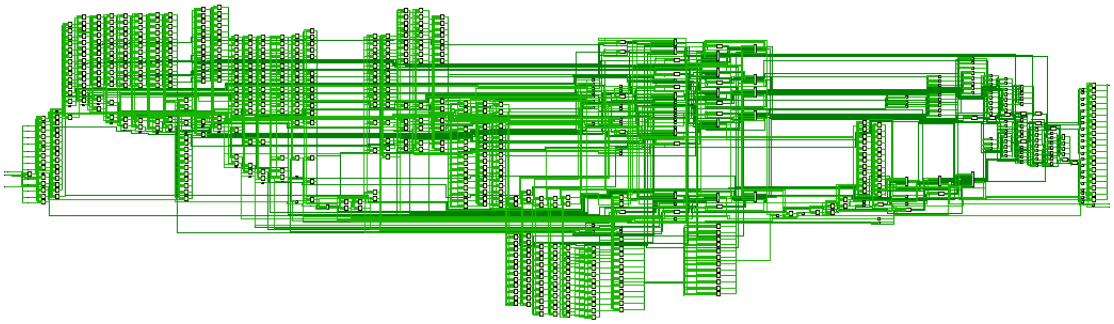
Total On-Chip Power:	**0.136 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.6°C**
Thermal Margin:	58.4°C (4.9 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power



Synthesis Schematic (Booth):



Compared to basic design and DSP design, in the same clock speed situation, we avoid using the DSP for our fir design, this cause more power reduce. However, the throughput is much reduced, which is about 32 times than basic design and DSP design. After using the booth multiplier, we will meet the situation of throughput and resource trade off. We should base on the application to decide whether to use this design.

Comparison table:

	LUT	Register	DSP	Bonded IO	BUFGCTRL	Power(W)	Throughput
Basic	313	518	35	36	1	0.181	1
DSP	197	518	18	36	1	0.162	1
Booth	1594	1738	0	38	1	0.136	1/32