# DPSIC Final Project Proposal

## 1. Purpose：

Base on the performance of homework 4, we have multiple method to optimize our result. Therefore, we can find the method to optimize homework 4 to design new FIR in final project, while having different performance with homework 4. (the MAC word length and input word length will use the same spec in my homework 4, which are 20 bits and 12 bits respectively.)

## 2. Optimize Method：

a. In homework 4, I design the FIR with tap depth = 37. However, I directly use 37 multipliers for my hardware design. I think we can fold our Hardware to save the number of multipliers, since the multiplier is costly part of hardware.
b. Observing the FIR taps, we can find out the symmetry of coefficients, I think we can use this property to reduce the number of multipliers.
c. I think both adder and multiplier optimization would be useful. However, since we want to perform many different multipliers saving method. This will cause the reduction of throughput. If further trading off the throughput and resource usage, the throughput would be very low. Therefore, I think we can increase the resource usage to make the calculation time of adder and multiplier be faster.