Digital Signal Processing Integrated Circuit Design

Homework #4 (Lab 1)

(Due date: 2023/12/7 PM 23:00)

1. Please design an 7x5 **Baugh-Wooley** multiplier based on Wallace-tree carry-save-addition (CSA) architecture.
   (a) Derive the long multiplication chart of an 7x5 **Baugh-Wooley** multiplier (similar to Page 29 and 34 of Chapter 9).
   (b) Plot architecture of the 8x6 Wallace-Tree multiplier (similar to Page 35 of Chapter 9) based on full adder and half adder.
   (c) Simulate the architecture by coding the 7x5 **Baugh-Wooley** multiplier in RTL Verilog HDL language. (Please use more than 20 sets of inputs to verify your design. Four combinations of negative and positive signs must all be included.)

2. Please design a low-pass digital FIR filter with the following target specifications

$$20 \cdot \log(\delta_s) < -40\text{dB stopband attenuation } (-40\text{dB})$$
$$f_p = 1.5\text{kHz passband edge frequency}$$
$$F_s = 8\text{kHz} \quad \text{sampling frequency}$$
$$\Delta f = 0.5\text{kHz transition width of the filter}$$

   (a) Design a low-pass digital FIR filter with the smallest number of floating-point coefficients using C/C++ program. You can use Matlab tool functions to calculate the filter coefficients.
      (i) List the floating-point coefficients of the digital FIR filter.
      (ii) Plot the frequency response of the digital FIR filter and the frequency mask of the target filter specifications (using matlab).

   (b) Fixed-point simulation: determine the word-length of input signals and filter coefficients of this low-pass digital FIR filter using C/C++ program.
      (i) Randomly generate test patterns of floating-point signed real-value signals with average power of 1. Please use enough number of test patterns to perform the target FIR processing. Please analyze the output signal spectral and verify that the output signals are filtered by the target filter specifications. You can plot the spectrum of the input signal spectrum/output signal spectrum along with the target

filter specifications of frequency response in a figure.

(ii) Perform the fixed-point simulations based on the output SNR metric. Plot the figure of output SNR versus input wordlength and the figure of output SNR versus word-length of the multiplier-and-accumulator (MAC) to determine the word-length of the digital FIR filter.

$$\mathrm{SNR} = 10 \log \frac{P_{\mathrm{float}}}{P_{\mathrm{float-fix}}}$$

$P_{\mathrm{float-fix}}$ is power of different between floating-point and fix-point result

P_{float} is power of floating-point result

(c) Design this low-pass digital FIR filter by using Verilog HDL according to word-length determined in the fixed-point simulations. You can use the Xilinx Vivado or ISE software to design and synthesize the HDL code with arbitrary FPGA device. (You can also use an available and legally licensed standard cell library to simulate the corresponding results to FPGA.)

(i) Simulate your Verilog HDL code with the same input pattern in the fixed-point simulation. Compare the output results of the fixed-point program and Verilog HDL simulations. (output waveforms)

(ii) List the circuit speed and FPGA resource numbers of your digital Filter design. Please provide synthesis and implementation reports of your design from the tools.