SOC Design

LAB 1 – 111061545 陳揚哲

● Brief introduction about the overall system

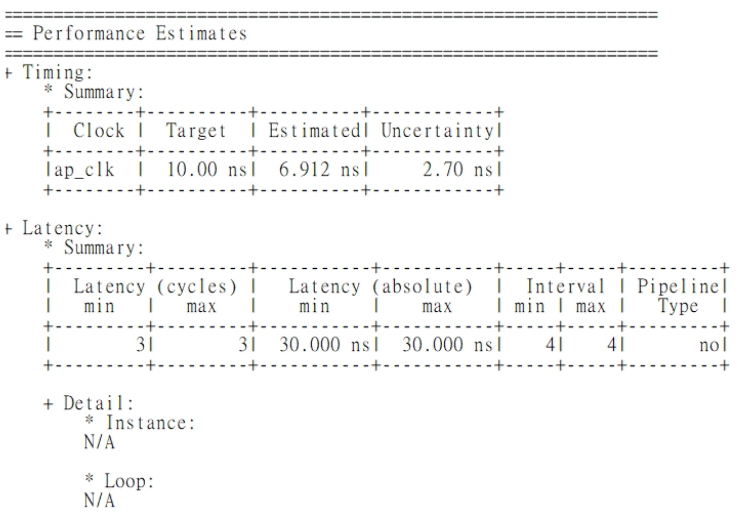
In lab 1, we get the pre-code of the multiplication. Before implementation, we add the C++ source code and header file to Vitis and the test file to testbench. In first step, we should set the top function for export RTL (IP). In lab 1, we don't need to set up the directives since using #pargma. Then, we can start simulation and synthesis. After synthesis, we can start Cosimulation. In this step, we can see the waveform. Finally, we can use vivado to connect the ZYNQ and our multiplication IP. We have to generate the wrapper and bitstream for PYNQ access the design.

● What is observed & learned

In this lab, we understand the basic HLS flow, use top function for export RTL. Generate the wrapper for PYNQ access the design. It's necessary to wrapped in Python package for Jupyter operate based on overlay.

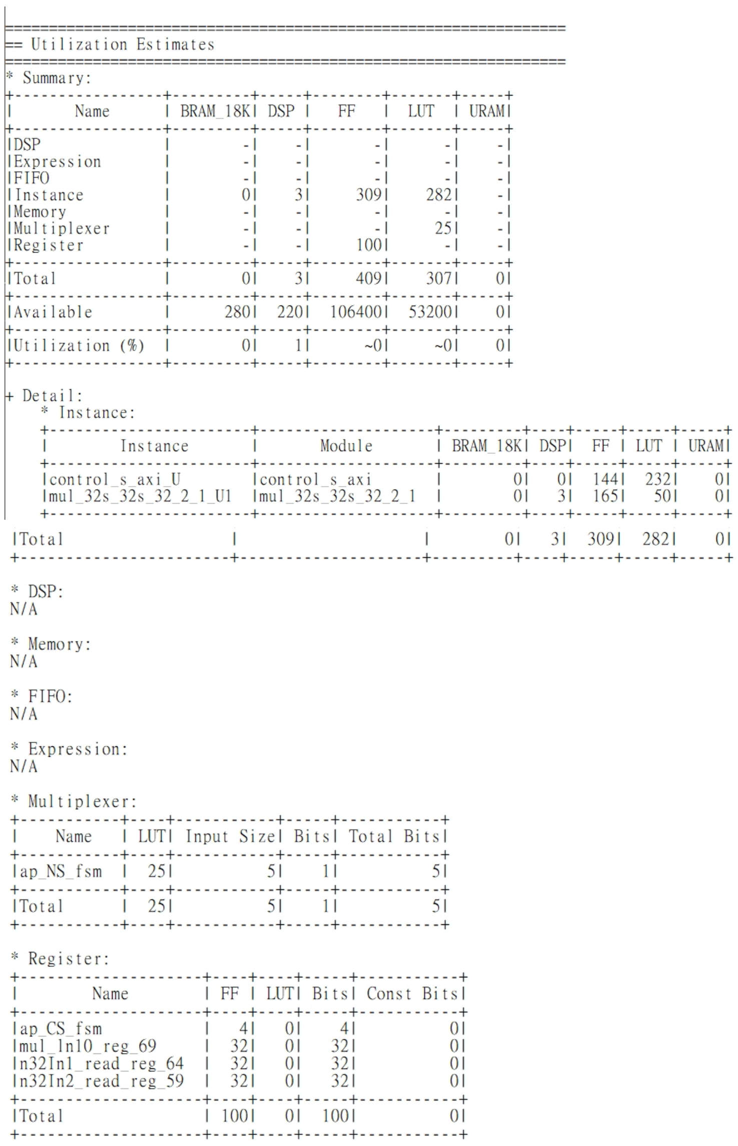
● Screen Dump

Performance：



```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    | Clock  |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  | 10.00 ns | 6.912 ns |     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+-----------+-----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute)   |  Interval | Pipeline|
    |   min   |   max   |    min    |    max    | min | max |   Type  |
    +---------+---------+-----------+-----------+-----+-----+---------+
    |        3|        3| 30.000 ns | 30.000 ns |    4|    4|       no|
    +---------+---------+-----------+-----------+-----+-----+---------+

    + Detail:
        * Instance:
        N/A

        * Loop:
        N/A
```

Utilization：

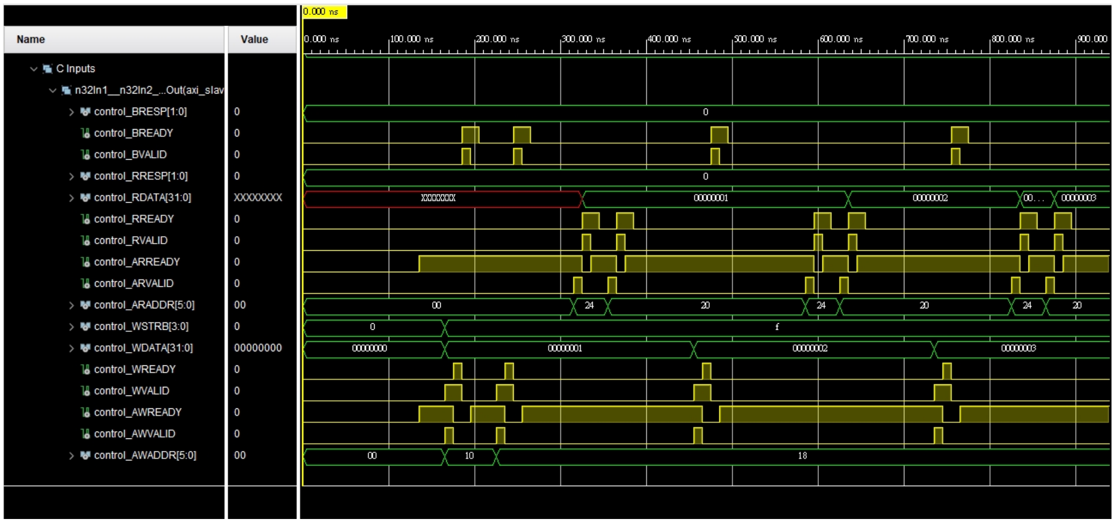


```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       -|      -|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|    3|     309|    282|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|     25|    -|
|Register         |        -|    -|     100|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|    3|     409|    307|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|    1|      ~0|     ~0|    0|
+-----------------+---------+-----+--------+-------+-----+

+ Detail:
    * Instance:
    +-----------------------+--------------------+---------+----+-----+-----+-----+
    |        Instance       |       Module       | BRAM_18K| DSP|  FF | LUT | URAM|
    +-----------------------+--------------------+---------+----+-----+-----+-----+
    |control_s_axi_U        |control_s_axi       |        0|   0|  144|  232|    0|
    |mul_32s_32s_32_2_1_U1  |mul_32s_32s_32_2_1  |        0|   3|  165|   50|    0|
    +-----------------------+--------------------+---------+----+-----+-----+-----+
    |Total                  |                    |        0|   3|  309|  282|    0|
    +-----------------------+--------------------+---------+----+-----+-----+-----+

    * DSP:
    N/A

    * Memory:
    N/A

    * FIFO:
    N/A

    * Expression:
    N/A

    * Multiplexer:
    +-----------+----+-----------+-----+-----------+
    |    Name   | LUT| Input Size| Bits| Total Bits|
    +-----------+----+-----------+-----+-----------+
    |ap_NS_fsm  |  25|          5|    1|          5|
    +-----------+----+-----------+-----+-----------+
    |Total      |  25|          5|    1|          5|
    +-----------+----+-----------+-----+-----------+

    * Register:
    +---------------------+----+----+-----+-----------+
    |         Name        | FF | LUT| Bits| Const Bits|
    +---------------------+----+----+-----+-----------+
    |ap_CS_fsm            |   4|   0|    4|          0|
    |mul_ln10_reg_69      |  32|   0|   32|          0|
    |n32In1_read_reg_64   |  32|   0|   32|          0|
    |n32In2_read_reg_59   |  32|   0|   32|          0|
    +---------------------+----+----+-----+-----------+
    |Total                | 100|   0|  100|          0|
    +---------------------+----+----+-----+-----------+
```

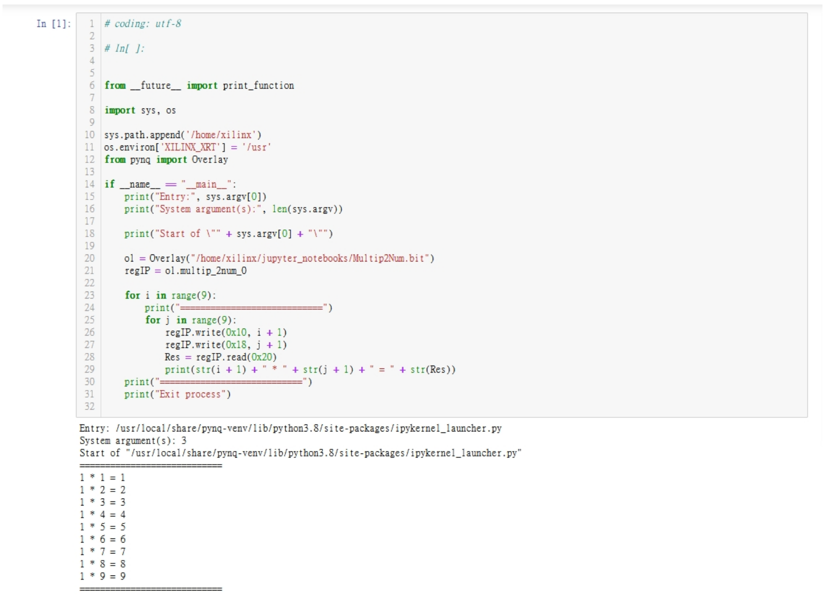
Interface：

```
================================================================
== Interface
================================================================
* Summary:
+-----------------------+-----+-----+------------+--------------+--------------+
|       RTL Ports       | Dir | Bits|  Protocol  | Source Object|    C Type    |
+-----------------------+-----+-----+------------+--------------+--------------+
|s_axi_control_AWVALID  |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_AWREADY  |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_AWADDR   |   in|    6|       s_axi|       control|       pointer|
|s_axi_control_WVALID   |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_WREADY   |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_WDATA    |   in|   32|       s_axi|       control|       pointer|
|s_axi_control_WSTRB    |   in|    4|       s_axi|       control|       pointer|
|s_axi_control_ARVALID  |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_ARREADY  |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_ARADDR   |   in|    6|       s_axi|       control|       pointer|
|s_axi_control_RVALID   |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_RREADY   |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_RDATA    |  out|   32|       s_axi|       control|       pointer|
|s_axi_control_RRESP    |  out|    2|       s_axi|       control|       pointer|
|s_axi_control_BVALID   |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_BREADY   |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_BRESP    |  out|    2|       s_axi|       control|       pointer|
|ap_clk                 |   in|    1|  ap_ctrl_hs|   multip_2num|  return value|
|ap_rst_n               |   in|    1|  ap_ctrl_hs|   multip_2num|  return value|
|ap_start               |   in|    1|  ap_ctrl_hs|   multip_2num|  return value|
|ap_done                |  out|    1|  ap_ctrl_hs|   multip_2num|  return value|
|ap_idle                |  out|    1|  ap_ctrl_hs|   multip_2num|  return value|
|ap_ready               |  out|    1|  ap_ctrl_hs|   multip_2num|  return value|
+-----------------------+-----+-----+------------+--------------+--------------+
```

Cosimulation waveform：

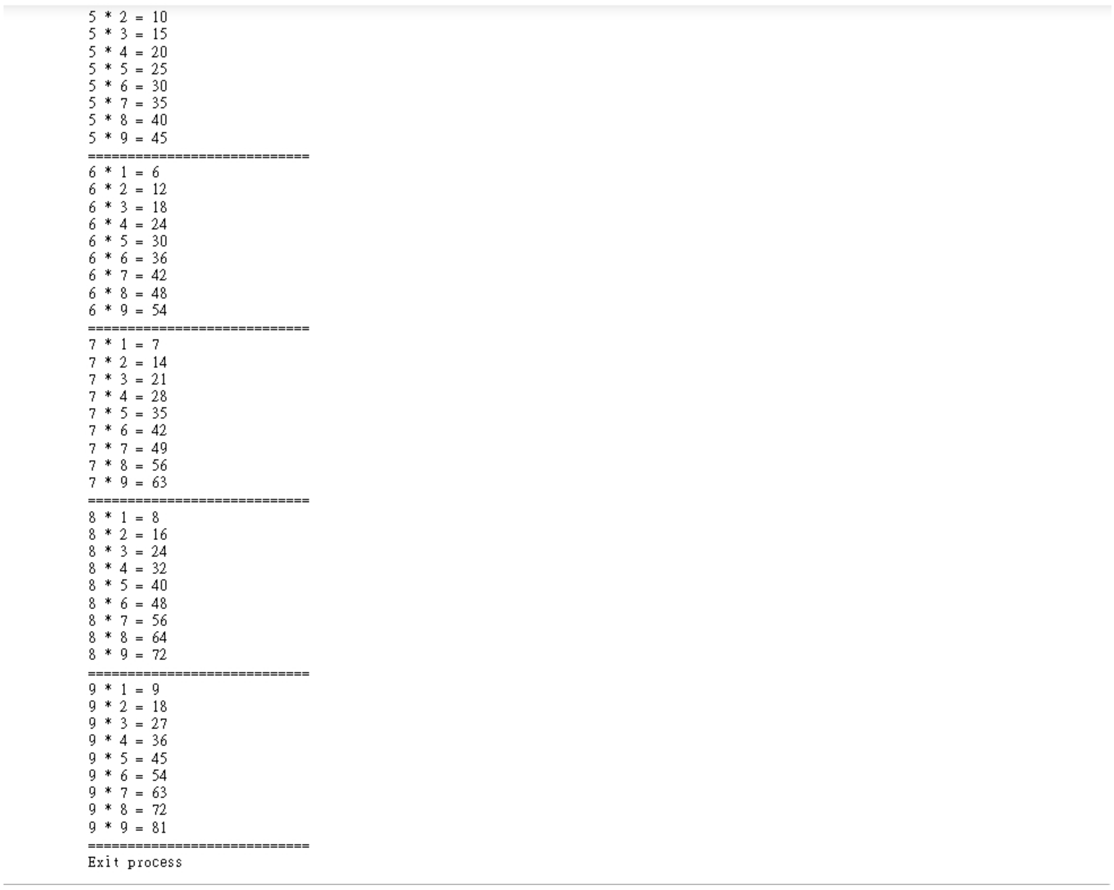


Jupyter Notebook execution results：



```
In [1]:
# coding: utf-8

# In[ ]:


from __future__ import print_function

import sys, os

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("/home/xilinx/jupyter_notebooks/Multip2Num.bit")
    regIP = ol.multip_2num_0

    for i in range(9):
        print("============================")
        for j in range(9):
            regIP.write(0x10, i + 1)
            regIP.write(0x18, j + 1)
            Res = regIP.read(0x20)
            print(str(i + 1) + " * " + str(j + 1) + " = " + str(Res))
    print("============================")
    print("Exit process")

```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
============================
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
============================
```



```
5 * 2 = 10
5 * 3 = 15
5 * 4 = 20
5 * 5 = 25
5 * 6 = 30
5 * 7 = 35
5 * 8 = 40
5 * 9 = 45
============================
6 * 1 = 6
6 * 2 = 12
6 * 3 = 18
6 * 4 = 24
6 * 5 = 30
6 * 6 = 36
6 * 7 = 42
6 * 8 = 48
6 * 9 = 54
============================
7 * 1 = 7
7 * 2 = 14
7 * 3 = 21
7 * 4 = 28
7 * 5 = 35
7 * 6 = 42
7 * 7 = 49
7 * 8 = 56
7 * 9 = 63
============================
8 * 1 = 8
8 * 2 = 16
8 * 3 = 24
8 * 4 = 32
8 * 5 = 40
8 * 6 = 48
8 * 7 = 56
8 * 8 = 64
8 * 9 = 72
============================
9 * 1 = 9
9 * 2 = 18
9 * 3 = 27
9 * 4 = 36
9 * 5 = 45
9 * 6 = 54
9 * 7 = 63
9 * 8 = 72
9 * 9 = 81
============================
Exit process
```