FIR Workbook (lab_3)

SOC Design

Function specification

- Same as course-lab_2(FIRN11stream)
- $y[t] = \Sigma (h[i] * x[t - i])$

Design specification

- Data_Width 32
- Tape_Num 11
- Data_Num TBD – Based on size of data file
- Interface
  - data_in stream （Xn）
  - data_out: stream (Yn)
  - coef[Tape_Num-1:0] axilite
  - len: axilite
  - ap_start: axilite
  - ap_done: axilite
- Using one Multiplier and one Adder
- Shift register implemented with SRAM (Shift_RAM, size = 10 DW) – size = 10 DW
- Tap coefficient implemented with SRAM (Tap_RAM = 11 DW) and initialized by axilite write
- Operation
  - ap_start to initiate FIR engine (ap_start valid for one clock cycle)
  - Stream-in Xn. The rate is depending on the FIR processing speed. Use axi-stream valid/ready for flow control
  - Stream out Yn, the output rate depends on FIR processing speed.

Deliver module header

- The I/O signals are listed in fir.v.
- You are requested to use simplified AXI-lite and AXI-stream protocol.

Configuration Register Address map

0x00 – [0] - ap_start -> set when ap_start signal asserts

-> reset, when start data transfer, i.e. 1st axi-stream data come in

[1] – ap_done -> when FIR process all the dataset, i.e. receive tlast, and last Y is generated

[2] – ap_idle -> indicate FIR is actively processing data

0x10-14 - data-length

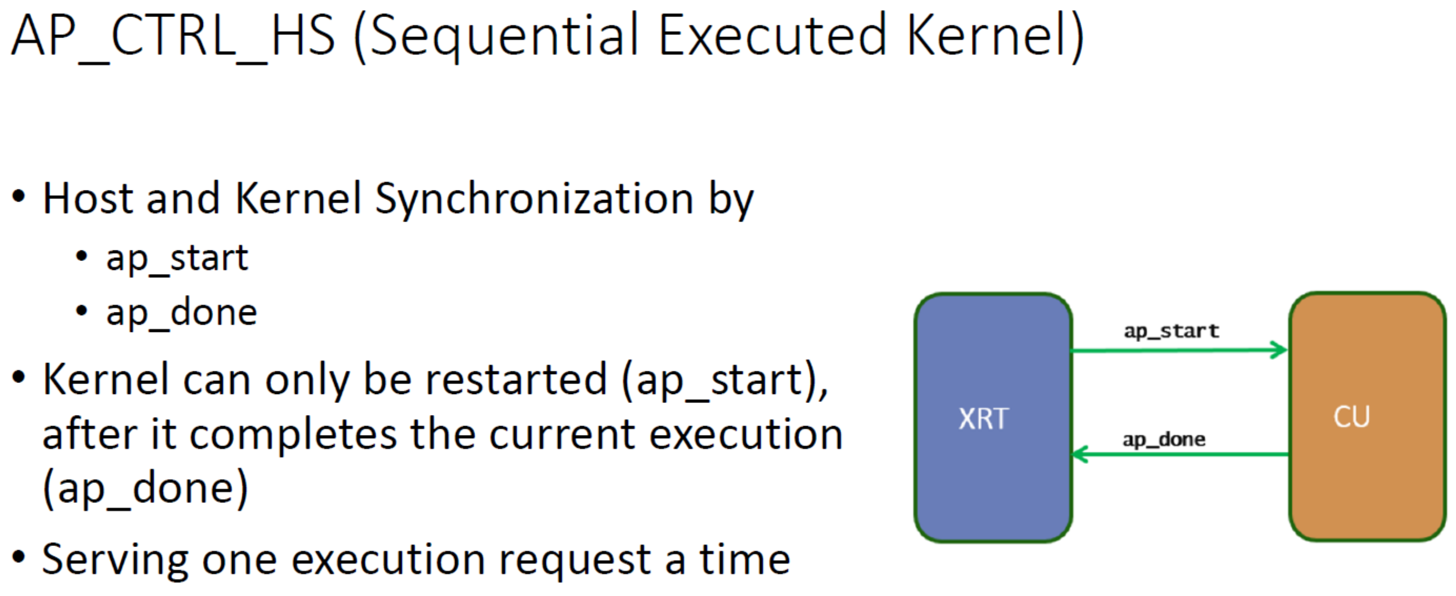
0x20-FF – Tap parameters, (e.g., 0x20-24 Tap0, in sequence …)

FIR module interface

- For your reference:
  - AXI-lite:
    - https://www.realdigital.org/doc/a9fee931f7a172423e1ba73f66ca4081
    - https://docs.xilinx.com/r/en-US/pg202-mipi-dphy/AXI4-Lite-Interface
  - AXI-stream:
    - https://developer.arm.com/documentation/ihi0051/latest/
    - https://docs.xilinx.com/r/en-US/pg256-sdfec-integrated-block/AXI4-Stream-Interface

Testbench

- fir_tb(Please name your top module same as **fir** for simulation)
- The testbench should keep in the same directory with Makefile
- Block-level Protocol (ap_start, ap_done):



AP_CTRL_HS (Sequential Executed Kernel)

- Host and Kernel Synchronization by
  - ap_start
  - ap_done
- Kernel can only be restarted (ap_start), after it completes the current execution (ap_done)
- Serving one execution request a time

Test dataset

- Samples_triangular_wave.dat
- out_gold.dat

Submission (1/2)

- Hierarchy:
  - StudentID_lab3/
    - Waveform
    - Simulation.log
    - Report.pdf
    - Synthesis report
    - Github link
- Your Github link should attach the file
  - Design, Synthesis report(Including FF, LUT, Bram), Waveform, simulation.log, makefile,…etc.
  - Report
- Location of design (If use vivado to design)
  - hostproject/hostproject.srcs/sources_1/new/

What is included in the report

- Block Diagram
    - Datapath – dataflow
    - Control signals
- Describe operation, e.g.
    - How to receive data-in and tap parameters and place into SRAM
    - How to access shiftram and tapRAM to do computation
    - How ap_done is generated.
    - …..
- Resource usage: including FF, LUT, BRAM
- Timing Report
    - Try to synthesize the design with maximum frequency
    - Report timing on longest path, slack
- Simulation Waveform, show
    - Coefficient program, and read back
    - Data-in stream-in
    - Data-out stream-out
    - Bram access control
    - FSM

Submission (2/2)

- Compress all above files in a single zip file named
  - StudentID_lab3.zip (e.g., 111061545_lab3.zip)
- Submit to NTHU eeclass
- Deadline:

  - 20% off for the late submission penalty within 3 days