

# CPLD Architecture



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Title Slide

## CPLD Architecture – forerunner of the FPGA

The Complex Programmable Logic Device, or CPLD, was the forerunner of the FPGA, and is still useful today in certain applications.

We will examine the historical development of CPLD in order to understand the limitations and advantages that flow from the architecture of these devices.

Most major PLD vendors, including Xilinx, Altera, and Lattice offer a wide range of CPLD devices for sale.



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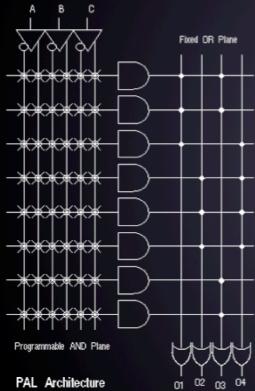
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## CPLD Architecture – forerunner of FPGA



- ⇒ Recall the PAL, which created sum of products logic functions using a programmable AND array followed by a fixed OR array. This allowed the replacement of up to a dozen discrete logic packages with a general logic solution, because arbitrary logic functions could be implemented in the disjunctive normal form.
- ⇒ Altera extended this concept by putting multiple PAL structures called macrocells in a single integrated circuit package in which all the input pins were available to each macrocell, and any output pin could be driven by any macrocell.



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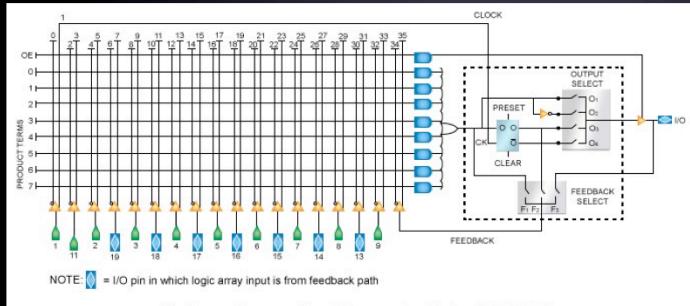
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<http://web.engr.oregonstate.edu/~sllu/fpga/lec1.html> Here

Recall the PAL, which created sum of products logic functions using a programmable AND array followed by a fixed OR array. This allowed the replacement of up to a dozen discrete logic packages with a general logic solution, because arbitrary logic functions could be implemented in the disjunctive normal form.

Altera extended this concept by putting multiple PAL structures called macrocells in a single integrated circuit package in which all the input pins were available to each macrocell, and any output pin could be driven by any macrocell. CPLDs were also built in CMOS to be reprogrammable, while bipolar PALs were not. Although it didn't seem to be a major attribute at the time, reprogrammability is now considered a very important aspect of PLD devices. The program that defined the interconnections in CPLDs is stored in an on-chip EEPROM.

## CPLD early device architecture



Altera extended this concept by putting multiple PAL structures called macrocells in a single integrated circuit package in all the input pins were available to each macrocell, and each macrocell had a dedicated output pin which could be fed back to the input array.

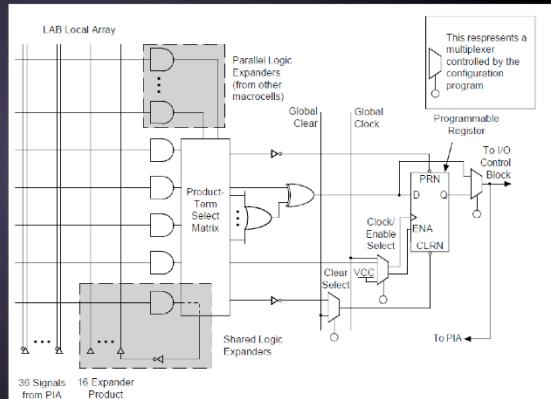
Ron Wilson, (2016/11/06). *In the Beginning*. [Online]. Available: [https://www.altera.com/solutions/technology/system-design/articles/\\_2013/in-the-beginning.html](https://www.altera.com/solutions/technology/system-design/articles/_2013/in-the-beginning.html)

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With the ability to look at 16 digital inputs at a time, each macrocell could decode a 16-bit address from a processor and generate a chip select. In this way, a single chip with 8 or 16 macrocells could create chip selects for an entire microprocessor system, and hence CPLD's were associated with processor system "glue logic".

## CPLD Macrocell

CPLD Macrocell is basically  
Just a registered PAL array



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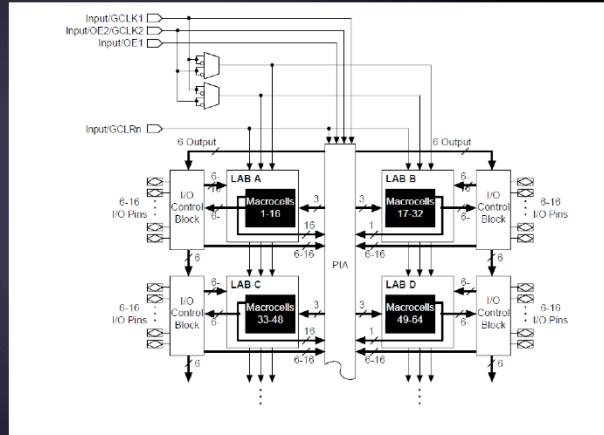
J. Hamblen, T. Hall, M. Furman, "Programmable Logic Technology", in *Rapid Prototyping of Digital Systems*, New York: Springer, 2008, p. 60.

Here's a picture of another CPLD macrocell. You can see that a CPLD Macrocell is basically just a registered PAL Array. The Mux symbols represent programmable configuration switches present in the device. The PIA is a matrix of interconnecting wires that connects the macrocells together, feeding the output of the cells to the inputs of other cells.

This structure is good for problems that require a good deal of logic for every flip-flop, like a complex 16-state state machine or wide input decoder.

## What's this programmable logic stuff anyway?

CPLD Top Level Architecture is PAL Macrocells connected Interconnection wires. Number of wires tends to Increase as N squared, making cost rise exponentially.



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J. Hamblen, T. Hall, M. Furman, "Programmable Logic Technology", in *Rapid Prototyping of Digital Systems*, New York: Springer, 2008, p. 61.

The CPLD Top Level Architecture is PAL Macrocells connected with Interconnection wires. The Number of wires tends to increase as N squared, making cost of the interconnections rise exponentially. To mitigate this problem, the interconnect was partitioned, so that every macrocell did not have all inputs present.

Here we see the CPLD is made of bigger groups of circuits called LAB's. What is an LAB? A LAB is an Logic Array Block, made of 16 Macrocells with local routing between the macrocells. The Programmable Interconnect Array, or PIA is a routing network between LABs, so it is apparent that CPLDS are inherently hierarchical devices. Hierarchy, which creates larger logical systems out of many smaller logic functions is an important concept in logic design. One consequence of this is the designer now had to plan which macrocells would implement a particular logic equation, and which ones need the result, and also take into account the delays possible through the interconnections and hierarchy. Better software tools were developed to assist in this planning.

## CPLD Architecture Summary

- The CPLD introduced reprogrammability to programmable logic devices, an important new feature.
- The architecture of the CPLD allowed for easy design of wide input combinational logic functions, like address decoders and state machines with deterministic timing.
- However, the CPLD architecture did not scale effectively for designs that required many flip-flops – this has become the province of the FPGA.



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In this video we have learned

The CPLD introduced reprogrammability to programmable logic devices, an important new feature. CPLDs also reinforced hierarchical design methods.

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However, the CPLD architecture did not scale effectively for designs that required many flip-flops – this has become the province of the FPGA.