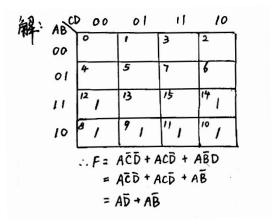
第一章课后作业

2154312 郑博远

8.(3)

10.(2)



11.(3)

Verilog 代码:

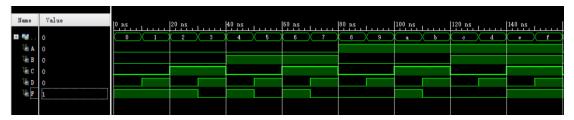
```
module test1(
   input A,
   input B,
   input C,
   input D,
   output F
   );

wire notA, notB, notC, notD, ans1, ans2, ans3, ans4;

nand (notA, A, A);
   nand (notB, B, B);
   nand (notC, C, C);
   nand (notD, D, D);

nand(ans1, notA, notB, notC);
```

```
nand(ans2, notA, B, notD);
nand(ans3, notB, C, notD);
nand(ans4, A, B, C);
nand(F, ans1, ans2, ans3, ans4);
endmodule
```



逻辑图:

