Assignment 1

Student ID:2154312 Name:郑博远

1. After the third pulse, the output would be 1 and 1;

   After the fourth pulse, the output would be 0 and 0.

   The reason is as follows: after the third pulse, the input of the bottom flip-flop would change from 0 to 1, causing its output to flip from 0 to 1; so the second flip-flop's input(received from the output of the NOT gate) would change from 1 to 0, and thus its output would remain 1. This is why the output would be 1 and 1; after the fourth pulse, the input of the bottom flip-flop would change from 0 to 1 again, causing its output to flip from 1 to 0; so the second flip-flop's input would change from 0 to 1, causing its output to change state from 1 to 0 too. This is why the output would be 0 and 0 after the fourth pulse.

2. On the 2st, 6th, 10th … pulses of the clock, a 1 will be sent on output B;

   On the 3st, 7th, 11th … pulses of the clock, a 1 will be sent on output C;

   On none of the outputs is a 1 sent on the 4th pulse.

   The reason is as follows: according to the answer of Question 1, the output of such a circuitry is cyclical as: 01, 10, 11, 00 … Because of the NOT gate and the AND gate, the output of A would be 1, 0, 0, 0 in one cycle; the output of B would be 0, 1, 0, 0 in one cycle, which means the 2st, 6th, 10th… pulses will send a 1 on output B; similarly, the 3st, 7th, 11th… pulses will send a 1 on output C. In conclusion, none of the output will be a 1 on the 4th pulse.

3. (1024 × 768 × 3 × 8) / 8 = 2359296 bytes

So 2359296 bytesize memory cells are required.

4. a. HE

b. FED

c. DEAD

d. CABBAGE

e. CAFE

5.

program counter	instruction register	memory cell at address 0x02
0x02	0x2211	0x32
0x04	0x3202	0x11
0x06	0xC000	0x11

6. a. 0x04

b. 0x04

c. 0x0E

The reason is as follows: we first get the instruction at address 0x00, which is 0x2004, to load the register 0 with the bit pattern 0x04; then as the program counter is incremented to 0x02, we get the instruction 0x2101 and load the register 1 with the bit pattern 0x01; then we get 0x4012 as the program counter points to 0x04, to move the bit pattern found in register 1 to register 2; then we get 0x5112 at address 0x06, to add the bit patterns in register 1 and 2 and leave the answer in register 1; then we get 0xB10C at address 0x08, and because the bit pattern in register 1 isn't equal to the bit pattern in register 0, we move on to get 0xB006 at address 0x10. The bit pattern in register 0 is the same to itself, causing the program counter

to point to 0x06, which means the program jumps to the instruction located there. So the bit pattern in register 1 will continuously be added 0x01 until it equals to the bit pattern in register 0. After that, the program counter will point to 0x0C, which is incremented to 0x0E after the instruction there is fetched. The instruction 0xC000 is decoded as the halt instruction, so the program is completed. This is why the bit patterns in register 0 and 1 are both 0x04.

7. a.

Address	Contents
0x00	0x10
0x01	0xD8
0x02	0x30
0x03	0xB3
0x04	0xC0
0x05	0x00

b.

Address	Contents
0x00	0x10
0x01	0xD8
0x02	0x11
0x03	0xB3
0x04	0x31
0x05	0xD8
0x06	0x30
0x07	0xB3
0x08	0xC0
0x09	0x00

8. $(200 \times 1024 \times 1024 \times 1024) / (15 \times 1000 \times 1000) / (60 \times 60)$

$= 3.98$ hours