第四章课后作业 2

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P164

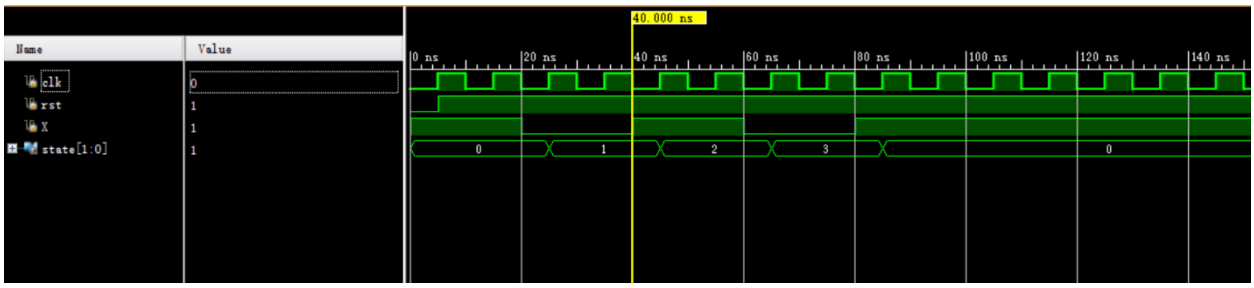
21.

```
module test1(
    input clk,
    input rst,
    input X,
    output[1:0] state
    );

    parameter S0 = 2'b00;
    parameter S1 = 2'b01;
    parameter S2 = 2'b10;
    parameter S3 = 2'b11;

    reg[1:0] cur_state;
    assign state = cur_state;

    always@ (posedge clk or negedge rst)
    begin
    if(~rst)
        cur_state = S0;
    else
       begin
           case(cur_state)
               S0: if(X) cur_state <= S0;
                   else cur_state <= S1;
               S1: if(X) cur_state <= S2;
                   else cur_state <= S1;
               S2: if(X) cur_state <= S2;
                   else cur_state <= S3;
               S3: if(X) cur_state <= S0;
                   else cur_state <= S3;
               default:
                   cur_state <= S0;
           endcase
       end
    end

endmodule
```

testbench 如下：

```
module test1_tb();
    reg clk;
    reg rst;
    reg X;
    wire[1:0] state;

    initial
    begin
        clk = 0;
    forever
        clk = #5 ~clk;
    end;


    initial
    begin
        X = 1;
        rst = 0;
        #5;
        rst = 1;
        #10;
        X = 0;
        #10;
        X = 0;
        #10;
        X = 1;
        #10;
        X = 1;
        #10;
        X = 0;
        #10;
        X = 0;
        #10;
        X = 1;
    end

    test1 test1_inst(clk, rst, X, state);

endmodule
```

仿真波形图如下：



测试了每个状态下不同输入的状态转移，符合题目中对状态机的描述。