In this homework we have five project options. You only need to pick one of them and finish it completely using full-custom approach. Your report must at least include circuit, layout, pre-layout and post-layout simulation results, LVS result, and DRC result. Also you may add I/O pads to your circuit core and run off-line DRC.

Project 1: Design and implement an 4×4 Booth's array multiplier (Slide 12-59) studied in the class.

Project 2: Design and implement an 8-bit synchronous binary counter.

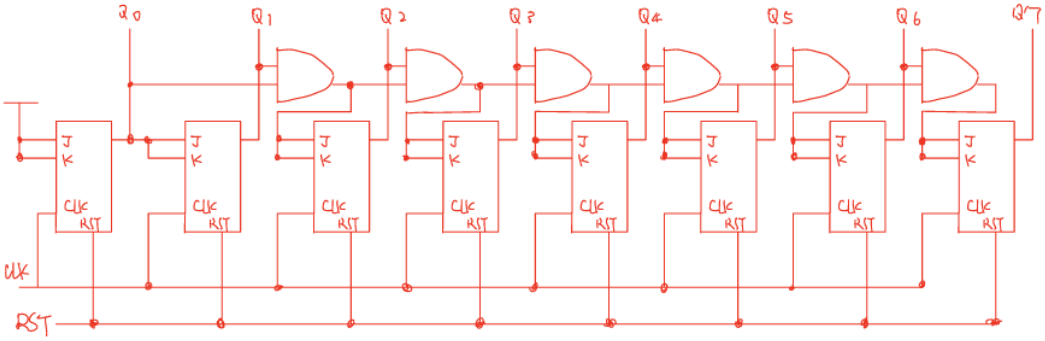
Project 3: Design and implement an 8-bit carry-lookahead adder.

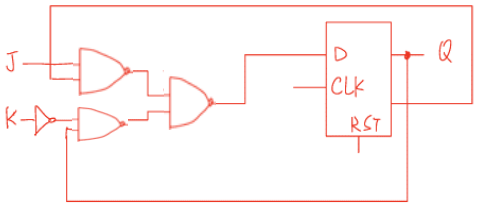
Project 4: Design and implement an 8-bit carry-skip adder.

Project 5: Design and implement the non-restoring array divider (Slides 12-63 and 12-64) studied in the class.

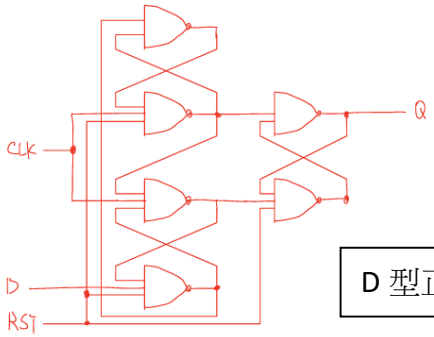
此次作業選擇 project 2:實作一個 8 bit 的二元計數器。

初步設計:透過 8 個 JK 正反器搭配 AND 來實現計數器。



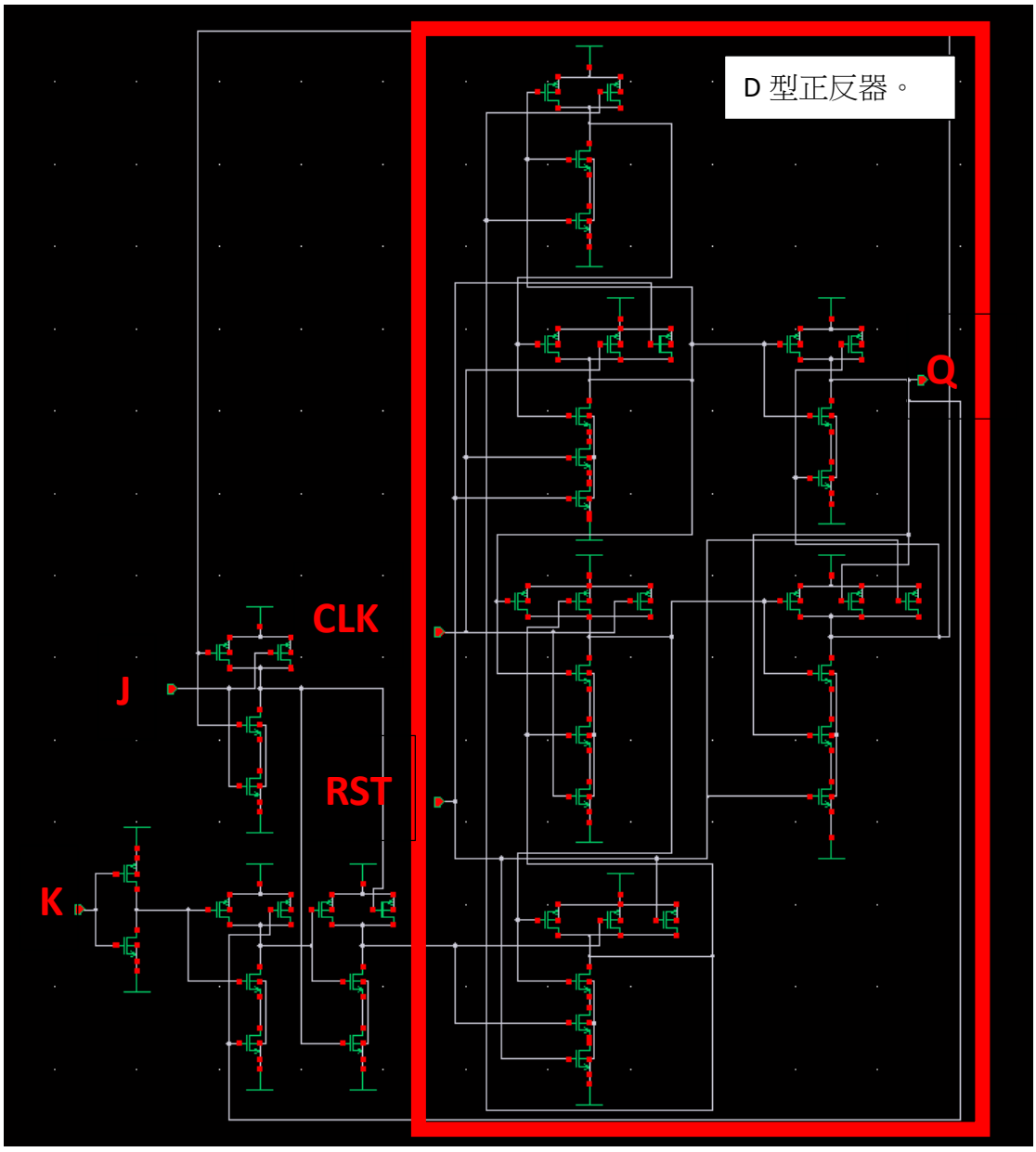


透過 D 型正反器來實現 JK 正反器。

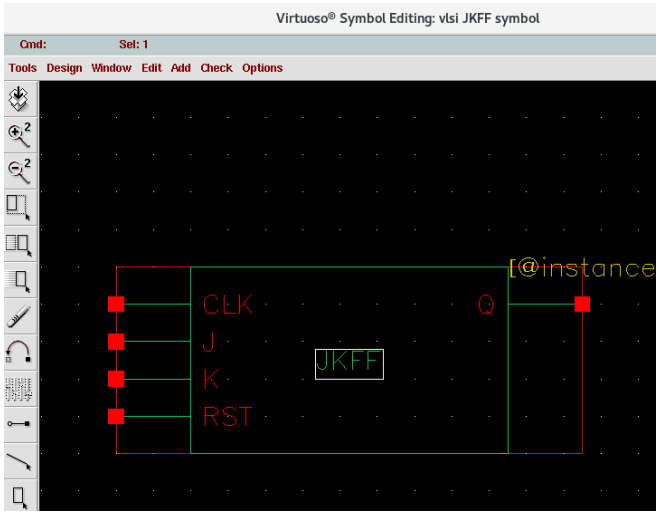


D 型正反器。

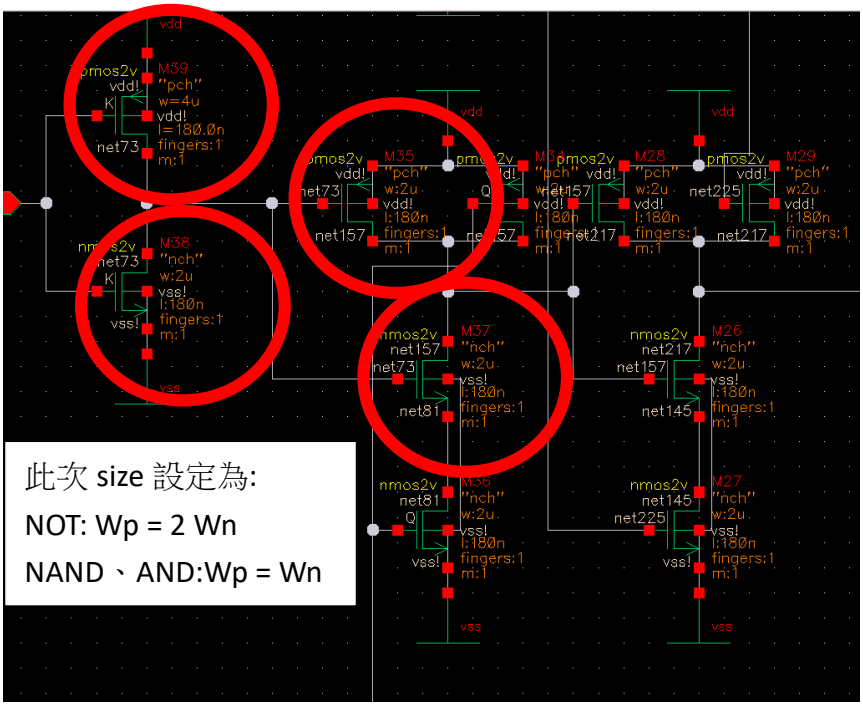
實作:



JK 正反器-schemetic。

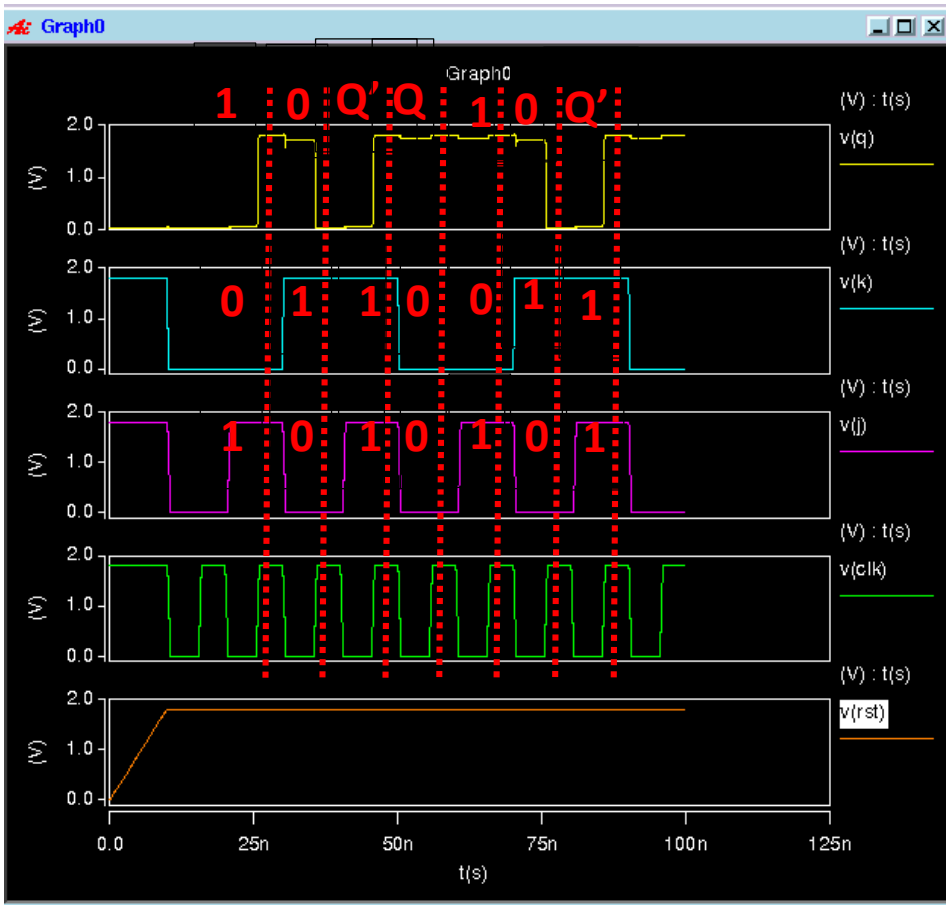


將 JK 正反器設定成 symbol
方便後續設計計數器。



此次 size 設定為:
NOT: Wp = 2 Wn
NAND、AND:Wp = Wn

JK 正反器功能測試



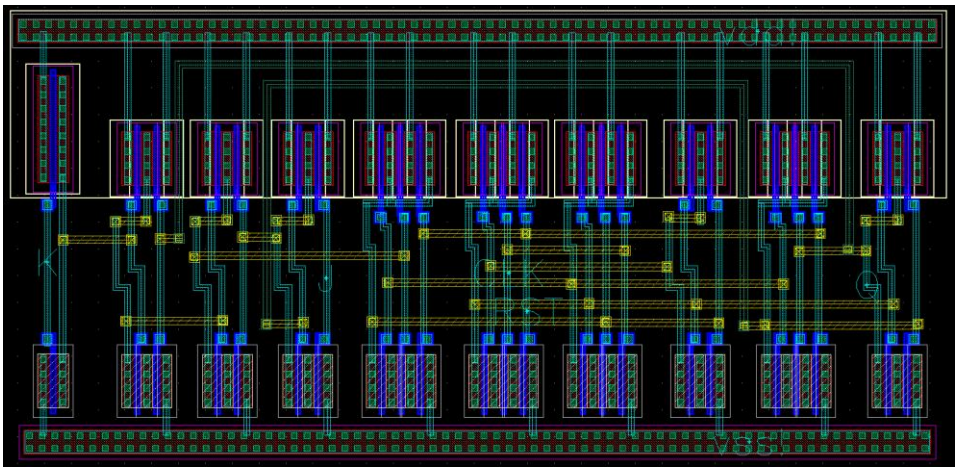
Truth Table

CLK	J	K	Q n+1
↑	0	0	Q n
↑	0	1	0
↑	1	0	1
↑	1	1	Q n'

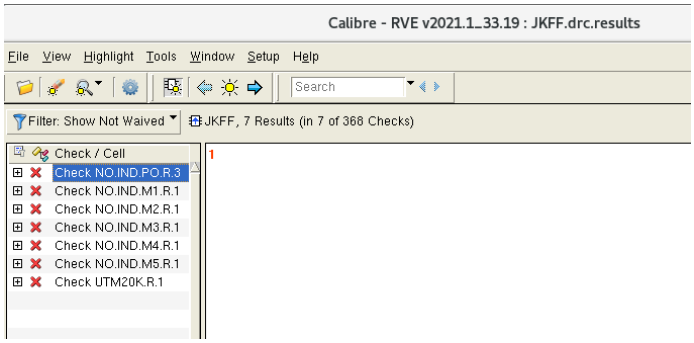
SP 檔(無測 delay)

```
*JKFF.sp
MM7 net183 CLK vdd! vdd! pmos l=180n w=2u m=1
MM8 net177 net217 vdd! vdd! pmos l=180n w=2u m=1
MM9 net177 net181 vdd! vdd! pmos l=180n w=2u m=1
MM12 net181 net183 vdd! vdd! pmos l=180n w=2u m=1
MM13 net181 net177 vdd! vdd! pmos l=180n w=2u m=1
MM14 net181 CLK vdd! vdd! pmos l=180n w=2u m=1
MM20 Q net183 vdd! vdd! pmos l=180n w=2u m=1
MM21 Q net227 vdd! vdd! pmos l=180n w=2u m=1
MM22 net227 Q vdd! vdd! pmos l=180n w=2u m=1
MM23 net227 net181 vdd! vdd! pmos l=180n w=2u m=1
MM40 net183 RST vdd! vdd! pmos l=180n w=2u m=1
MM42 net177 RST vdd! vdd! pmos l=180n w=2u m=1
MM0 net167 net183 vdd! vdd! pmos l=180n w=2u m=1
MM1 net167 net177 vdd! vdd! pmos l=180n w=2u m=1
MM28 net217 net157 vdd! vdd! pmos l=180n w=2u m=1
MM29 net217 net225 vdd! vdd! pmos l=180n w=2u m=1
MM32 net225 net227 vdd! vdd! pmos l=180n w=2u m=1
MM33 net225 J vdd! vdd! pmos l=180n w=2u m=1
.ENDS

.lib "PTM180.l" cmos
xJKFF CLK J K Q RST JKFF
vdd vdd! 0 1.8
vss vss! 0 0
VCLK CLK 0 pulse( 1.8 0 10n 0.5n 0.5n 4.9n 10n )
VJ J 0 pulse( 1.8 0 10n 0.5n 0.5n 9.9n 20n )
VK K 0 pulse( 1.8 0 10n 0.1n 0.1n 19.9n 40n )
VRST RST 0 PWL(0n 0v 10n 1.8v)
.trans 1ps 100ns


.probe tran V(CLK) V(J) V(K) V(RST) V(Q)
.option post=2
.end
```

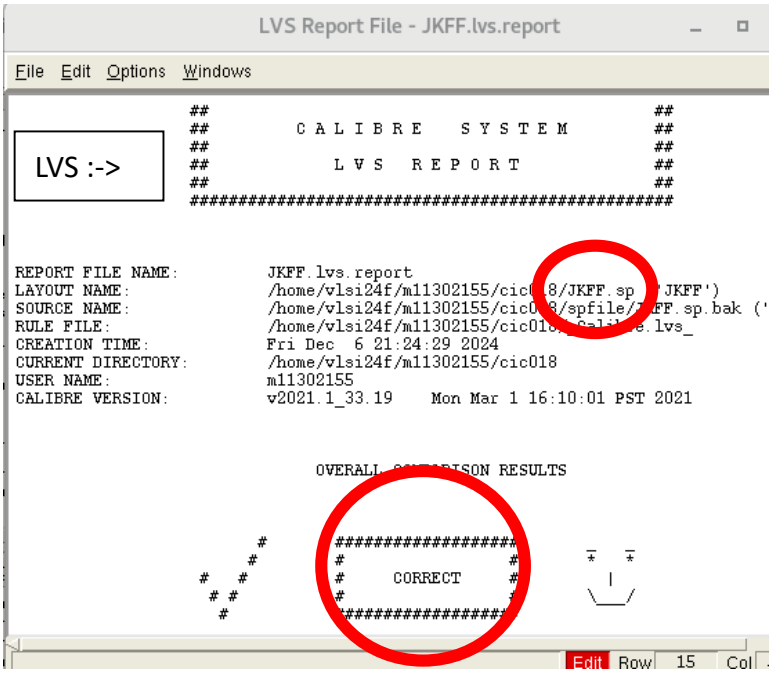
JK layout



DRC:全為 density 問題(忽略)

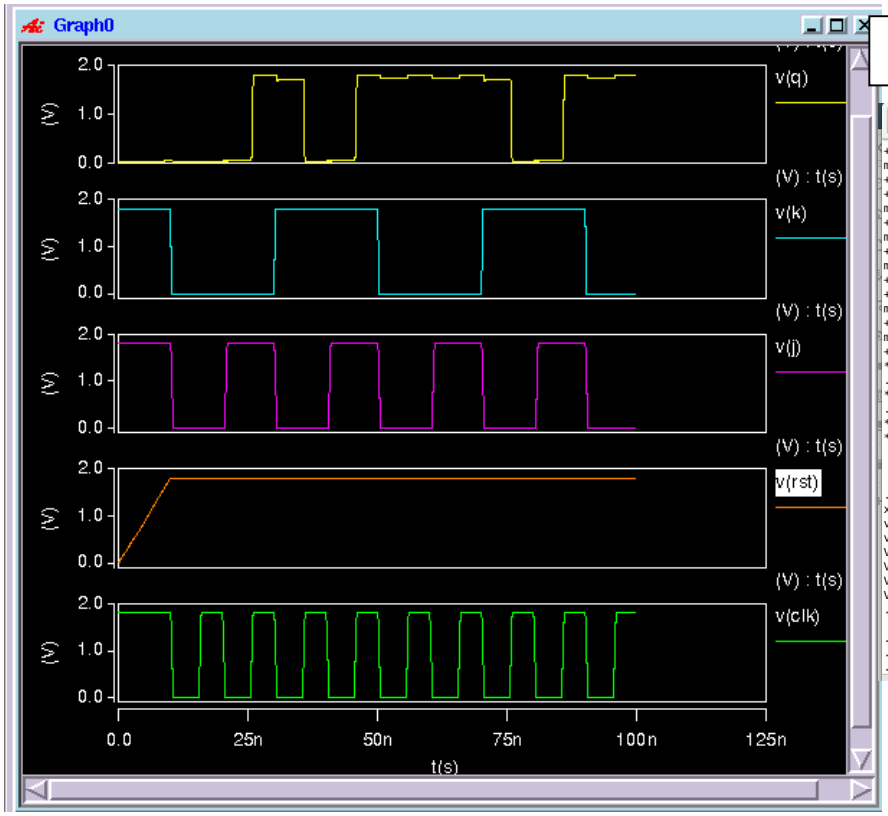


LVS :->



```
JKFF.lvs.report.ext
JKFF.pex.sp
JKFF.pex.sp.JKFF.pxi
JKFF.pex.sp.pex
```

PEX :檔案如圖



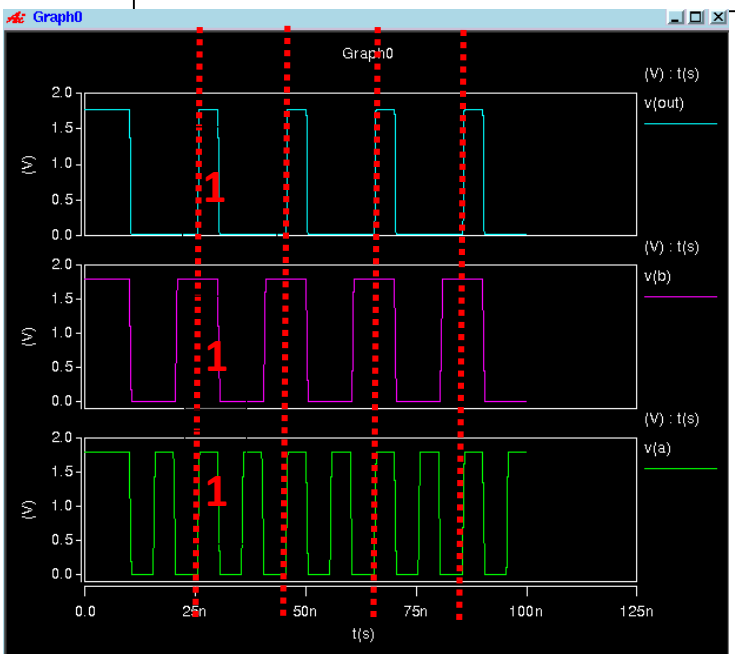
PEX :測試波形

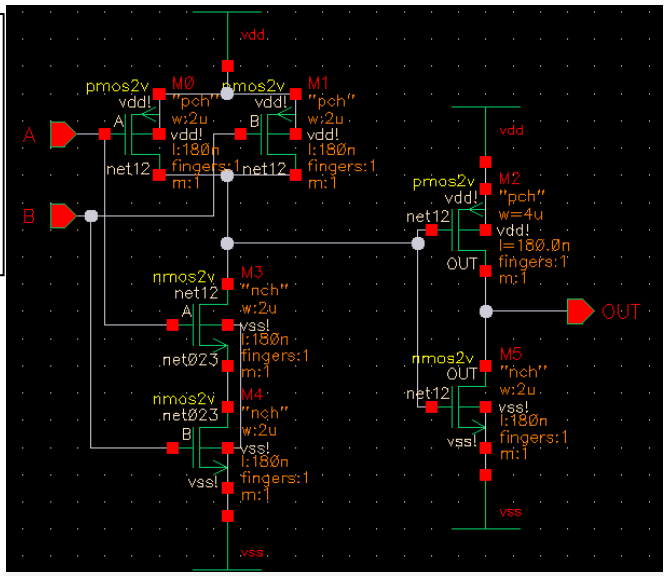
```
Open
*JKFF.pex.sp
~/cic018/pex

+ NRS=0.135
mX39/M0 N_8_X39/M0_d N_CLK_X39/M0_g N_VDD!_X39/M0_s N_VDD!_X37/M1_b pmos
+ L=1.8e-07 W=2e-06 AD=9.6e-13 AS=5.4e-13 PD=4.96e-06 PS=2.54e-06 NRD=0.24
+ NRS=0.135
mX39/M1 N_8_X39/M1_d N_13_X39/M1_g N_VDD!_X39/M1_s N_VDD!_X37/M1_b pmos L=1.8e-07
+ W=2e-06 AD=5.4e-13 AS=9.6e-13 PD=2.54e-06 PS=4.96e-06 NRD=0.135 NRS=0.24
mX39/M2 N_VDD!_X39/M2_d N_14_X39/M2_g N_8_X39/M2_s N_VDD!_X37/M1_b pmos L=1.8e-07
+ W=2e-06 AD=5.4e-13 AS=5.4e-13 PD=2.54e-06 PS=2.54e-06 NRD=0.135 NRS=0.135
mX40/M0 N_6_X40/M0_d N_RST_X40/M0_g N_VDD!_X40/M0_s N_VDD!_X37/M1_b pmos
+ L=1.8e-07 W=2e-06 AD=9.6e-13 AS=5.4e-13 PD=4.96e-06 PS=2.54e-06 NRD=0.24
+ NRS=0.135
mX40/M1 N_6_X40/M1_d N_8_X40/M1_g N_VDD!_X40/M1_s N_VDD!_X37/M1_b pmos L=1.8e-07
+ W=2e-06 AD=5.4e-13 AS=9.6e-13 PD=2.54e-06 PS=4.96e-06 NRD=0.135 NRS=0.24
mX40/M2 N_VDD!_X40/M2_d N_Q_X40/M2_g N_6_X40/M2_s N_VDD!_X37/M1_b pmos L=1.8e-07
+ W=2e-06 AD=5.4e-13 AS=5.4e-13 PD=2.54e-06 PS=2.54e-06 NRD=0.135 NRS=0.135
*
.include "JKFF.pex.sp.JKFF.pxi"
*
.ends
*
*


.lib "PTM180.l" cmos
xJKFF K Q J RST CLK VSS! VDD! JKFF
vdd vdd! 0 1.8
vss vss! 0 0
VCLK CLK 0 pulse( 1.8 0 10n 0.5n 0.5n 4.9n 10n )
VJ J 0 pulse( 1.8 0 10n 0.5n 0.5n 9.9n 20n )
VK K 0 pulse( 1.8 0 10n 0.1n 0.1n 19.9n 40n )
VRST RST 0 PWL(0n 0v 10n 1.8v)
.trans 1ps 100ns

.probe tran V(CLK) V(J) V(K) V(RST) V(Q)
.option post=2
.end
```

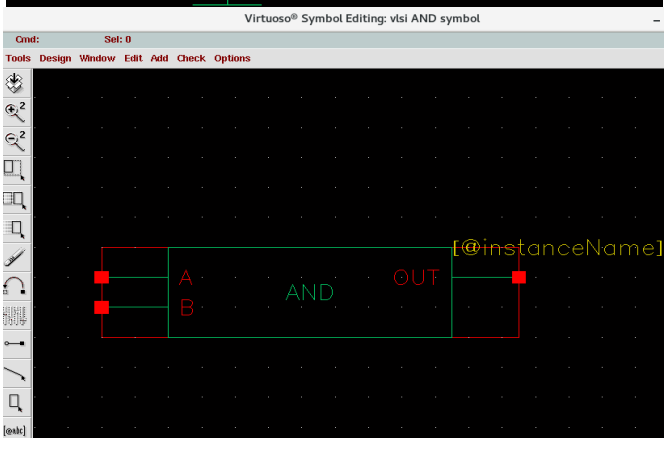
SP 檔(無測 delay)

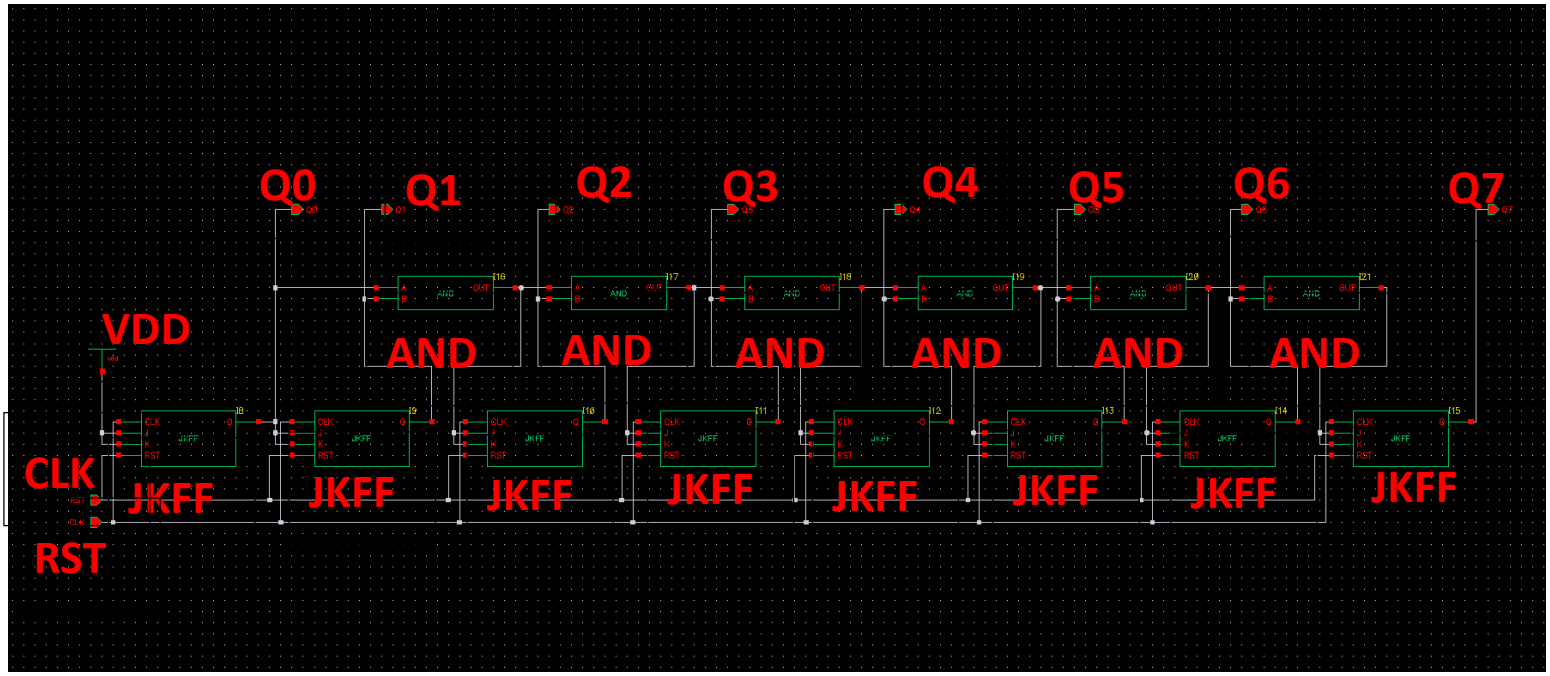
AND 如同右圖(之前作業有透過 NAND 練習)，一樣透過創立 symbol 的方式，方便後續呼叫(AND 並沒有額外測試 DRC、LVS 等)。

波形圖如下







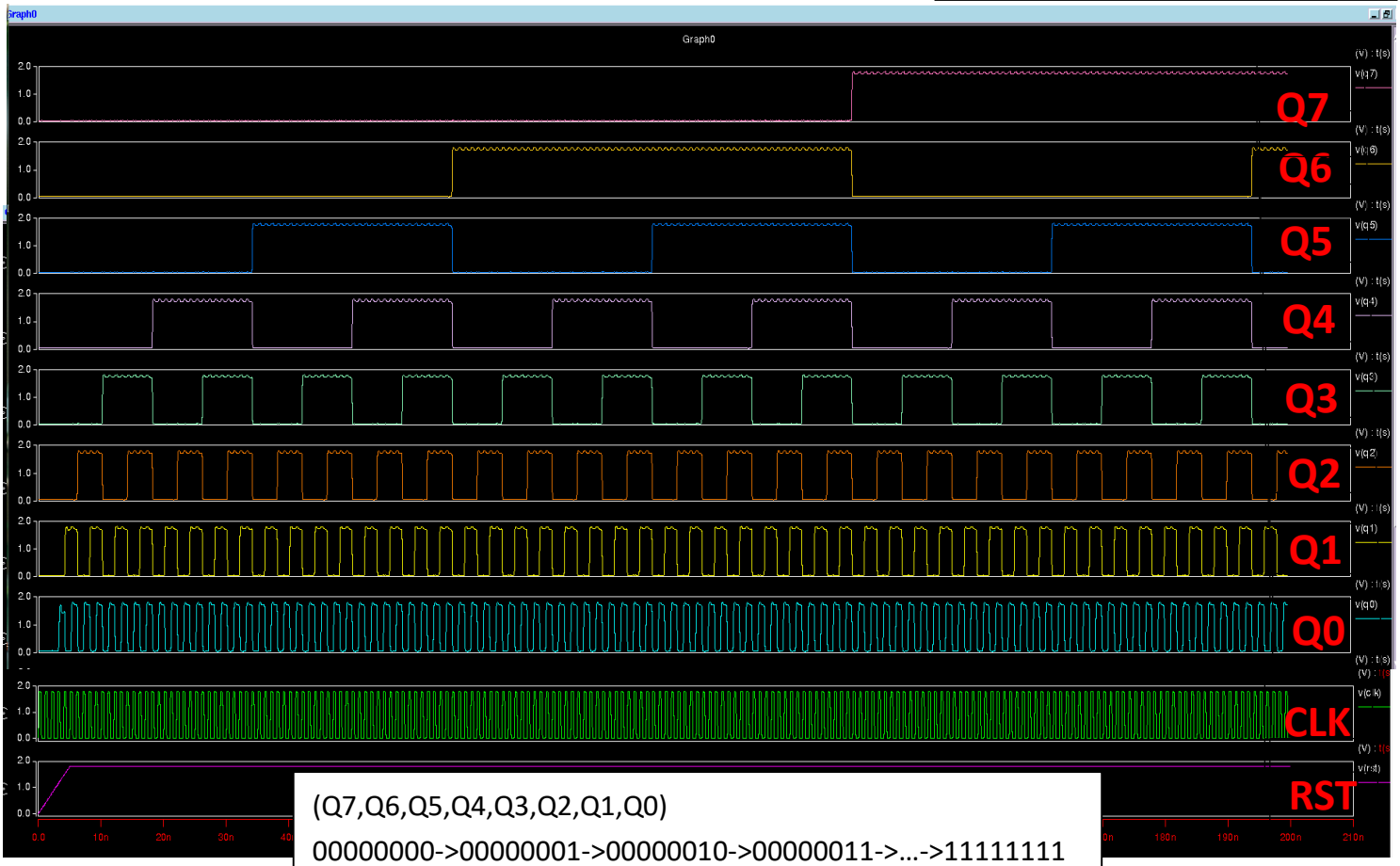


Open *bit8_syn_binary_counter.sp ~/cic018/spfile

```
********************************************************************************
* Library Name: vlsi
* Cell Name:    bit8_syn_binary_counter
* View Name:    schematic
********************************************************************************

.SUBCKT bit8_syn_binary_counter CLK Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 RST
*.PININFO CLK:I RST:I Q0:O Q1:O Q2:O Q3:O Q4:O Q5:O Q6:O Q7:O
XI16 Q0 Q1 net131 / AND
XI18 net125 Q3 net119 / AND
XI17 net131 Q2 net125 / AND
XI20 net107 Q5 net137 / AND
XI19 net119 Q4 net107 / AND
XI21 net137 Q6 net143 / AND
XI8 CLK vdd! vdd! Q0 RST / JKFF
XI13 CLK net107 net107 Q5 RST / JKFF
XI9 CLK Q0 Q0 Q1 RST / JKFF
XI12 CLK net119 net119 Q4 RST / JKFF
XI11 CLK net125 net125 Q3 RST / JKFF
XI10 CLK net131 net131 Q2 RST / JKFF
XI14 CLK net137 net137 Q6 RST / JKFF
XI15 CLK net143 net143 Q7 RST / JKFF
.ENDS

.lib "PTM180.l" cmos
xbit8_syn_binary_counter CLK Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 RST bit8_syn_binary_counter
vdd vdd! 0 1.8
vss vss! 0 0
vCLK CLK 0 pulse (0 1.8 0 0.1n 0.1n 0.3n 1n)
VRST RST 0 PWL(0n 0v 5n 1.8v)
.trans 1ps 200ns

.probe tran V(CLK) V(RST) V(Q0) V(Q1) V(Q2) V(Q3) V(Q4) V(Q5) V(Q6) V(Q7)
.option post=2
.end
```

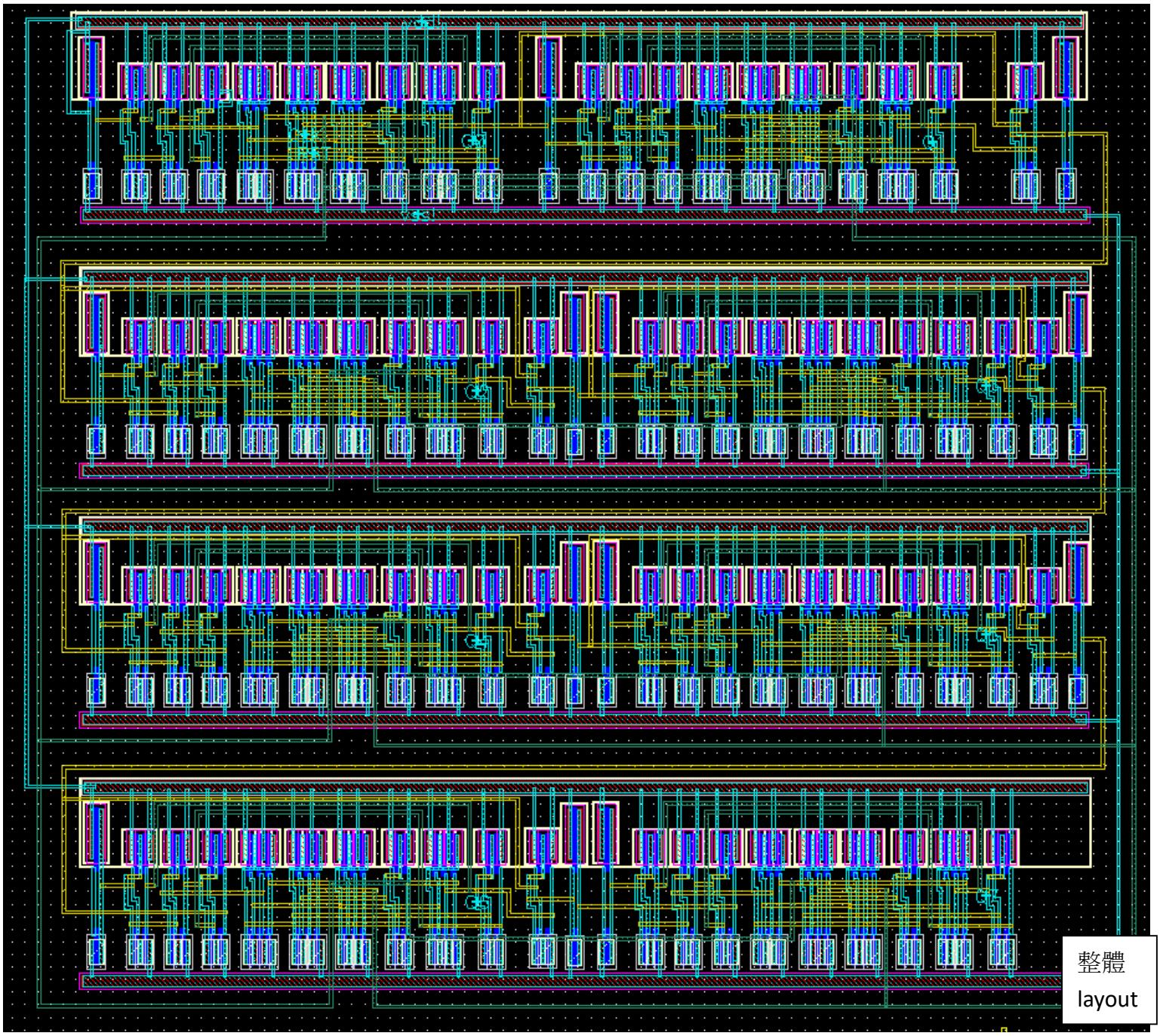
SP 檔(無測 delay)

可以看到每個 Qn+1 的頻率都是 Qn 的 1/2 倍。



(Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0)

00000000->00000001->00000010->00000011->...->11111111



Calibre - RVE v2021.1_33.19 : bit8_syn_binary_counter.drc.results

File View Highlight Tools Window Setup Help

Filter: Show Unresolved | bit8_syn_binary_counter, 7 Results (in 7 of 368 Checks)

Check / Cell
- Check NO.IND.PO.R.3
- Check NO.IND.M1.R.1
- Check NO.IND.M2.R.1
- Check NO.IND.M3.R.1
- Check NO.IND.M4.R.1
- Check NO.IND.M5.R.1
- Check UTM20K.R.1

DRC:全為 density 問題(忽略)

NO.IND.PO.R.3 (@ Min. density of POLY area >= 14% (exclude application for inductor)
ALL_POLY_NIND = POLY1 OR DPO
POLYT_NIND = ALL_POLY_NIND NOT INDDMY
CHIP_NIND = CHIP NOT INDDMY

LVS Report File - bit8_syn_binary_counter.lvs.report

File Edit Options Windows

LVS :->

```
                  ##                                          ##
                  ##        C A L I B R E   S Y S T E M       ##
                  ##                                          ##
                  ##           L V S   R E P O R T            ##
                  ##                                          ##
                  ##############################################


REPORT FILE NAME:          bit8_syn_binary_counter.lvs.report
LAYOUT NAME:               /home/vlsi24f/m11302155/cic018/bit8_syn_binary_counte
SOURCE NAME:               /home/vlsi24f/m11302155/cic018/spfile/bit8_syn_binary_
RULE FILE:                 /home/vlsi24f/m11302155/cic018/_calibre.lvs_
CREATION TIME:             Fri Dec  6 21:44:19 2024
CURRENT DIRECTORY:         /home/vlsi24f/m11302155/cic018
USER NAME:                 m11302155
CALIBRE VERSION:           v2021.1_33.19    Mon Mar 1 16:10:01 PST 2021


                    OVERALL COMPARISON RESULTS

                        ###################
                        #                 #
                        #     CORRECT     #
                        #                 #
                        ###################


********************************************************************************
                            CELL  SUMMARY
********************************************************************************
```

Edit Row 25 Col 25

```
bit8_syn_binary_counter.calibre.db
bit8_syn_binary_counter.lvs.report.ext
bit8_syn_binary_counter.pex.ic0
bit8_syn_binary_counter.pex.lis
bit8_syn_binary_counter.pex.mt0
bit8_syn_binary_counter.pex.pa0
bit8_syn_binary_counter.pex.sp
bit8_syn_binary_counter.pex.sp.BIT8_SYN_BINARY_COUNTER.pxi
bit8_syn_binary_counter.pex.sp.pex
bit8_syn_binary_counter.pex.st0
bit8_syn_binary_counter.pex.tr0
```

PEX :檔案如圖

Open *bit8_syn_binary_counter.pex.sp ~/cic018/pex

```
mX125/X17/M0 N_78_X125/X17/M0_d N_CLK_X125/X17/M0_g N_VDD!_X125/X17/M0_s
+ N_VDD!_X71/M0_b pmos L=1.8e-07 W=2e-06 AD=9.6e-13 AS=5.4e-13 PD=4.96e-06
+ PS=2.54e-06 NRD=0.24 NRS=0.135
mX125/X17/M1 N_78_X125/X17/M1_d N_89_X125/X17/M1_g N_VDD!_X125/X17/M1_s
+ N_VDD!_X71/M0_b pmos L=1.8e-07 W=2e-06 AD=5.4e-13 AS=9.6e-13 PD=2.54e-06
+ PS=4.96e-06 NRD=0.135 NRS=0.24
mX125/X17/M2 N_VDD!_X125/X17/M2_d N_92_X125/X17/M2_g N_78_X125/X17/M2_s
+ N_VDD!_X71/M0_b pmos L=1.8e-07 W=2e-06 AD=5.4e-13 AS=5.4e-13 PD=2.54e-06
+ PS=2.54e-06 NRD=0.135 NRS=0.135
mX125/X18/M0 N_74_X125/X18/M0_d N_RST_X125/X18/M0_g N_VDD!_X125/X18/M0_s
+ N_VDD!_X71/M0_b pmos L=1.8e-07 W=2e-06 AD=9.6e-13 AS=5.4e-13 PD=4.96e-06
+ PS=2.54e-06 NRD=0.24 NRS=0.135
mX125/X18/M1 N_74_X125/X18/M1_d N_78_X125/X18/M1_g N_VDD!_X125/X18/M1_s
+ N_VDD!_X71/M0_b pmos L=1.8e-07 W=2e-06 AD=5.4e-13 AS=9.6e-13 PD=2.54e-06
+ PS=4.96e-06 NRD=0.135 NRS=0.24
mX125/X18/M2 N_VDD!_X125/X18/M2_d N_Q3_X125/X18/M2_g N_74_X125/X18/M2_s
+ N_VDD!_X71/M0_b pmos L=1.8e-07 W=2e-06 AD=5.4e-13 AS=5.4e-13 PD=2.54e-06
+ PS=2.54e-06 NRD=0.135 NRS=0.135
*
.include "bit8_syn_binary_counter.pex.sp.BIT8_SYN_BINARY_COUNTER.pxi"
*
.ends
*
*

.lib "PTM180.l" cmos
xbit8_syn_binary_counter VDD! Q0 Q6 Q4 Q2 RST CLK Q1 Q7 Q5 Q3 VSS! bit8_syn_binary_counter
vdd vdd! 0 1.8
vss vss! 0 0
vCLK CLK 0 pulse (0 1.8 0 0.1n 0.1n 0.3n 1n)
VRST RST 0 PWL(0n 0v 5n 1.8v)
.trans 1ps 200ns

.probe tran V(CLK) V(RST) V(Q0) V(Q1) V(Q2) V(Q3) V(Q4) V(Q5) V(Q6) V(Q7)
.option post=2
.end
```

SP 檔(無測 delay)

PEX 後的波形與前模擬一樣