

Wideband Trans-Impedance Amplifier Design

i. Introduction and literature search

TIAs have evolved from basic resistor-based designs to sophisticated feedback circuits optimized for modern applications like optical communications and RF receivers. The first notable implementations (e.g., Miller's 1967 patent) laid the groundwork for today's designs, which tackle challenges of high-speed data rates and noise management. The use of feedback topologies to regulate input impedance and extend bandwidth is a cornerstone of modern TIA designs. The current research trends including minimizing power consumption while meeting high-performance metrics; Integration of TIAs in mixed-signal systems for compact and low-cost solutions; Enhanced modeling for parasitics, thermal noise, and stability in low-power and low-voltage environments.

Back to our project, wideband TIAs are necessary for high-speed systems, but they amplify noise, requiring careful optimization of gain and feedback elements. We need to carefully design the architecture to reach all the design requirement.

The examples of how TIA is optimized in two different scenario is given by Razavi's paper. In Optical Communication Systems, Feedback TIA with resistor is implemented. Use a resistive feedback network around a high-gain amplifier (common-source or CMOS inverter core) could reduce input impedance, stabilizing the response and extending bandwidth. Since TIA use photodiode as current source, having low input impedance is critical to handle the photodiode's parasitic capacitance.

In RF Communication Systems, TIA with Series Inductive Peaking is preferred. RF systems often deal with blockers and noise. Inductive peaking optimizes performance at specific frequencies while current-mode operation reduces nonlinearity. The architecture incorporates on-chip inductors to broaden bandwidth and can achieve a second-order system that manages stability and noise. For current mode, it minimizes voltage swings at sensitive nodes (e.g., at mixer inputs) to enhance linearity.

In summary, we learn some design method to improve the TIA's performance. In this task, I choose to use a 2-stage amplifier, which starts from a common gate amplifier, followed by a differential pair to generate differential output as required and each output equipped with an output buffer. The detailed design strategy will be given in part iii.

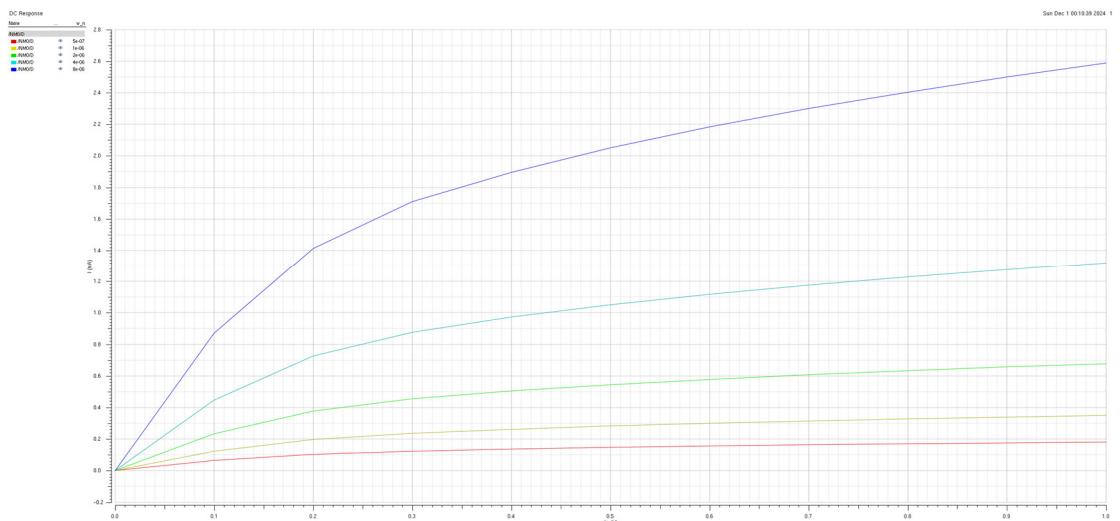
ii. Process Characterization

45nm Process parameter table (From HW3)

| Technology | NMOS 45nm | PMOS 45nm | Source |
|---|-----------|-----------|------------------------------------|
| μC_{ox} ($\mu A/V^2$) | 157.2 | 63.4 | Calculated from I_d |
| V_{t0} (V) | 0.45 | -0.45 | V_{th} from Cadence |
| $\lambda \cdot L$ ($\mu m/V$) | 0.117 | 0.105 | Calculated from I_d and r_{on} |
| C_{ox} (fF/ μm^2) | 17.78 | 19.11 | Calculated from C_{gs} |
| t_{ox} (nm) | 2.41 | 2.4 | Read from Cadence |
| $C_{ov}/W = L_{ov} C_{ox}$ (fF/ μm) | 0.152 | 0.152 | Read from Cadence |
| $C_{db}/W \approx C_{sb}/W$ (fF/ μm) | 0.0726 | 0.0266 | Read from Cadence |

1. I_D vs. V_{DS} (NMOS)

Simulation result:



Hand Calculation:

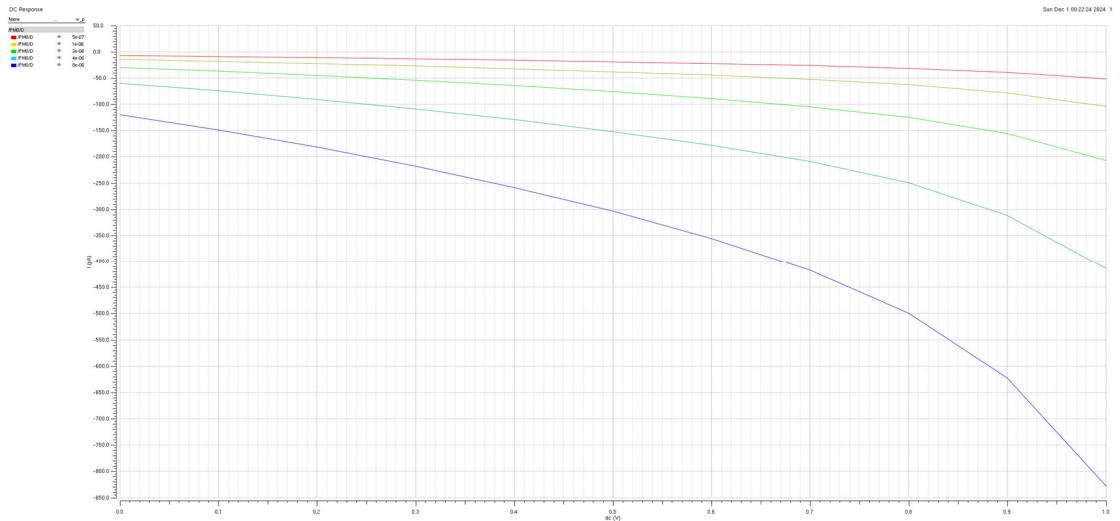
$$\begin{aligned}
 I_{D_N} &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 [1 + \lambda(V_{DS} - V_{eff})] \\
 &= \frac{1}{2} \times 157.2 \frac{\mu A}{V} \times \frac{W}{45nm} \times (1 - 0.45)^2 \times \left[1 + \frac{\frac{117nm}{V}}{45nm} (V_{DS} - 0.55) \right] \\
 &= 0.528W[1 + 2.6(V_{DS} - 0.55)] \mu A
 \end{aligned}$$

The trend is match with the simulation result. When $W = 8 \mu m$, $V_{DS} = 1V$

$$I_{D_N} = 0.528 \times 800[1 + 2.6(1 - 0.55)] \mu A = 0.916 mA$$

I_D vs. V_{DS} (PMOS)

Simulation result:



Hand Calculation:

$$\begin{aligned}
 I_{D_P} &= -\frac{1}{2}\mu_P C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 [1 + \lambda(V_{SD} - |V_{eff}|)] \\
 &= -\frac{1}{2} \times 63.4 \frac{\mu A}{V} \times \frac{W}{45nm} \times (-1 + 0.45)^2 \times \left[1 + \frac{\frac{105nm}{V}}{45nm} (V_{SD} - 0.55) \right] \\
 &= -0.213W[1 + 2.333(V_{SD} - 0.55)] \mu A
 \end{aligned}$$

The trend is match with the simulation result. When $W = 8 \mu m$, $V_{SD} = 1V$

$$I_{D_N} = -0.213 \times 800[1 + 2.333(1 - 0.55)] \mu A = -0.349 mA$$

The discrepancy between hand calculation and simulation result may because of Modern transistors (e.g. 45nm process we use) exhibit short-channel effects that are included in Cadence simulations but ignored in basic theoretical models.

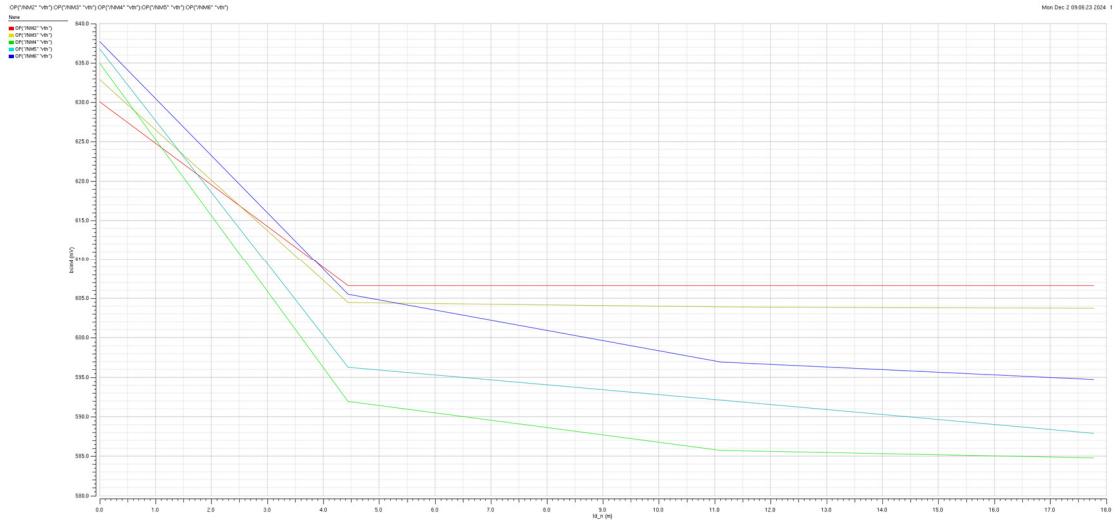
At high V_{DS} , carrier velocity saturates rather than increasing linearly with the electric field. This leads to a higher current than predicted by the quadratic relationship in the theoretical model.

In addition, a high V_{DS} could also reduce effective V_{th} , which brings larger I_D .

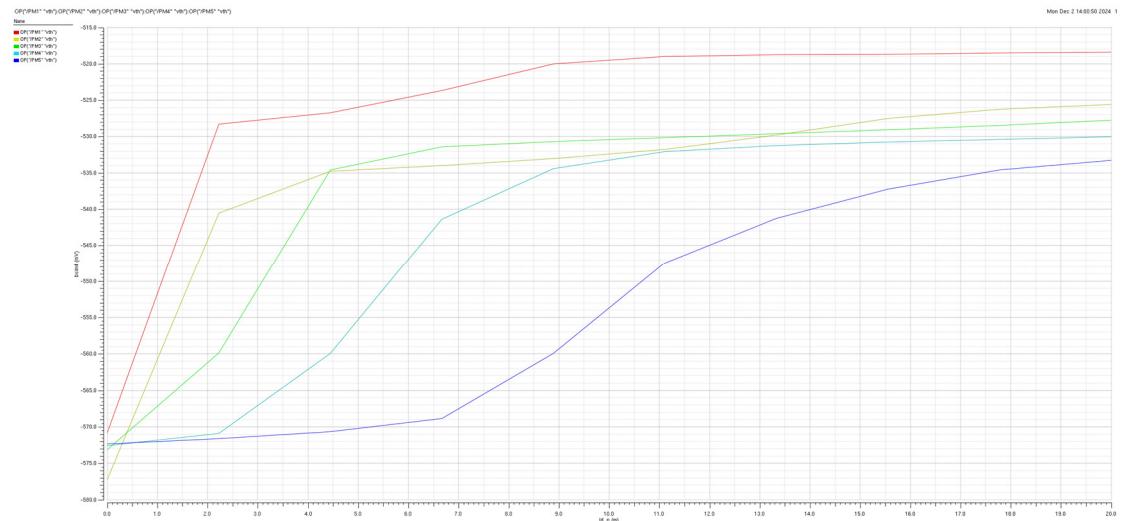
2. V_{th} vs. I_D (NMOS)

To clarify, NM_{2-6} in following graph with width of $0.5\mu m, 1\mu m, 2\mu m, 4\mu m, 8\mu m$
 PM_{1-5} in following graph with width of $0.5\mu m, 1\mu m, 2\mu m, 4\mu m, 8\mu m$

Simulation result:



V_{th} vs. I_D (PMOS)



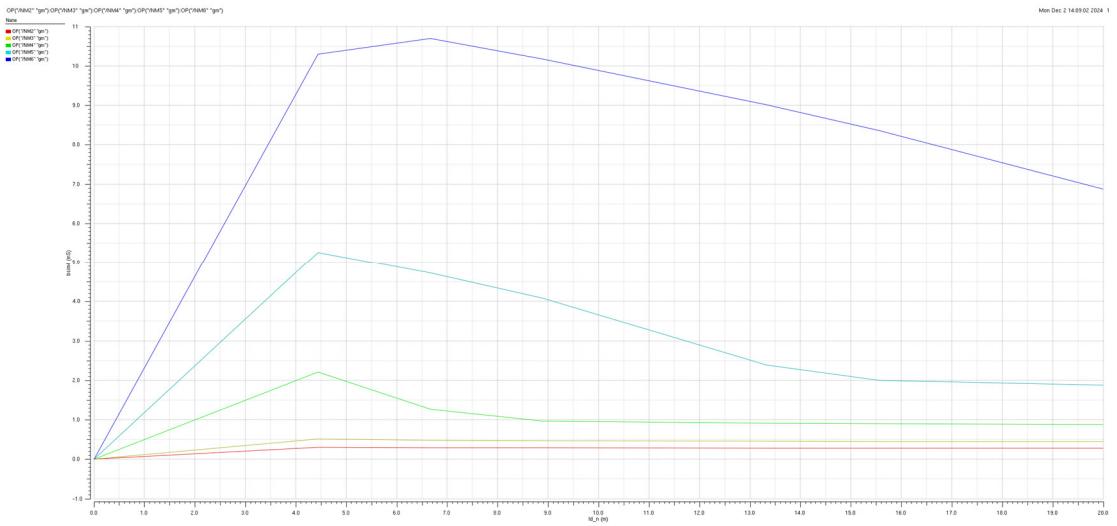
Hand Calculation:

$$V_{th} = V_{th0} + \gamma(\sqrt{|\phi_s + V_{SB}|} - \sqrt{|\phi_s|})$$

Since there is no body effect ($\gamma = 0$), $V_{th} = V_{th0}$ should not change. However, channel length modulation (CLM) will slightly influence the V_{th} . With I_D increase, V_{DS} will increase, which cause the reduction of L_{eff} . Therefore, V_{th} will be lower. When I_D is big enough to reach the velocity saturation, V_{th} will remain stable.

3. g_m vs. I_D (NMOS)

Simulation result:



Hand Calculation:

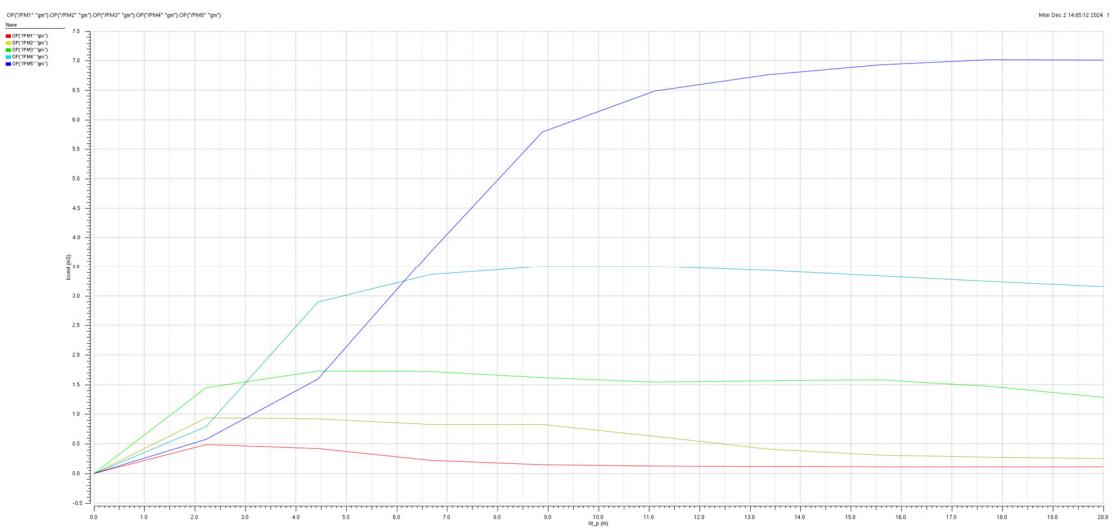
$$\begin{aligned}
 g_{mN} &= \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \\
 &= \sqrt{2 \times 157.2 \mu A/V \times \frac{W}{45 nm} I_D} \\
 &= 0.083 \sqrt{W I_D} \text{ mS}
 \end{aligned}$$

The trend is match with the simulation result. When \$W = 8 \mu m\$, \$I_D = 4 mA\$

$$g_{mN} = 0.083 \sqrt{800 nm \times 4 mA} = 4.695 \text{ mS}$$

\$g_m\$ vs. \$I_D\$ (PMOS)

Simulation result:



Hand Calculation:

$$\begin{aligned}
g_{m_P} &= \sqrt{2\mu_p C_{ox} \frac{W}{L} I_D} \\
&= \sqrt{2 \times 63.4 \mu A/V \times \frac{W}{45nm} I_D} \\
&= 0.053\sqrt{WI_D} mS
\end{aligned}$$

The trend is match with the simulation result. When $W = 8 \mu m$, $I_D = 4 mA$

$$g_{m_N} = 0.053\sqrt{800 nm \times 4 mA} = 2.998 mS$$

The discrepancy between hand calculation and simulation results also caused by short channel effects in 45 nm process.

High V_{DS} reduces the effective V_{th} , causing I_D to increase more rapidly with V_{GS} , resulting in a higher g_m . Also, the velocity saturation will cause slightly I_D increase in simulation result.

4. C_{gs} and C_{gd} vs. W (NMOS)

Simulation result:



If we ignore the sign, C_{gs} is proportional to W with $k = 0.67 fF/\mu m$
 C_{gd} is proportional to W with $k = 0.15 fF/\mu m$

Hand Calculation:

In simulation, NMOS is diode connected. Therefore, we use formula of C_{gs} and C_{gd} in saturation region to do hand calculation.

$$\begin{aligned}
C_{gs} &= \frac{2}{3} W L C_{ox} + W C_{ox} L_{ov} \\
&= \frac{2}{3} \times \frac{17.78 fF}{\mu m^2} \times 45 nm \times W + 0.152 W fF \\
&= 0.6854 W fF
\end{aligned}$$

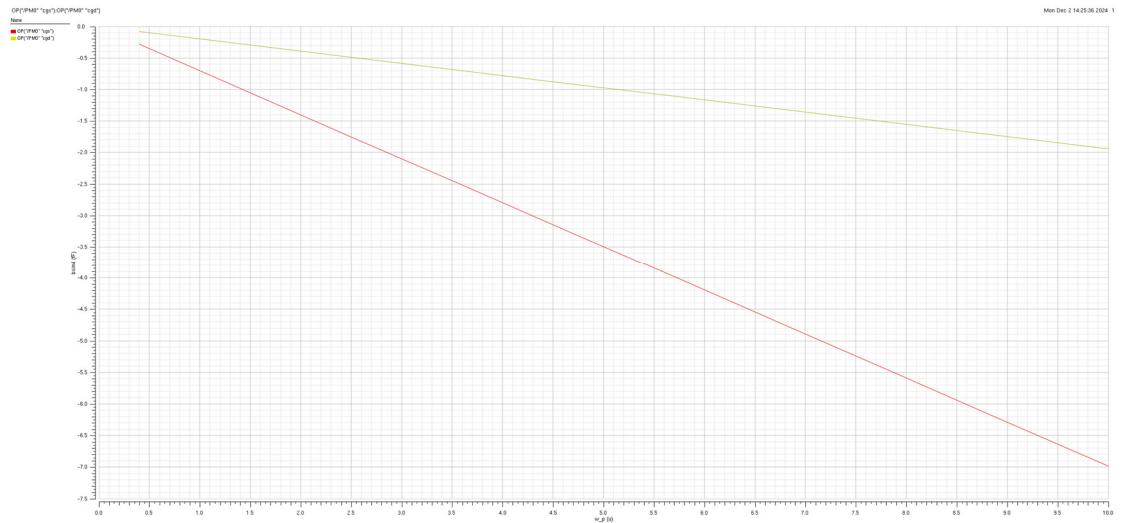
$$C_{gd} = WL_{ov}C_{ox}$$

$$= 0.152W \text{ fF}$$

Both C_{gs} and C_{gd} are very close to the simulation result.

C_{gs} and C_{gd} vs. W (PMOS)

Simulation result:



If we ignore the sign, C_{gs} is proportional to W with $k = 0.705 \text{ fF}/\mu\text{m}$
 C_{gd} is proportional to W with $k = 0.15 \text{ fF}/\mu\text{m}$

Hand Calculation:

In simulation, PMOS is diode connected. Therefore, we use formula of C_{gs} and C_{gd} in saturation region to do hand calculation.

$$C_{gs} = \frac{2}{3}WL_{ov}C_{ox} + WC_{ox}L_{ov}$$

$$= \frac{2}{3} \times \frac{19.11 \text{ fF}}{\mu\text{m}^2} \times 45 \text{ nm} \times W + 0.152W \text{ fF}$$

$$= 0.7253W \text{ fF}$$

$$C_{gd} = WL_{ov}C_{ox}$$

$$= 0.152W \text{ fF}$$

Both C_{gs} and C_{gd} are very close to the simulation result.

5. f_T (frequency of unity voltage gain)

Since C_{gs} and C_{gd} is constant when W fixed, f_T is proportional to g_m

and thus $f_T \propto \sqrt{I_D}$

For NMOS:

$$\begin{aligned}
f_T &= \frac{g_m}{2\pi(C_{gs} + C_{gd})} \\
&= \frac{\sqrt{0.00698WI_D} \text{ mS}}{2\pi(0.6854W + 0.152W)fF} \\
&= 15.87\sqrt{WI_D} \text{ GHz}
\end{aligned}$$

For PMOS:

$$\begin{aligned}
f_T &= \frac{g_m}{2\pi(C_{gs} + C_{gd})} \\
&= \frac{\sqrt{0.00281WI_D} \text{ mS}}{2\pi(0.7253W + 0.152W)fF} \\
&= 9.61\sqrt{WI_D} \text{ GHz}
\end{aligned}$$

Since the calculation value of C_{gs} and C_{gd} is approximately same with the simulation results, the f_T calculated using simulation value will be larger than the theoretical value because of the g_m . The reason is same to the g_m discrepancy (short channel effect such as velocity saturation and changing V_{th} with higher V_{DS})

iii. Design Strategy

1. Input Stage: Current Gain (CG) Amplifier

The CG amplifier converts the current signal from the photodiode into a voltage signal while maintaining a wide bandwidth. This stage provides large gain. (around 80dB)

- Use a common-gate configuration for its wideband performance and low input impedance, which minimizes the impact of the parasitic capacitance at the photodiode.
- Select the transistor dimensions to ensure high g_m while maintaining stability and low noise (noise mainly come from this stage).

2. Intermediate Stage: Differential Amplifier

This stage is to amplifies the signal further and converts it into a differential output. The gain is lower than the first stage (around 20dB)

- Use a differential pair with a current mirror load to ensure good common-mode rejection and high gain.
- Optimize the transistors' W/L for high g_m while not lost too much bandwidth.
- The tail current source must be carefully designed to ensure consistent operation and good linearity.

3. Output Stage: Buffer

Drives the load impedance (600Ω differential) without large significant signal degradation or loading of the intermediate stage.

- Use a source-follower for low output impedance.
- Optimize the transistor sizes for sufficient current driving capability while minimizing power consumption.
- Ensure the stage operates within the output voltage swing specifications

General Considerations Across Stages

Between each stage, DC de-coupling capacitor could be used to ensure that the DC operating points of one stage do not interfere with the next stage.

iv. Hand Calculation

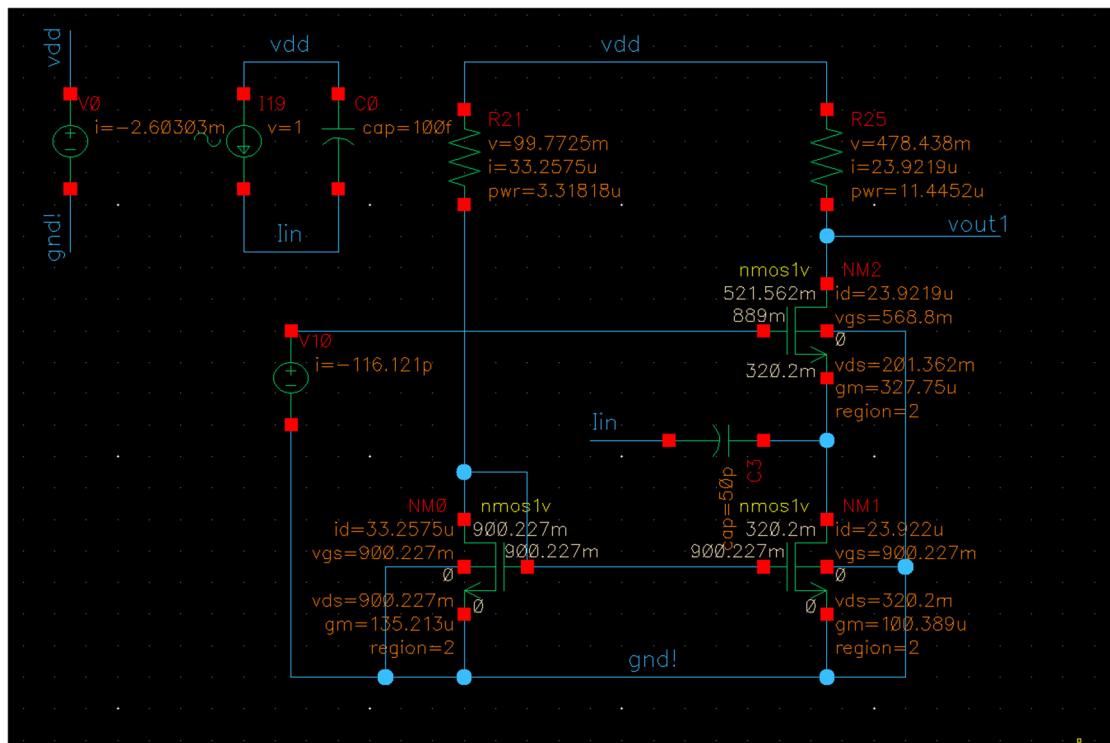
In the first stage:

we want to get 80dB gain. Because the gain of the first stage is just R_d , we set R_d as 20 k Ω .

v. Cadence Simulation Results

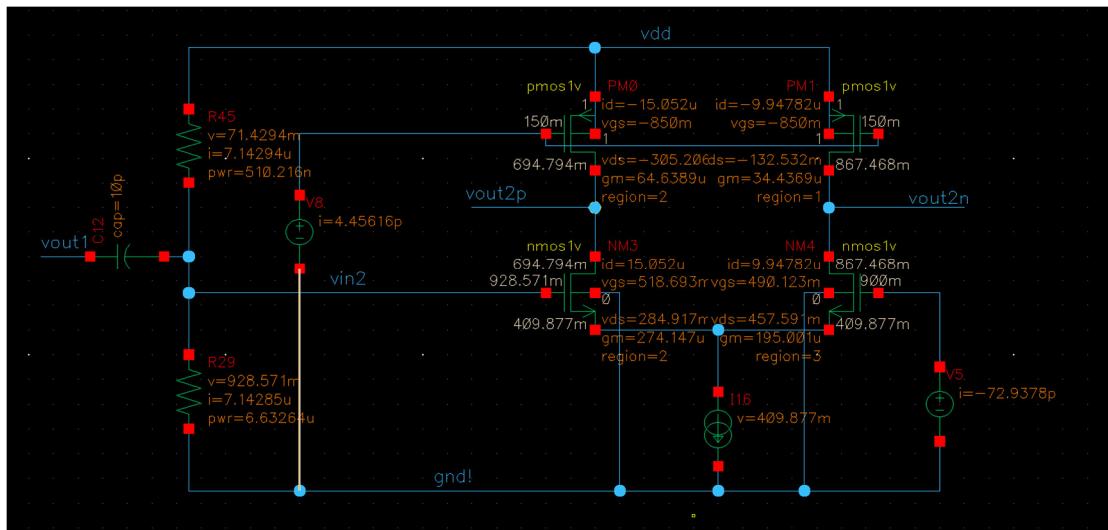
1. DC Operating point table

First stage: CG Amp



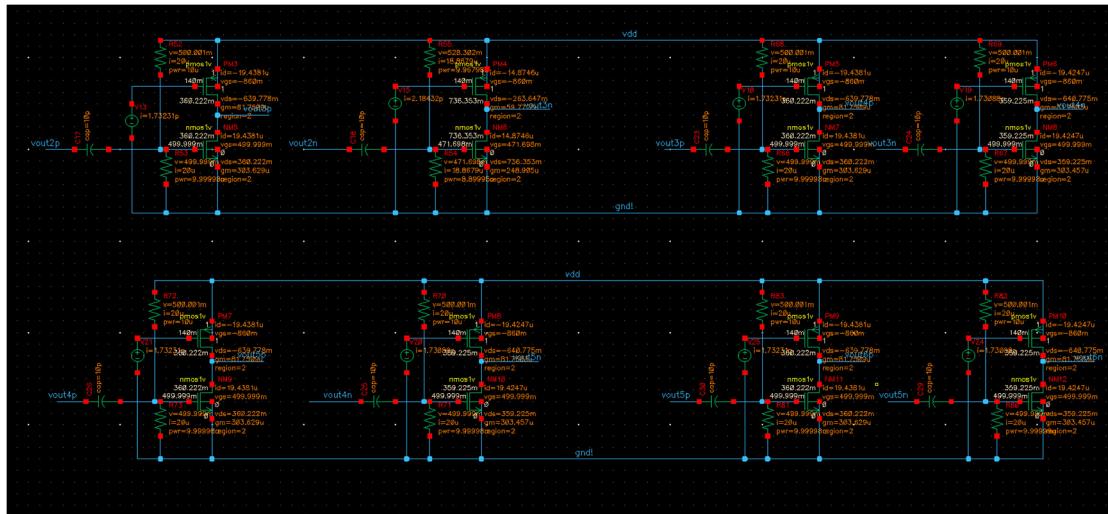
| MOS | I_a | V_{gs} | V_{ds} | g_m | Region |
|-----|----------|----------|----------|----------|--------|
| NM0 | 33.25 uA | 900 mV | 900 mV | 135 uA/V | 2 |
| NM1 | 23.92 uA | 900 mV | 320 mV | 100 uA/V | 2 |
| NM2 | 23.92 uA | 568 mV | 201 mV | 327 uA/V | 2 |

Second stage: Differential Amp



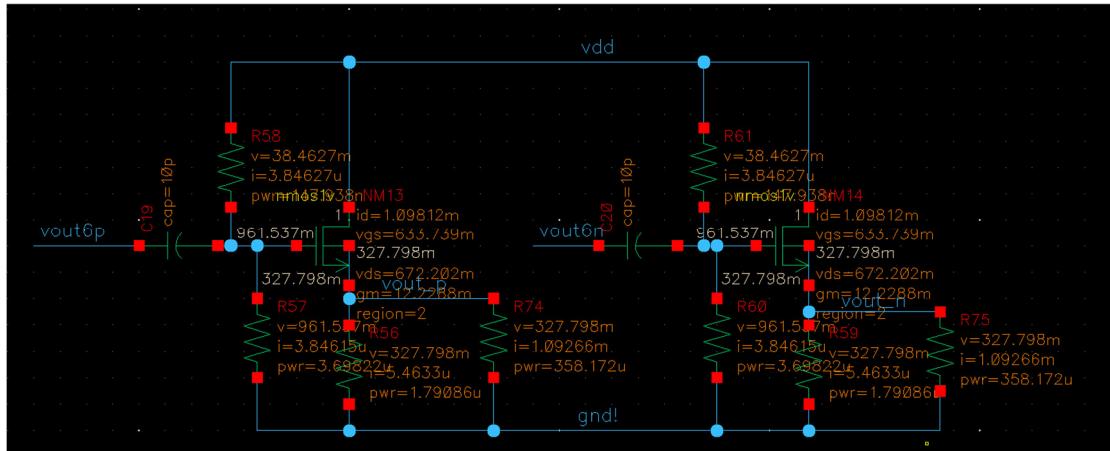
| MOS | I_d | V_{gs} | V_{ds} | g_m | Region |
|-----|---------|----------|----------|----------|--------|
| NM3 | 15 uA | 518 mV | 284 mV | 274 uA/V | 2 |
| NM4 | 9.9 uA | 490 mV | 457 mV | 195 uA/V | 3 |
| PM0 | -15 uA | -850 mV | -305 mV | 64 uA/V | 2 |
| PM1 | -9.9 uA | -850 mV | -132 mV | 34 uA/V | 1 |

Third stage: CS Amp Array



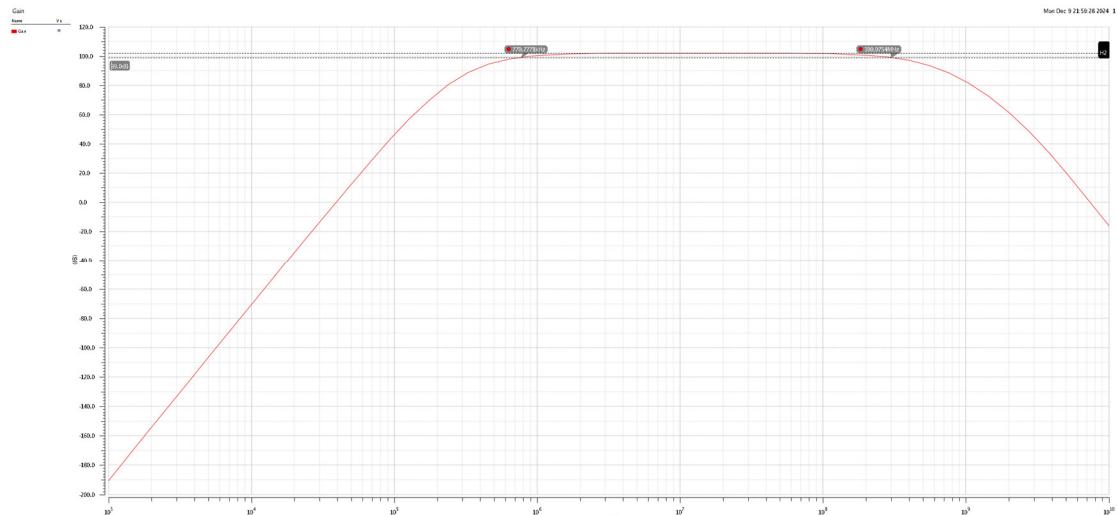
| MOS | I_d | V_{gs} | V_{ds} | g_m | Region |
|----------|----------|----------|----------|-----------|--------|
| NM5-NM9 | 19.43 uA | 500 mV | 360 mV | 303 uA/V | 2 |
| PM3-PM10 | -19.43uA | -860 mV | -640.mV | 59.77uA/V | 2 |

Last stage: Buffer (Source follower)

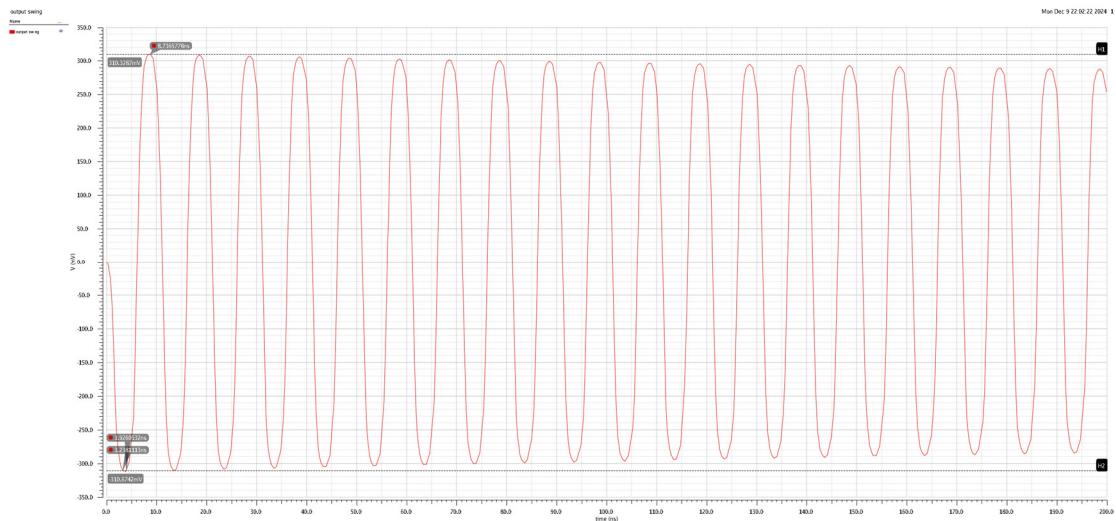


| MOS | I_a | V_{gs} | V_{ds} | g_m | Region |
|------|---------|-----------|----------|-----------|--------|
| NM13 | 1.09 mA | 633.74 mV | 672.2 mV | 12.2 mA/V | 2 |
| NM14 | 1.09 mA | 633.74 mV | 672.2 mV | 12.2 mA/V | 2 |

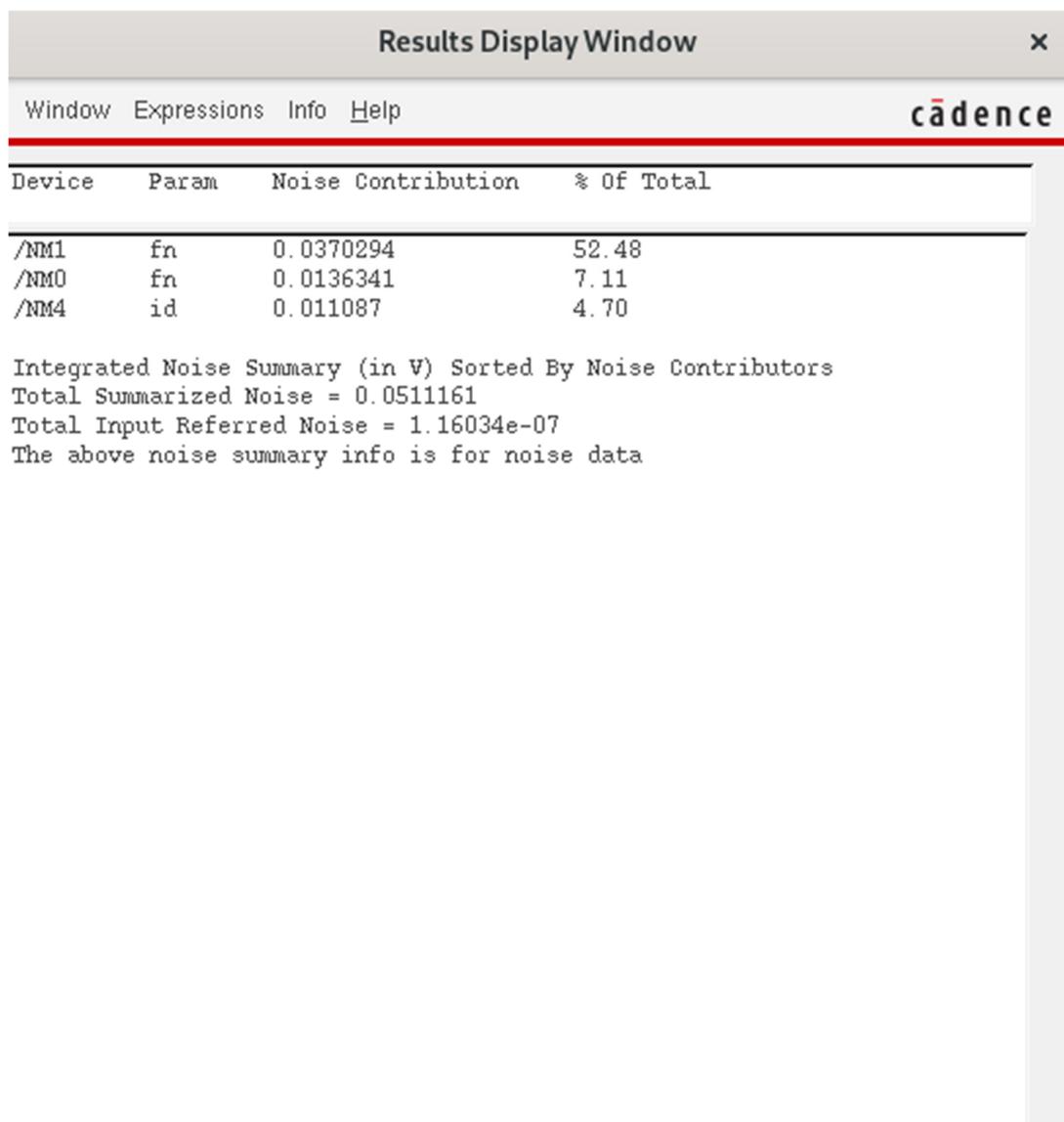
2. AC Simulation (transfer function)



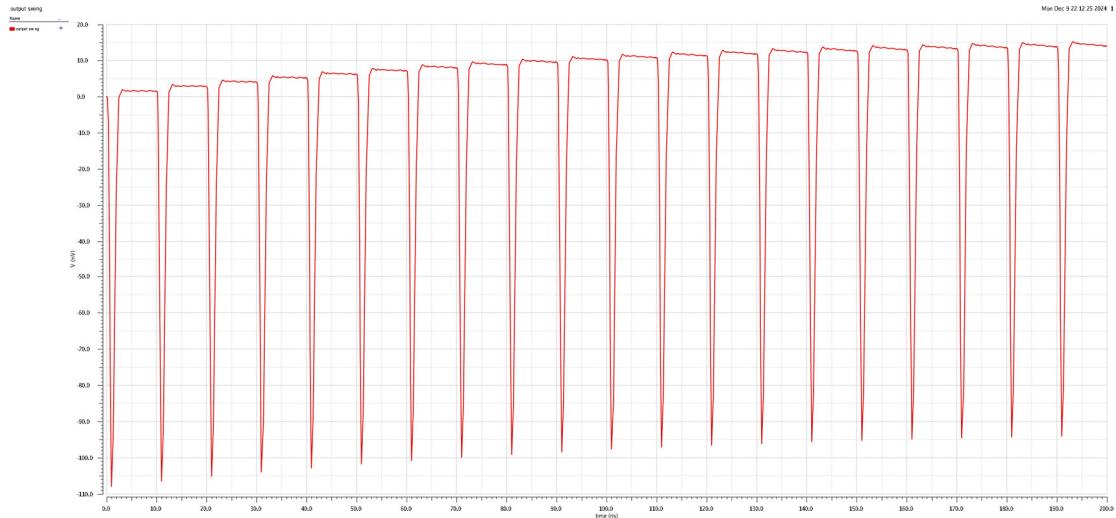
3. Transient Simulation (output swing)



4. Noise Simulation



5. Stability (Step response)



6. Table of Comparison

| No. | Parameter | Requirement | Value |
|-----|------------------------------------|----------------------|-----------|
| 1 | output peak-to-peak voltage swing | > 0.4V(differential) | 0.62 V |
| 2 | Transimpedance gain | > 150 kΩ | 158.48 kΩ |
| 3 | The -3dB upper corner frequency | > 250 MHz | 300 MHz |
| 4 | The -3dB low corner frequency | < 10 MHz | 0.77 MHz |
| 5 | Total input referred current noise | < 125 nA | 116 nA |
| 6 | Total power consumption | < 15 mW | 6 mW |

vi. Comparison of hand calculation and simulations

The discrepancy between hand calculation and simulation result is because of Modern transistors (e.g. 45nm process we use) exhibit short-channel effects that are included in Cadence simulations but ignored in basic theoretical models.

At high V_{DS} , carrier velocity saturates rather than increasing linearly with the electric field. This leads to a higher current than predicted by the quadratic relationship in the theoretical model.

vii. Conclusion

The design and implementation of the wideband Trans-Impedance Amplifier (TIA) presented in this project successfully meet the specified performance requirements, including gain, bandwidth, noise, and power consumption. Through careful process characterization and simulation in a 45nm CMOS

process, we observed strong agreement between theoretical calculations and simulated results, with minor discrepancies attributed to short-channel effects and parasitic inherent to advanced processes.

The TIA design employs a three-stage architecture: a current-gain common-gate amplifier, a differential amplifier for differential voltage output, and an output buffer to ensure low impedance and load driving capability. In addition, to further increase the gain and voltage swing, a series of common source amplifier are used to amplify the signal without bring large input referred noise (because of the main noise source is the first stage).

Key performance metrics, such as transimpedance gain (158.48 kΩ), -3dB bandwidth (300 MHz), and input-referred current noise (116 nA), exceed the design targets. The power consumption of 6 mW also falls well within the specified limit, underscoring the energy efficiency of the implementation.

Overall, this project demonstrates the effectiveness of combining theoretical analysis, simulation, and modern CMOS design principles to develop a robust TIA suitable for high-speed optical and RF communication systems. The insights gained here can serve as a foundation for further enhancements, such as integrating inductive peaking or adaptive feedback for extended performance in future designs.

viii. References

1. Razavi, Behzad. *The Design of a Transimpedance Amplifier*. IEEE Solid-State Circuits Magazine, Winter 2023. DOI: 10.1109/MSSC.2022.3219682
2. Razavi, Behzad. *The Transimpedance Amplifier: A Circuit for All Seasons*. IEEE Solid-State Circuits Magazine, Winter 2019. DOI: 10.1109/MSSC.2018.28818