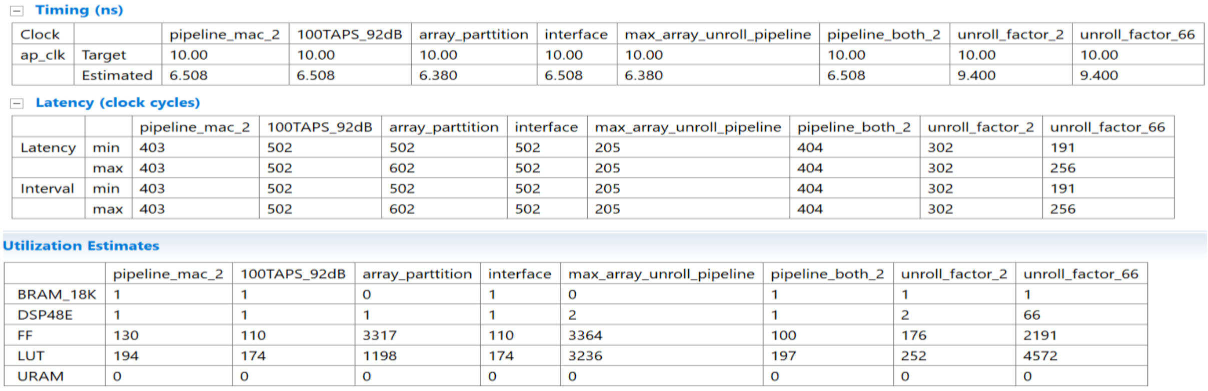
Report

Xrenzh00

Extension of FIR Filter: 100TAPS filter (92dB)



⊟ Timing (ns)

Clock		pipeline_mac_2	100TAPS_92dB	array_parttition	interface	max_array_unroll_pipeline	pipeline_both_2	unroll_factor_2	unroll_factor_66
ap_clk	Target	10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00
	Estimated	6.508	6.508	6.380	6.508	6.380	6.508	9.400	9.400

⊟ Latency (clock cycles)

		pipeline_mac_2	100TAPS_92dB	array_parttition	interface	max_array_unroll_pipeline	pipeline_both_2	unroll_factor_2	unroll_factor_66
Latency	min	403	502	502	502	205	404	302	191
	max	403	502	602	502	205	404	302	256
Interval	min	403	502	502	502	205	404	302	191
	max	403	502	602	502	205	404	302	256

Utilization Estimates

	pipeline_mac_2	100TAPS_92dB	array_parttition	interface	max_array_unroll_pipeline	pipeline_both_2	unroll_factor_2	unroll_factor_66
BRAM_18K	1	1	0	1	0	1	1	1
DSP48E	1	1	1	1	2	1	2	66
FF	130	110	3317	110	3364	100	176	2191
LUT	194	174	1198	174	3236	197	252	4572
URAM	0	0	0	0	0	0	0	0

Answer

1- description of the step of Extension FIR filter.

I applied different techniques to fig out the different solution also printf Signal and Nosie in case to determine how different filter coefficient and TAPS can be influent filter performance, and then I simplify mixing all techniques together to get less latency and resource cost.

a: generally, every tap need singe mac, singe mac operation takes 1 CPU clock cycle =1/766,therefore, at most 766 TAPS.

b:66 TAPS are able to implement in FPGA logic since set pragma resource to boundary context, Otherwise, TAPS its depends on sample frequency.(theory) but when I try to implement more TAPS and resource do not change, only latency changed

c: basically resource and specific requirement are limits the further extension of the FIR filter.

For example: using resource technique can representment var to dsp48e

Reference: http://www.stud.fit.vutbr.cz/~xnovot96/iir/example-1.html to generate coefficient set