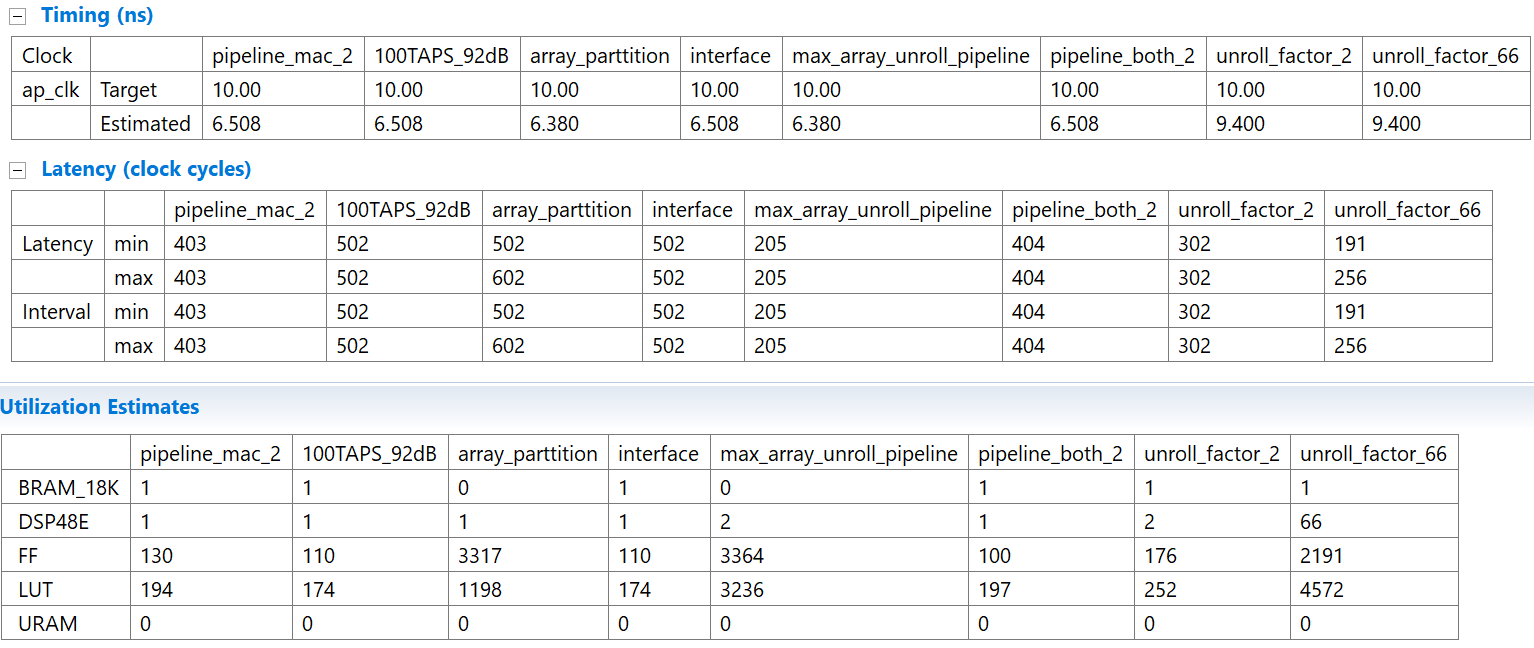
# Report

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Extension of FIR Filter: 100TAPS filter (92dB)



**Answer**

1. **description of the step of Extension FIR filter**.

I applied different techniques to fig out the different solution also printf Signal and Nosie in case to determine how different filter coefficient and TAPS can be influent filter performance, and then I simplify mixing all techniques together to get less latency and resource cost.

**a**: generally, every tap need singe mac, singe mac operation takes 1 CPU clock cycle =1/766,therefore, at most 766 TAPS.

**b**:66 TAPS are able to implement in FPGA logic since set pragma resource to boundary context, Otherwise, TAPS its depends on sample frequency.(theory) but when I try to implement more TAPS and resource do not change, only latency changed

**c**: basically resource and specific requirement are limits the further extension of the FIR filter.

For example: using resource technique can representment var to dsp48e

Reference: [http://www.stud.fit.vutbr.cz/~xnovot96/iir/example-1.html](http://www.stud.fit.vutbr.cz/~xnovot96/iir/example-1.html?fbclid=IwAR01f5CB6_os3zFZxjNdLGd4a0H7qT_zoAU2axWb8E6Df8fbJMIkCw7eEiQ) to generate coefficient set